Design and Analysis of VLSI Subsystems
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Lecture - 80
TPDQ and TPCQ

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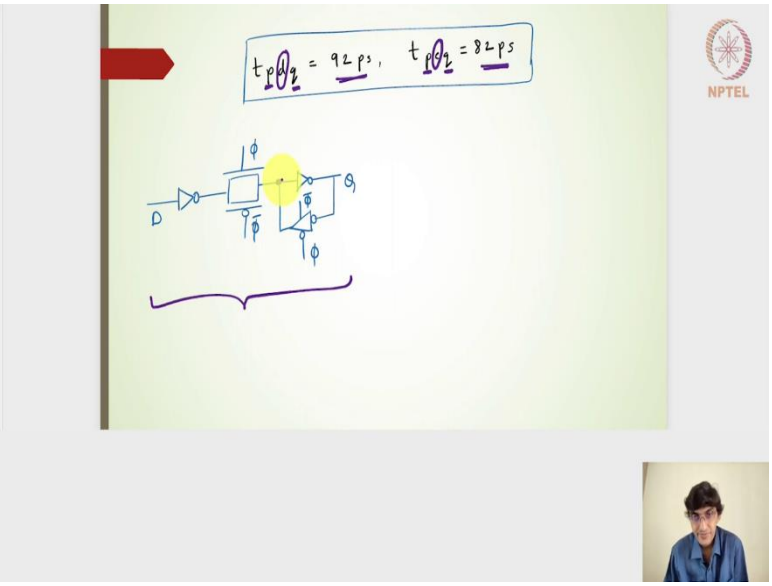

Let us have a look into this particular t_{pdq} = 92ps and then the t_{pcq} = 82ps. This is kind of characterized from the latch design and it is nothing to do with the pulse clock or generating signals, because once the pulse signal is given to the latch design, the latch output is my Q signal.

Then p stands for the propagation, the only thing we have to see is why is the delay from D to Q higher than the delay from clock to Q alright. If I in that case I will have to look into the latch designs here. If I consider the latch design here this is the latch design a simple CMOS latch design.

I have an inverter here and then the transmission gate and then inverter followed by the tristate inverter. This inverter and this inverter will ensure that the output noise are not coupled inside the latch and this particular feedback tristate inverter helps in ensuring that this particular node is static size.

Let us have a look into this particular design and see that what is the delay from D to Q and what is the delay from C to Q and then try to understand whether it should be higher.

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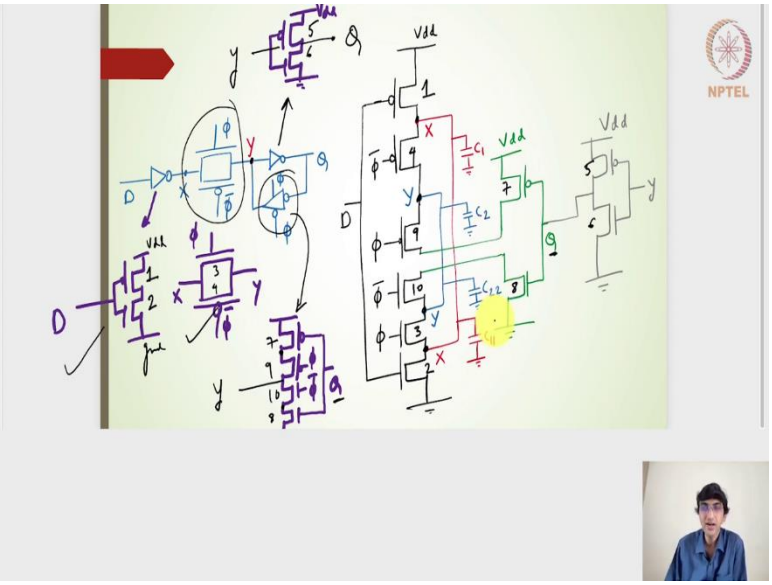

If this is my gate level diagram and this will be my transistor level diagram. Let us have a look into it. What I am going to do is I am going to draw the transistor for individual gates here. I am going to draw the inverter, this inverter I am going to draw the transistor here for the inverter.

This is my D input and let me also number it out, this is transistor PMOS number 1 and NMOS number 2 or rather I will say the transistor number 1 and transistor number 2 and this is the that the transmission gate. I will just redraw the transmission gates because it is the transmission gate is anyways has the transistors, this is ϕ and this is $\overline{\phi}$ and let me say that this is the node X and then this is the node Y and let me also write the number as 3 and 4 here.

The NMOS is 3 transistor and the fourth is the PMOS transistor and then I have this particular inverter. I will also draw this particular inverter, this is V_{dd} and then this is ground and let us say that this particular transistor is transistor number 5 and 6 and we have this tristate inverter.

Let me draw the tristate inverter there should be 4 such inverters. I am going to draw it something like this and ground and then this is V_{dd} and this is my Q signal, Q input and

this 2 will be $\overline{\phi}$ and ϕ here. Remember that this tristate inverter works when the clock is low here. When the clock is high we will have this transmission gate to be passing the signal. During the $\overline{\phi}$ signal this particular output will be passed from this tristate inverter.

The $\overline{\phi}$ to the NMOS here and transmission gate we will have the ϕ to the NMOS and let me also write the transistors here. We completed 5, 6, I will write it as 7 and 8 and then finally, 9 and 10. There are 10 transistors and then this 10 transistors I have configured into this particular transistor level schematic. But I am trying to club it in together. So, that I can visualize what happens to the D to Q output and clock to Q output.

Let me map this transistor into that particular transistor schematic into this particular schematic. The D signal is going to 1 and 2 transistor. Which are closer to the V_{dd} rail, so this is V_{dd} and then this is ground. The transistor number 1 is here, the transistor number 2 is here that is where the input D is going our transistors closest to the V_{dd} and then the ground rail, that is good. This is done and then we have the 3 and 4. The 3 goes to this is 3 and then this is 4 on one side it is the X input on one side. It is the X input on one side it is the X input for both the 3 and 4 transistors. The other diffusion is the Y nodes or the other diffusion is Y node here and that is why I have connected this X and Y together. My 3 and 4 transistors are also done and now I am taking this particular transistor ϕ and $\overline{\phi}$ signal, that is basically 9 and 10, 9 on the PMOS side.

The transistor number 9 and then the transistor number 10 within gate signal as ϕ and $\overline{\phi}$ respectively 9 and 10 transistors. On one side it is the Y input, this Y input is there or rather this output is nothing but the Y output, that is what it is. I should have written it before, this is the output is the Y output.

For the 9 and 10 transistors, the 9 and 10 transistors on one side it is the Y output. This is the Y output the 9 and 10 transistors alright and on the other diffusion it goes and that is connected to the 7 and 8 transistors. The 9 transistors on one side diffusion it is Y and on the other side it goes to this particular inverter, this particular inverter and I am going to call this as let us say 7 and 8. Then 7 and 8 look at the 7 and 8 it is nothing but it is going to the rail on one side and then the rail on the other side of the 8 transistor. It is satisfies 8 and $7V_{dd}$ and 8 gets connected to the graph.

The input to the 7 and 8 is nothing, but the Q signal and the input to the 7 and 8 is the Q signal here. Finally this particular inverter also output is Q the input is Y here. This output Q it is output of the 5, 6 transistors. I am going to write it as transistor number 5 and 6 where the input is Y and the output is Q.

I have covered all the 10 transistors here and try to make it as compact as possible. This transmission gate especially some part of this tristate inverter we are trying to club it in this particular stage. Having the same nodes X Y and then it takes this particular transistor or rather this particular clock, then the clock signals are given appropriately.

In that sense this schematic is very very similar to this particular gate level diagram or it satisfies the gate level diagram. Now if I actually find out the diffusion common or the merge diffusion capacitances here it is nothing but I have written it as this 1 and this 1, 1 and 4 transistor will have a emerge diffusion capacitance of C_1.

The Y is nothing, but the node of the merge diffusion node of the 9 and 4 transistor which is C_2. Similarly we will have C_{22}, C_{22} and C_{11} on the pull out side. Now if I look into this particular 4 capacitances then we should be able to make a comment on the delay from D to Q and the delay from the clock to Q.

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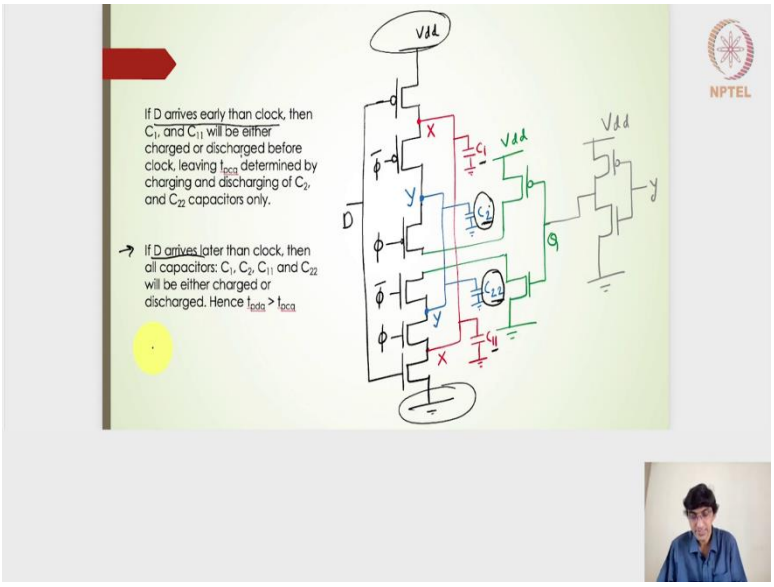

Now, let us say that if the D arrives earlier then the clock, the D signal is given here. The D arrives earlier than the clock, the clock arrives later. This 4 transistors we have the clock signals and let us say that the clock arrives later, but the D arrives earlier.

If the D arrives earlier we know that C_{11}, C_1 as well as C_{11} can either get discharged completely or it will be charged completely. Whenever the clock arrives then the output before the clock leaving the t_p C_{11} C_1 and C_{11} will either be discharged or charged before the clock leaving the propagation clocked to Q determined by the charging of only C_2 and C_{22}.

What it means is? If the D signal arrives earlier then this C_1 and C_{11} is either discharged or charged it is already been done and then when the clock arrives it leaves only this particular capacitance C_2 and C_{22} to be charged appropriately. The delay here from clock to Q actually depends on only the C_2 and C_{22} transit capacitance to be either charged or discharged. It does not know the C_1 and C_{11} are not in the picture at all, because it is already been charged or it is already been discharged.

Let us say if it is the other case if the D arrives later. Then the clock although the clock is as arrived earlier. Even though if it has done that way the C_2 charge will be shared by the C_1 it will be only be shared by the C_1. But it does not go to V_{dd} or go to the ground it will be only be shared by C_2 will share with the C1 C_{22} will share with C_{11} and then vice versa. If the D arrives later then it provides a part of the V_{dd} a source path of V_{dd} or a sink path of ground and that is when all the charge that has been there in C_2 C_1 C_{22} and C_{11} will either be discharged complete to the ground or it will be charged to the V_{dd}.

When the D arrives later than the clock then all the capacitors will be either recharged or discharged and hence for the delay from D to Q we have to account for all the capacitances here. Whereas, for determining the clock to Q determining the clock to Q only C_2 and C_{22} transistors are accountable. The C_1 and C_{11} has anyways been completely discharged or it has been charged completely. That is why we always get the t_{pdq} to be slightly higher than the t_{pcq} for both the pulse latches as well as in the latch design. That is something it is a characteristic of the latch and not the characteristics of the clock or the pulse signal. Hope you are able to understand this.