Design and Analysis of VLSI Subsystems
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Lecture - 78
Static Timing Analysis - Part 2.1

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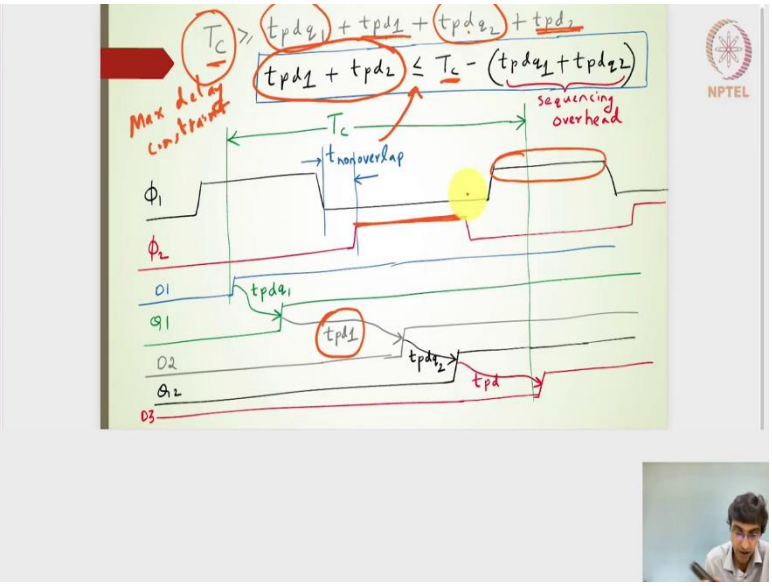

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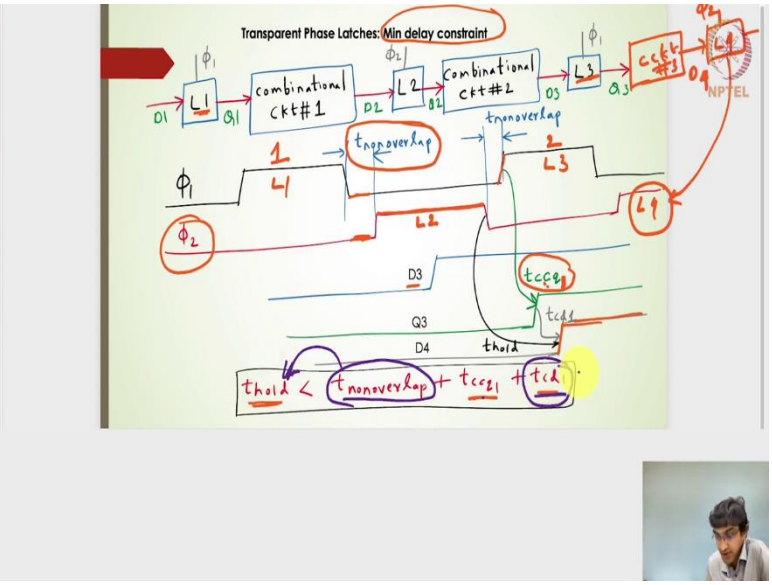

Moving further what should be the minimum delay constraints. Now this is very interesting to see here I have a clock 1 and then the clock 2 and the clock 1 and clock 2 have some

tnon-overlapping time, tnon-overlapping time means we do not have any overlapping of between the clock 1 being high and clock 2 being high.

Only when the clock 1 goes low we will have the clock 2 going high. Of course, there will be an overlapping for the clock being low, but that is not the definition of the t nonoverlap, the definition of t nonoverlap is both of them are not high at any point of time because that is what we are giving the high level of the latch. The latch is working in a positive level of the clocks. Both the latches L1, L2, L3 and so on are working in the positive level of the latches. We have the definition of t nonoverlap with respect to the high level of the clocks. We have this clock 1 and clock 2 now and let us say that we have a combinatorial circuit here also which is nothing but the similar to the combinatorial circuit 1.

I will write it as circuit number 1 or I can write it as a circuit number 3 which is all the even odd numbers are same goes to the latch number 4. Again, latch number four we will have the clock 2 signal. Let us say that we have the contaminated output whatever the D1 the Q1 the D2 and then the Q2 and then the D3 signal. The D3 signal has arrived much earlier.

It has arrived much earlier here and the Q3 which is the output of the latch 3 and remember that the clock the latch 3 should work for the clock 1 and latch 1 should work for the clock 1, but the latch 1 will work it is supposed or expected to work in the 1st clock edge and L3 should work in the second or rather the 2nd clock level. The 1st clock level and then the 2nd clock level the L 3 should work.

That is what I am writing here L3 and L1 alright and for the $\phi 2$ we wanted L2 to capture in the clock 2 first high level and L4, the L4 should work in the 2nd clock level of the clock 2. With that in mind let us say that the D3 signal has arrived here and then a D3 signal should be captured, D3 which is nothing but the L3 latch should capture it in the 2nd clock level of the $\phi 1$ clock.

The D3 is here, the Q3 will be with respect to the propagation of clock whenever the clock goes high we will say that it will be its a contaminated output let us say that we are taking into account the contaminated output because this is what the minimum delay constraints we are talking about with respect to the contaminated output we have to see whether there is any hold time failures and if at all there is a hold time failure we need to add a buffer.

So, that it avoids the hold time failures, if I consider the very fast output which is nothing but a contaminated output. The clock to Q and here we are taking clock to Q because the D3 signal has already come and it is just waiting for the clock to do the transition and then we will get the output of Q3 alright.

If I have the clock Q3 here and this will be the contaminated clock to Q for the latch number 3 which is nothing but similar to the design of the latch number 1 and that is why I have written as clock to Q instead of 3 I have written it as 1, because the designs of latch 1, 3, 5 and all the odd number of latches are still the same and after that we will have the combinatorial circuit number 3 passing the output here.

This will be D4, my D4 signal will come after the contamination delay of the combinatorial circuit number 3 and we can assume that combinator circuit number 1 and combinatorial circuit number 3, 5, 7 all of them are the same characteristics.

In that sense the t_{cd1} is written instead of t_{cd3} and then we will get very close here. This is my D4 signal, the D4 signal is supposed to be captured in the 2nd level of the clock, but if it is very very close to the level the 1st level of the clock 2 and it is close in the sense that if it is false within the t hold time of the design for the latch 4, latch 2 and latch 6. Which is having the same characteristics if it falls within the t hold time then it can actually get sneaked in. The output here D4 output which we are expecting in the 2nd level of the $\phi 2$ clock, but it can get actually sneaked in the 1st level of the clock 2 and to ensure that does not happen we have to make sure that $t_{cd1} + t_{ccq1}$.

$$t_{hold} < t_{nonoverlap} + t_{ccq1} + t_{cd1}$$

I am assuming that the combinatorial circuit number 3 and all the odd number of combinatorial circuits have the same characteristics and the latches odd number of latches and then even the odd number of latches has the same characteristics of the t_{ccq} and then the t_{cd} are the same. I can instead of 3 I can write it as 1 and t nonoverlap will remain the same throughout the both the clocks, it should be more than that of the t_{hold} time.

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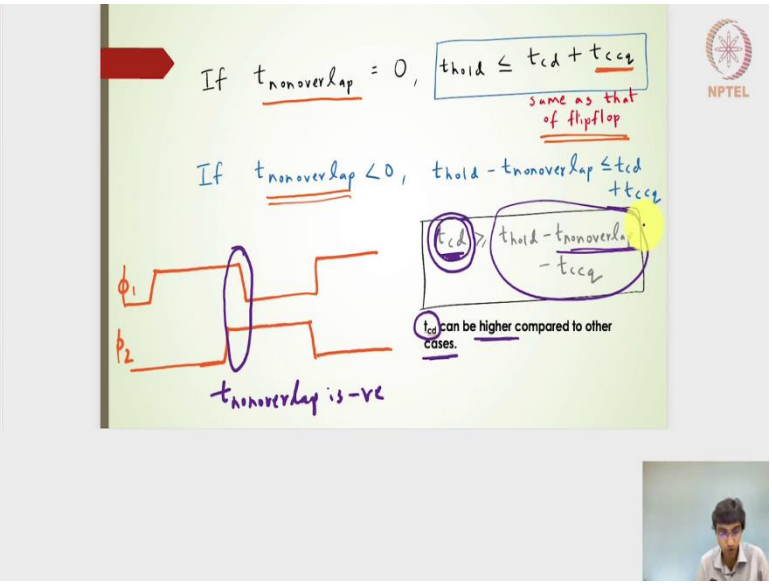

What we are supposed to design is the

$$t_{hold} \leq t_{cd} + t_{ccq}$$

$$t_{cd} \geq t_{hold} - t_{nonoverlap} - t_{ccq}$$

Now, what if the $t_{nonoverlap} = 0$ then we should make sure that the $t_{hold} \leq t_{cd} + t_{ccq}$ duration same as that of the flip flop designs. Remember the flip flop design we had this $t_{hold} \leq t_{cd} + t_{ccq}$.

Now, the other condition is what if that t nonoverlap is negative, if I go back to the previous slide you can see that here the t nonoverlap is positive if it is negative that means, what I will have is the clock 1. This is my clock 1 and clock 2 will have some overlapping some positive overlapping time.

This particular duration we can consider it to be of course, non-overlapping time which is negative. In this particular negative the t hold in this particular negative value what is likely to happen is, if I go back to the previous slide if $t_{nonoverlap}$ becomes negative my t_{cd} which I have designed which I am supposed to design for the combinatorial circuit.

This becomes negative, $t_{hold} \leq t_{cd} + t_{ccq} - t_{nonoverlap}$, but the $t_{nonoverlap}$ is itself negative. This negative is going to go here and become more positive, my t_{cd} values is going to actually increase. The t_{cd} values can be higher compared to the other cases. If

$t_{nonoverlap}$ is negative if it has some positive overlapping time the overlapping high time between the 2 clocks then the t_{cd} has to be more.

What it really means is my t_{cd} designs or the designs for the combination circuit which I had much more relaxed design criterias in the earlier case when the $t_{nonoverlap}$ was positive here it is actually ensuring that it goes slightly more. Remember that the propagation delay is always more and the contamination delay should be greater than this particular parameters.

My constraints of the propagation delay in contamination delay we should have some kind of a difference there, but it is coming closer and closer if I have the t non or nonoverlap to be negative. I do not have that much of room now if the t nonoverlap is negative if it is positive then we will have much of a room here, because the t_{cd} value turns out to be a much much less if it is positive value. It will be very very low, but if it is negative value this t_{cd} value will be higher. The t_{cd} that we want to achieve for the combinational circuit will be higher and the design for the combinatorial circuits will not be as much relaxed as when it was for the non overlapping time to be positive, hope this is clear.