**Design and Analysis of VLSI Subsystems**
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**Lecture - 74**
**CMOS Latch and flipflop Design**

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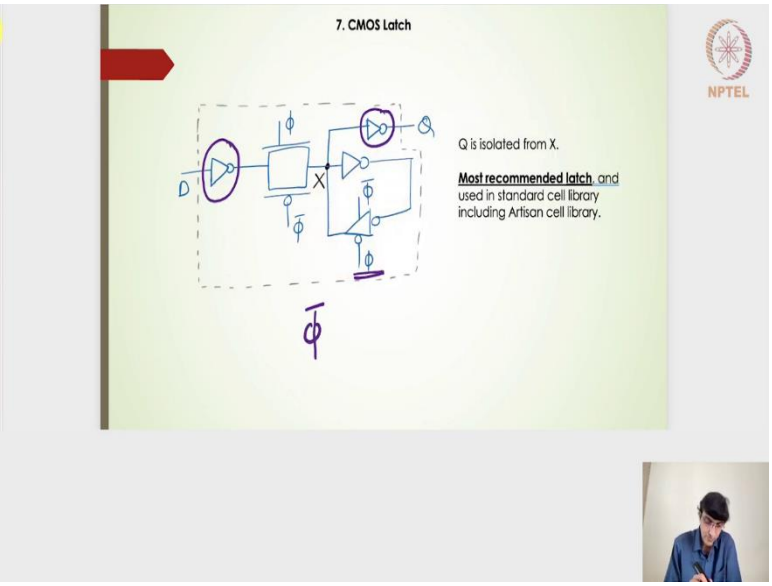


Alright, this is what we had seen the CMOS Latch in the last lecture where we had this particular inverter. This particular inverter is used to make sure that the input noise does not get passed into the output of the flipflop and this particular inverter is there. So, that we avoid the sensitivity of the output noise getting coupled into the input of the latch design.

This particular tri state inverter which is there in the feedback is there to make sure that this particular X node is staticized and it is not the dynamic any more. If it remains to be dynamic or if it remains to be floating there is a possibility of the X node getting discharged to a lower voltage or getting charged to a higher voltage thereby this particular output or the X node voltage level will change due to the sub threshold leakage current.

For the same reason what we have done is added this the tri state inverter especially when the latches in the opaque mode or when it operates in the $\overline{\Phi}$ mode that is when the clock is for the low level of the clock that is when this particular tri state inverter is ensuring that the X node retains to the previous X node. Does not get any changes in the voltage level

and does not have any change in the output values of the latch. This is the most recommended latch and used in the standard cell library including the artisan cell library.

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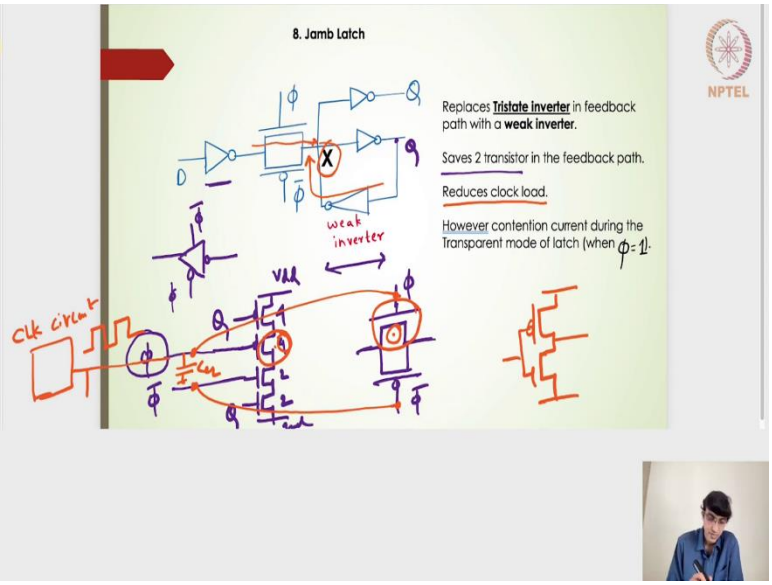


Let take a look at another latch it is called as jamb latch. Instead of the tri state inverter here we are using a weak inverter and everything else remains the same the we have the inverter at the input side we have the inverter at the output side. It takes care of being an insensitive due to the input as well as the output noise.

This one replaces the tri state inverter in the feedback path with a weak inverter, the advantage of the weak inverter is the weak inverter is of 2 transistors the inverter is naturally is of 2 transistors whereas, a tri state inverter because it is a it the 2 transistors the input of the 2 transistors are being clocked. We have 4 transistors in a tri state inverter whereas, in the weak inverter we have only 2 of the transistors.

It saves 2 transistors in the feedback path the other thing is that the clock in the tri state inverter. Let me draw the tri state inverter here. If I go back to the previous slide. This is what I am talking about the tri state inverter which is kind of clocked. What we had was a tri state inverter and this was considered $\overline{\phi}$ and this one was $\phi$.

What it means is I have now 4 transistors of course, this one will be the $V_{dd}$ rail and then this will be will be the ground rail and then this being the PMOS this being the NMOS and we have this connected to this one and then this one is $\overline{\phi}$. Notice that this is $\overline{\phi}$, that is when

the clock level is low these 2 transistors should be on. This should be $\overline{\phi}$ and this should be $\phi$ and the input here is nothing but this coming from here which will be nothing but Q. This particular output is what I am considering here Q and Q.

Remember notice that these 2 transistors whatever is the width of these 2 transistors if it would be regular size of 4 4 and 2 and 2. This goes to the clock this clock is also driving this particular transmission gate. If I draw the transmission gate here somewhere here. I am drawing this particular portion and the transmission gate here. I will have the $\overline{\phi}$ here I will have the $\phi$ here.

What it means is these two connections this point and this point are actually connected and then this $\overline{\phi}$ this one and this one are also connected. What it really means is if there is a clock that has been generated. The clock circuit is there and that is generating the clock signal, there is a circuit here which is generating the clock signal.

It is giving the clock signals it not only has to drive this particular transistor it has to drive this particular transistor also and similarly this inverted one will go to drive this particular transistor and then this particular transistor. Based on this particular size of the transistors this clock or whatever the generating circuit it needs to drive for the total capacitance which is there here as well as here.

Based on the width of this it will have an effective total input gate capacitance which it needs to drive. Now any kind of an additional load is going to make this clock generating circuit or any kind of a circuit to be really slow. We need to increase the strength of this particular clock generating circuit.

Whereas, in a weak inverter I do not have this clock connection to the transistor, in a weak inverter it will be nothing but two of the transistors and then that is about it, this will be the weak inverter, it is an inverter design basically. There is no clocked transistors. That is the reason it says that it reduces the clock load. The additional input capacitance will act as a load to this clock generating circuit.

This will be my clock generating circuit, additional transistors here in the feedback path which is nothing but the clocked or the tri state inverter is going to add to the input capacitance of this particular clock generating circuits output. That is getting reduced with the help of this weak inverter.

However, there is a contention current during the transparent mode of the latch is when this particular transmission gate is going to pass and because there is a weak inverter and does not have any clock to control it.

This is going to be operating every time. It is going to pass a output signal every time and this transmission gate this is going to be positive because my clock is high and that is in the transparent mode. There will be a signal here there will be a signal here, X will be in contention.

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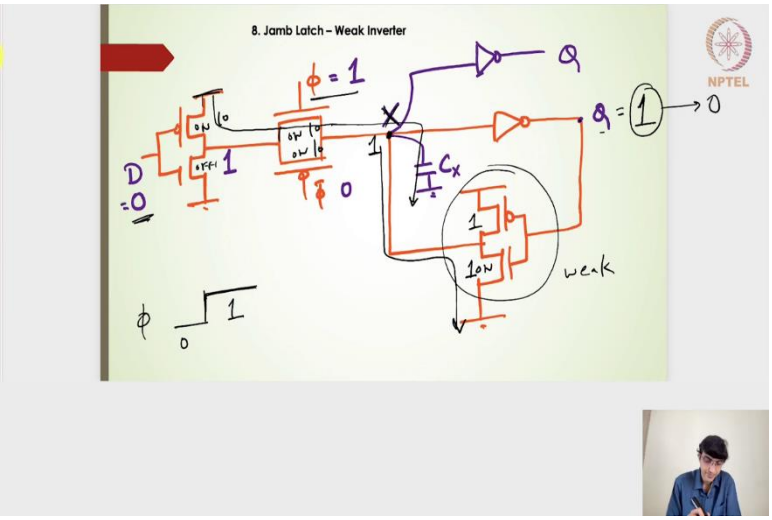


Let us have a look at it in more details. What it means? I have this inverter. In fact, let us draw everything in let us draw everything in the transistor level. We have an inverter first. this is the inverter this goes to the transmission gate. The transmission gate this is $\phi$ and then this is $\overline{\phi}$ and then this goes to one more inverter.

Let me draw a gate level diagram and here I am going to draw this thing the transistor level diagram and this is a weak inverter I am going to draw an inverter first and then talk about being weak. This will be the inverter and finally, it gets connected to the node X right. This is my node X and then it goes to the other inverter and so on.

This will be my Q signal. In this sense this is the input here let us say the input is 0 in the transparent mode that means, when the clock is 1, $\overline{clock} = 0$. Both this PMOS and NMOS will be on and if it is 0 here this will be 1 here at the output of the inverter and it is going

to drive the transmission gate. The current that will be there and then I will also draw this particular capacitance here some particular capacitances will be there.

The $C_X$ is going to get charged through this particular $V_{dd}$ rail because this is passing these 2 transistors are passing and the $V_{dd}$ is going to charged the $C_X$ node here. Whatever is the capacitance of the X node is going to get charged from this particular $V_{dd}$ rail because d = 0 that means, that this will be on and this will be off and this on transistor the PMOS on transistor as well as this particular both the transmission gates or transistor both the transistors, because the clock = 1 transparent mode both of them will be on and the $C_X$ node is going to get charged from this particular $V_{dd}$ rail. Let us say that previously your Q was 1, if it is 1 it will pass 1 and 0. Previously let us say it is one, this means that it is going to change from 1 to 0 because of this 0 and then 1 and this particular value will be 1 and then finally it will be 0.

But let us say that the previous stage it was 1, because it was previously 1 and now when the clock from $\phi$ to 1. During this particular initial portion of 1 of the clock that is when the d = 0 here alright. The previous state of the Q is the 1 here that means, that this particular NMOS transistor is on. The $C_X$ mode was completely what it was because this is 1 this was held to be 0 that means, it was held to be 0 means this particular mode is on, because this NMOS is on here previously, the NMOS is driving the X node to the ground whereas, because d = 0 now and this one will be 1. That means, that this PMOS transistor from here is going to charge the X node to high whereas, this particular transistor is going to make the X node discharge to ground.

The X node here has a contention that means, that there is one particular path charging path and there is another discharging path. That is the contention we are talking about and to avoid the contention whichever current is lower that is going to lose. That means, that whichever current is dominant that is going to win and ultimately X is going to favour the dominant current and we can do that by sizing this particular transistors more.

Let us say if I have a size of 10 here if I have a size of 10 here and if I have a size of 10 here and whereas, here if I make the size of 1 and 1 here. The width of this particular transistor is actually very very less than that of the size of the transistors here. The current that will be passing for charging the X node is actually more. It is actually 10 times more than that of the current that is passing of that is actually used for discharging the X node.

That is why I make this inverter as a weak inverter which will help in finally, making the X node pass the input here, if it is 0 it is 1 and then this one will be passed here. In the transparent mode we want this particular path to win over the feedback path. If I am using an weak inverter here and make weak inverter means the width of this particular tri state inverter to be less.

So, that the forward path not the feedback path the forward path is going to likely to win during the transparent mode. In the opaque mode this is the path is anyways off because the clock will be 0. This particular transmission gate will be off this particular transmission gate will be transistors will be off, the transmission gate itself will be off. There is no forward path the only path is the weak inverter which is nothing but the feedback path. Hope this is clear moving ahead.

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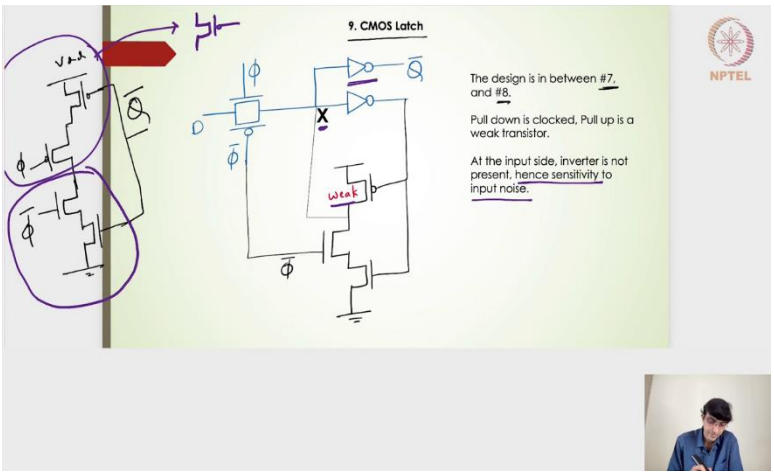


The one more variant of the CMOS latch instead of the weak inverter or instead of the tri state inverter it is a basically a combination of both. That this design is basically between the 7 and 8. Here if you notice that the pull up part is taken from the weak inverter and the pull down part is taken from the tri state inverter. If you notice the tri state inverter let me redraw that tri sate inverter. I am drawing the tri state inverter in the feedback path and just putting placing the transistors in a different way.

Let me complete this diagram alright. This is my $V_{dd}$ and this is my ground, this is the PMOS this is the PMOS, this is the NMOS and this is the NMOS. Notice that in the tri state inverter when in the feedback path if I had a tri state inverter or the design number 7

which we said that was the most recommended one. This one was coming from the output Q or whatever it the output $\overline{Q}$ in this case.

This two was coming from the clock. We said that this is $\overline{\phi}$ and this is $\phi$ because when the latch is in opaque mode that is when the $\overline{clock}$ will be fed to the NMOS and clock will be fed to the PMOS. What we have done is in this particular design the 9th design this particular portion of the pull downside is taken and for the pull up side it is nothing but the pull up of the weak inverter.

It is kind of the pull up side its nothing but a normal PMOS transistor, but it is a weak PMOS transistor, that is what is written here the weak PMOS transistor and the pull down side is taken from the tri state inverter. The advantage is instead of the 4 transistors or we have 3 transistors and the other advantage is with respect to the weak inverter is on the pull downside it is not weak anymore and there will not be any contention.

The moment the contention is there will be more delay to pull up or pull down the X node based on the input, because there is no contention on the pull downside because it is now clocked properly. During the forward path if at all the X has to go down rather go up here the X has to go up here. This particular path this particular pull down circuit is not going to pull down the X node it will easily go to the pull, it will easily go to a $V_{dd}$ level.

In that sense it has disadvantages or rather it has advantages. At the input side inverter is not present and sensitivity to the input noise. This particular portion we always had an inverter in the last 2 designs, that is taken away. If that is gone away then we will have its input noise sensitivity issues and that is what is this particular latch is having because the inverter is not there, but the output inverter is there.

It becomes insensitive to the output noise which is a good for the circuit, that is about this particular circuit 9 or the design number 9. We saw design number 7, we saw design number 8 and then design number 9.

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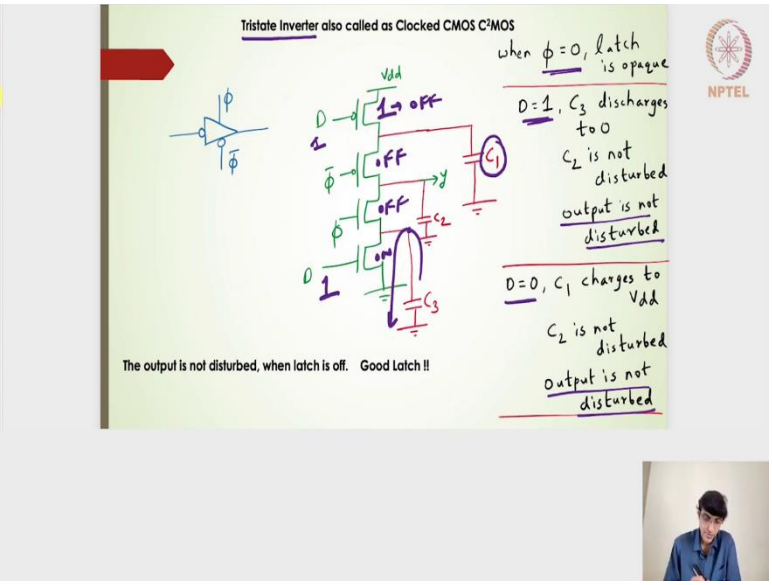


Let us take a look at the tri state inverter before going into the flipflop designs. The tri state is kind of symbolized in this particular way and its transistor level schematic is shown here where the D input is going to the D input or the Q input is going to the transistors closer to the $V_{dd}$ and ground rail. We have the clock given to the transistors which are closer to the output node. Let us draw a set of parasitic capacitances here just to notice what really happens.

The $C_1$, $C_2$ and $C_3$ are nothing but the diffusion or the merged or unmerged diffusion capacitances. Let us say that when $\phi = 0$ that is in the latch is opaque it is not in the transparent mode that is when this one will be working. What happens if the $\phi = 0$ in this particular case if $\phi = 0$ this one will be off and this one will be off. When the $\phi = 0$ that means, $\phi$ 1 = 1. The PMOS will be off and let us say that the input changes.

If the input changes here. What we really do not want is if this is off or the $\phi$ is 0 that means, the output node should not change at all right. But because these 2 clocks are 0 and this will be 1. These 2 transistors will be off and if D changes from d changes to 1 here that means, that D means D will be one. So, that will give us this 1 represents that this will be off and then this 1 will represent this will be on.

Now I have the $C_3$ can get completely discharged to the ground, but the $C_2$ because this is an off transistor the $C_2$ which is connected to the output node does not drop at all because this is not at all y node is not at all connected to the c three node. Then similarly if I make

d = 0 here this will become turn on the PMOS transistor and $C_1$ will get completely charged to $V_{dd}$.

But output node is not getting disturbed because this particular clock has ensured that the PMOS transistor is off. The output does not get disturbed at all in this particular case and that is why it is a very good design. Normally the clocks in a tri state inverter the clocks are given to the transistors the clocks in the sense clock and $\overline{clock}$ are provided or fed to the transistors which are closer to the output node. The input is given to the transistors which are closer to the $V_{dd}$ and ground rail.

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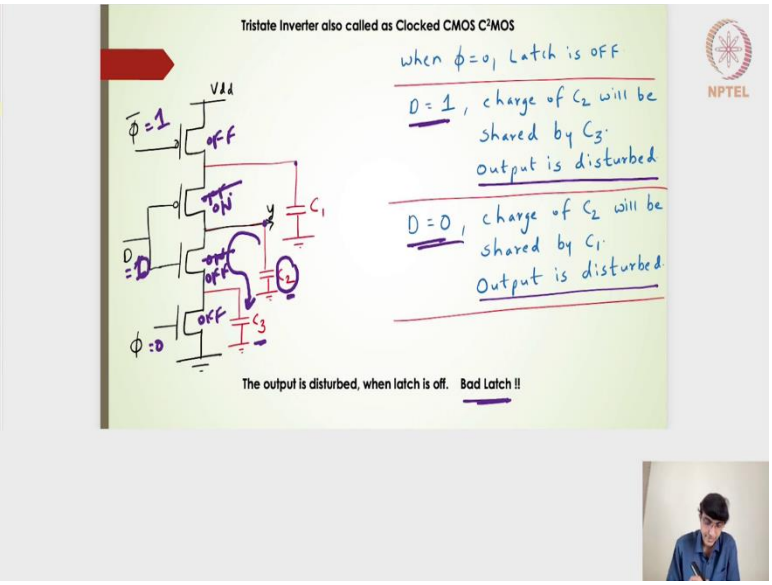


If I actually take a different design where the clocks are connected to the transistors closer to the rail $V_{dd}$ and ground rail and input is given to the transistors closer to the output node, the input are given to the inner transistors. The output are given to the outermost transistors the clock are fed to the outermost transistors. In that case what really happens if $\phi = 0$ that means, it is in the opaque board. The $\phi = 0$ represents, this is off and $\overline{\phi} = 1$ which will be nothing but this will be off.

Now, if d = 1 here and D = 1 here that means, that this will be on and of course, this will be off here, but this on transistor will ensure that whatever is a node voltage initially let us say it is connected to $V_{dd}$. Now this the charge from $C_2$ will be shared to the $C_3$ capacitance although this transistor is off, but $C_3$ is kind of connected to the $C_2$ capacitance via this

particular on transistor. Thereby the $C_2$ and $C_3$ are going to share the charge and thereby the output node voltage level is going to get dropped.

In this sense the output the level is kind of disturbed. The other problem is if D = 0 here D = 0 represents this will turn on alright. If this is made 0, this will be on and this will be off. This on transistor is now making $C_2$ and $C_1$ kind of connected by the transistor and if it was $C_2$ was $V_{dd}$ at $V_{dd}$ level then it is going to charge to $C_1$ or if it was at 0 voltage level and $C_1$ had some particular amount of voltage across it then this $C_1$ is going to share the charge to the $C_2$ and thereby the output node voltage is likely to change.

The charge of $C_2$ is going to be shared by $C_1$ now and that is why the output is disturbed. This is a very bad latch design or rather the tri state inverter if at all we were to use it in the CMOS latch in the feedback path this design becomes a very bad contribution to the design. Normally when we design the latch or when we use the tri state inverter into the feedback path of the latch the clocks are provided to the innermost transistors that is the transistors closer to the output node. The inputs are given to the transistors which are closer to the rail voltages. Hope this is clear.

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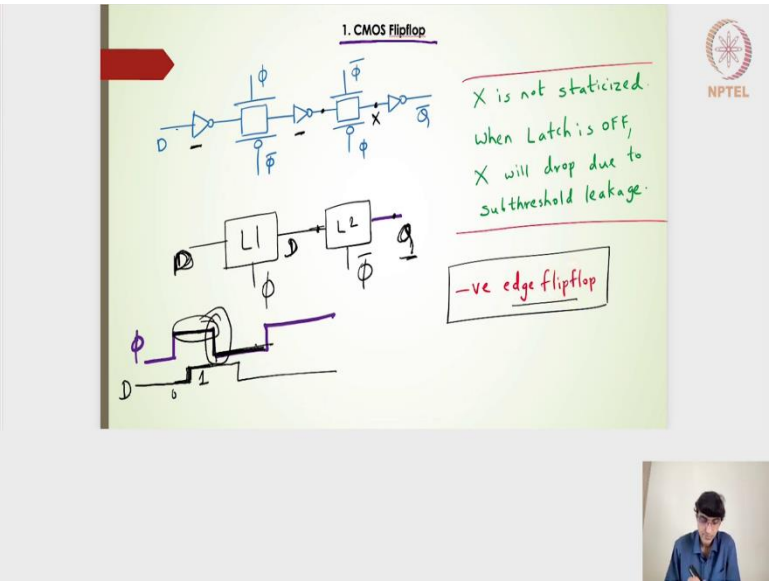


Moving ahead let us introduce to the CMOS flipflop as we know flipflop is made up of two latches L1 and L2. If I have a clock here of a high level and then followed by a low level of clock then this behaves like the flipflop. Whatever is the input that has been

provided. Let me draw the simple timing diagram. If this is the clock here and let me take the input somewhere here.

Let us say this is the input here. D is my input for the first latch L1. This D is going to pass as the output of the latch you know latch L1 during the high level of the clock. During this particular level of the clock whatever is the D here will get passed. At the output of the latch 1 and it has to wait for the latch 2 to become active and the latch 2 will become active only during the negative level of the clock.

Whatever it has passed from 0 to 1 in this case 1 will be it has to wait till the negative level of the clock has reached because that is when the L2 is going to pass the signal from the input to the output. The input to the output is passed from positive level to the negative level, that is during this particular transition of the positive to the negative level that is when the input from here this portion of the input of the first latch will be passed to the input to the output of the second latch.

This works like a flipflop because flipflop is operating only on the clock edges. Just use the latch design and then derive the flipflop design it is very simple. We use the very basic CMOS latch design where we have the inverter here and inverter here inverter here and inverter here at the outputs of the latch design helps in making the circuit more insensitive to the input and output noise. We have the transmission gates here which is going to pass the input to the output based on the clock level.

This clock level is high that is when it is passing the D to this particular portion and we have another transmission gate which is operating at $\overline{\Phi}$. That is when the clock level is low. This particular input to this particular second latch will be passed to the output of this particular transmission gate. Again, that this design has problems, the X is not staticized.

There is a possibility of the X getting discharged due to the sub threshold leakage current, it is not staticized that means, that it is a dynamic mode it is in a dynamic state or it is in a floating node voltage. It can drop due to the sub threshold leakage current and this works like a negative edge flipflop because negative edge means the decreasing edge or the falling edge of the clock we can say that and this negative edge because it gives the output at the negative edge of the clock that is when the transition is falling from the clock from high to low that is when it is going to give the output and that is why it is called as a negative edge flipflop.

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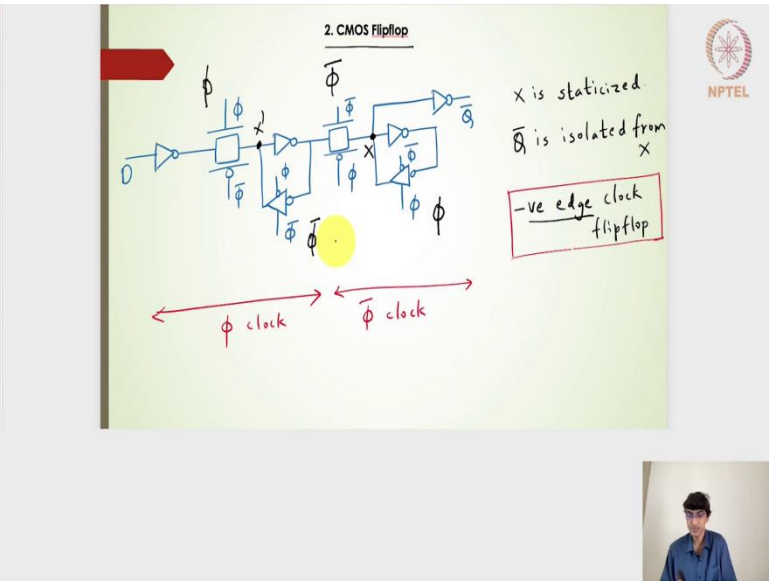


Just to make it more robust design just as we had done for the CMOS latch we are introducing the feedback path or the tri state inverter in the feedback path to ensure that this particular node and then the X node here as well as the X dash node here is staticized. Very similar to the latch design what we are doing is we are bringing in the tri state inverter here to ensure that this X node.

Although there will be a sub threshold leakage current this the moment it drops little bit there will be a charging back from this tri state inverter or if it is getting charged due to the sub threshold leakage current. It will ensure that this has a stronger discharging part connected to the ground. Similarly on the X node also, X is now staticized and then of course, there is the inverter at the input side and the inverter at the output side making sure that the $\overline{Q}$ is isolated from X.

Whatever is the output noise here does not get coupled into the X and whatever is the noise at the input side does not get coupled into the into this particular path. A $\overline{Q}$ is isolated from X and of course, it is a negative edge because I have this latch design is working as a transparent mode when the clock is high and this particular transmission gate is or this particular latch design works when the clock is low and that is why it is said that this is the latch of positive clock and this is the latch of a negative clock and thereby it works like a negative edge flipflop.

Notice that this tri state inverters as supposed to know as we have seen in the CMOS latch design the tri state inverter here if it gets clocked this clock of the tri state inverter has to be opposite to that of the transmission gate. For this particular latch we know that the clock is $\phi$. The tri state inverter should work in the $\overline{\phi}$ mode that is in the opaque mode and transparent mode this particular transmission gate will pass the signal in the lower level of the clock this particular feedback path is going to pass the signal.

Whereas, for this particular latch it is working in the $\overline{\phi}$ mode, the tri state inverter here should work in the $\phi$ clock the positive level of the clock and because this particular latch is transparent during the low level of the clock. Thereby the feedback mode or the feedback path should work in the positive level of the clock, that is the additions which we have done in this particular CMOS flipflop design.