Design and Analysis of VLSI Subsystems
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Lecture - 72
Introduction to CMOS Latch design

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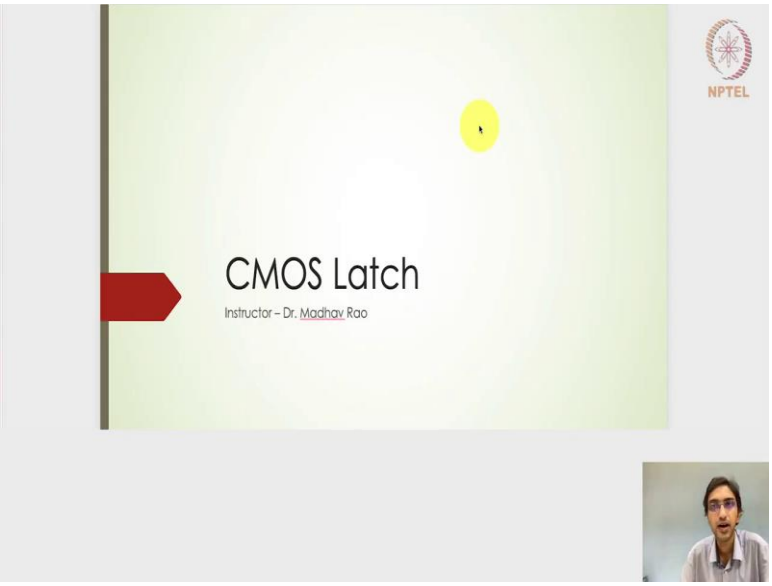

Hello students, welcome to this lecture on the sequential circuits. The sequential circuits as such is very important for the subsystem design for the VLSI subsystem design in the sense that we normally have some component of the sequential circuits, interface to the combinational circuit.

While we actually design the combinational circuit to reduce the delay, to improve the power and then the footprint the timing parameters is mostly dependent on the sequential design which we choose. Let us say that, if we choose the latch design or a flip flop design. The combinational circuit has to be designed in such a way that it does not violate the setup and the whole time of the sequential circuit which is there in the subsequent stage.

In that sense I think the sequential design is kind of very important for designing the overall subsystem. For example, if I am doing an adder circuit, the adder circuits output has to go to the another combinational circuit, but it has to be timed. In that sense I will have to introduce a flip flop or a latch element in between the two combinational circuits.

While I am designing the combinational circuit or while I am designing the adder circuit in this case, we have to ensure that it does not violate the subsequent the sequential element such as the latch or the flip flop which is there to interface to the other combinatorial circuit.

In generally in today's VLSI design or today's digital circuit VLSI design we will see lot of sequential elements just to time it out. To make sure that the combinatorial the combinational circuits output are well timed and it is kind of reached to the next combinatorial circuit in a proper synchronous timed manner.

In this particular lecture what we are going to do is, we will try to understand the basic, the most primitive sequential element and that to the latch design we will try to understand how the latch design has evolved from the basic the CMOS circuits. Starting from the pass transistor going to the transmission gate and then some variant of the transmission gate, that we will get a most robust the latch design.

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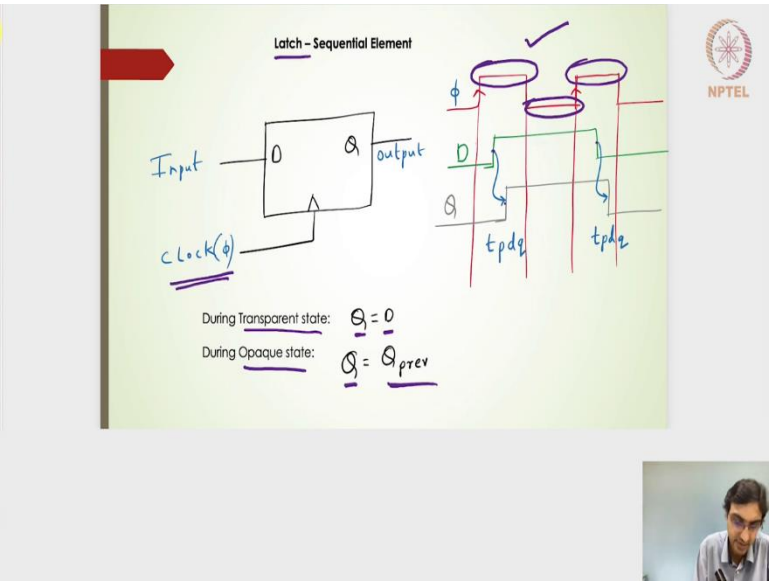

Moving ahead, as we understand from the latch definition. Now let me also pick up my pointer here, as we understand that latch is a sequential element and then by definition what we really want is, for a latch design and then this is a block diagram of a latch design where I have the input D and then the output Q.

$$Q = D \text{ in a transparent mode}$$

$$Q = Qprev \text{ in an opaque mode}$$

Actually the latch is defined in the transparent state it is defined in two states one is the transparent state and one is the opaque state. The latch is actually working in two different states transparent and opaque state. During the transparent state the output will follow the input whatever changes happens in the input or whatever is the input level we will get the output.

In an opaque state at the trans the output does not follow the input. The output will be nothing but the previous output state and this particular transparent state and opaque state are actually defined by the clock signal which is applied to the latch chip. This is the very simple primitive definition of the latch. The input and output are given with the clock. If I have a clock in this particular, this is basically the timing diagram of the latch design. If I have a clock here, and for a latch it is always defined by the clock levels. In this case I have considered the high level of the clock, the high level of the clock here.

Only during this particular high level of the clock the latch is in a transparent mode or in a transparent state that means, the output will follow whatever the changes happens in the input side. During this particular the negative clock cycle, it will be in opaque state that means, that the output will not follow the input levels or the input changes, but it will retain in the previous state.

Here in this particular timing diagram, if the input is applied like this as shown in the D signal and the output will follow the input during the high level of the clock, during the high level of the clock whatever is the input level the output will follow. Of course, there will be some kind of a delay there will be some kind of a propagation delay in this case the output is arising.

It will be the propagation delay from D to Q and it should be the rising one. And here the output will follow the input, of course with some delay and then this particular delay is defined as propagation delay D to Q and it is falling. It should be and f labeling should be there, t_{pdq} which is nothing, but the propagation delay from D to Q.

This is how the timing diagram defines the latch. Most importantly to summarize the latch design what we really need to design for achieving the latch as a sequential element is, there should be two modes the transparent mode and then the opaque mode. Transparent

mode the output should follow the input of course, with some delay. During the opaque state whenever the clock is at a low level, it should work like an opaque state where the output should not follow the input and the output should retain the previous state.

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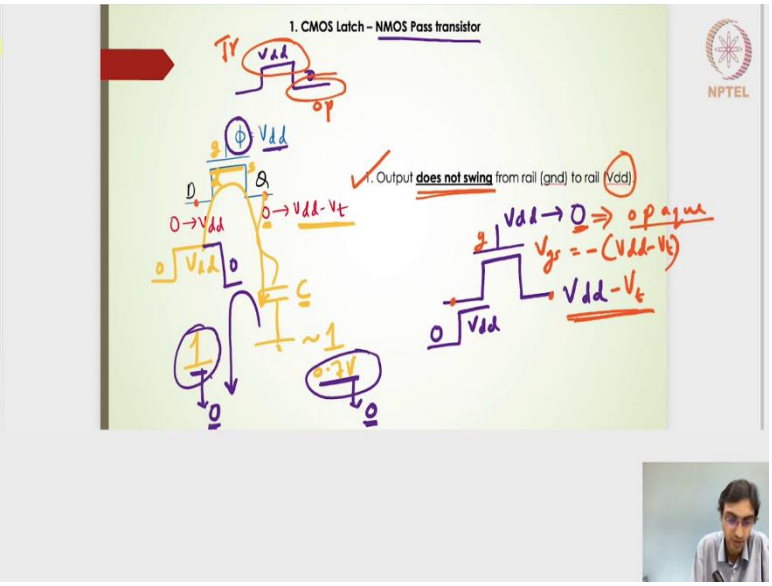

With those definitions or with those specifications of designing the CMOS latch, let us try to understand whether the NMOS pass transistor as an very simple primitive single transistor can it work like a latch. Let us say this is the NMOS transistor with the gate, the gate is given to the clock, the clock is applied to the gate.

If I have a V_{dd} level and then a 0 level V_{dd} and then a 0 level, applied to the clock. This particular level we will have it as a transparent mode and at this particular level the low level of the clock we will have it as a transfer we will have it as an opaque mode. This will be opaque and this will be the transparent mode. Whenever the clock or especially the gate is applied with a V_{dd} level, we will have it as a transparent mode and then whenever the gate is configured to the low level of the voltage we will have it as an opaque state.

Now, let us try to understand during this particular two different voltage levels applied to the gate, whether it behaves like the latch. Let us say this is the input and the D signal is given here to one of the diffusions of the pass transistor. What happens to the output? let me also draw the capacitance at the output side just to understand its effect. The capacitor let us say that initially it is not at all charged.

In initial charge is 0, and we apply a any step input of 0 to V_{dd} at this side. The logic one is applied. In that sense this is anyways the gate and then this is having a 0 voltage. It will work like a source, it will act like a source drain, and then this one should work act like a drain terminal alright it is having a higher potential.

In that sense V_{gs} value is actually $V_{dd} - 0$, initially the capacitor is having a charge of 0. We will have V_{gs} as V_{dd}, it will have a channel here. This particular channel because this $V_{dd} - 0 > V_t$. This particular channel will ensure that there is a charging path from the V_{dd} to the capacitance.

A normal working of the pass transistor. Now this charger still it reaches $V_{dd} - V_t$ beyond that this $V_{gs} < V_t$ and thereby this channel will not be there and no more there will be a charging path. The capacitor here which is at the output node here charges still $V_{dd} - V_t$. Applying a logic level of 1 here at the output, I will get close to 1 not really 1, but it will be 0.7 volts if I consider $V_{dd} = 1V$ and $V_t = 0.3V$. A logic level of 1 is giving me a 0.7 volts here. If I then change apply the step input make it back to 0 here, then this capacitor will have the charging path as a you know as a normal pass transistor NMOS pass transistor working, this capacitor will now actually discharge to 0.

If I change this from 1 to 0 here this will change from 0.7 to 0 volts. Whenever the gate is at set at V_{dd}, its transparent mode working of this particular the PMOS or the NMOS transistor it is working perfectly well whenever the gate is at a high level, the output will follow the input, especially when it is at 0 logic we will getting the 0 logic here at the output whenever it is 1 logic we will get 0.7 volts at the output.

Now, let us say that I have this pass transistor and let us say it is at V_{dd}. I have applied 0 to V_{dd} here the step input. The capacitor here will get charged to V_{dd} and after that the gate voltage is exchanged to 0 volts. That means, now it should be in an opaque mode; that means, that the output should not change.

When it does change to 0 here the V_{gs} value. In fact, the output will be $V_{dd} - V_t$. The $V_{gs} = -(V_{dd} - V_t)$ suddenly when the clock is applied when the gate voltage is sees a 0 volts here, it will be in a cut off mode this transistor will be in the cutoff and whatever the channel it was it had been formed earlier to charge this particular output node it will disappear.

The output voltage will be retained at $V_{dd} - V_t$ because it does not have a discharging path or it does not have a charging path anymore, because the gate voltage now sees the voltage of 0 and thereby it is in opaque mode. This particular a very simple pass transistor an NMOS pass transistor is behaving like a latch, because it satisfies both the transparent mode operation as well as the opaque state operation.

The NMOS pass transistor it works like a latch provided if the gate voltage is given the clock signal and the input is applied to one particular diffusion side and the output should be taken from the other diffusion terminal. In that sense the NMOS pass transistor works like the latch whatever we need, but there are some disadvantages and let us have a look at the disadvantages.

The first disadvantage is output does not swing from rail to rail. The output whenever it reaches to 0 perfectly, because the NMOS pass transistor passes a successful 0, but when the input is at V_{dd} it actually reaches to 0.7 volts or $V_{dd} - V_t$. It does not pass a successful logic level 1. It is passing a very weak logic level. That is what is one of the disadvantages, it does not know the output does not swing from rail to rail, it actually swings from ground to $V_{dd} - V_t$.

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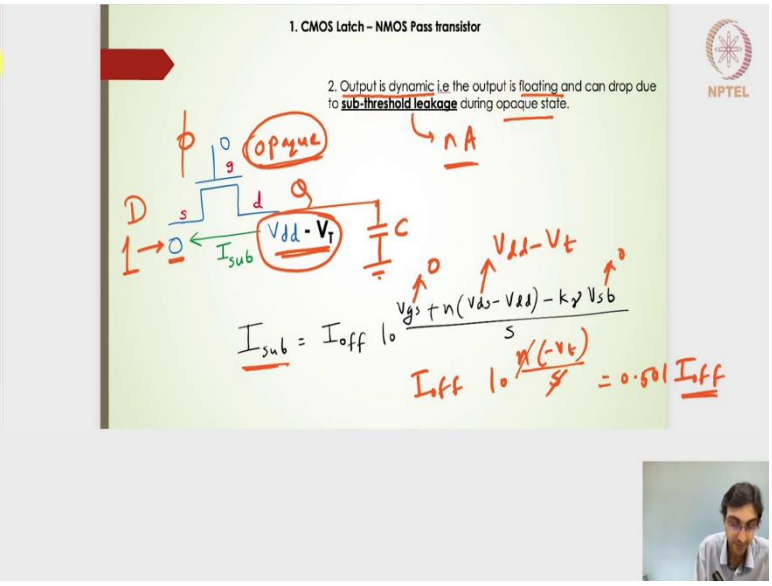

Hope this is clear. The second disadvantage is the output is dynamic that means, that this particular output node if I consider as a capacitor it is let us say it is charged to $V_{dd} - V_t$ alright. Now the gate is fed with a 0 volts that means, it should be in a opaque mode, it

should be in a locking state. The output it reaches to $V_{dd} - V_t$ and it is should retain at $V_{dd} - V_t$.

Let us say there are some changes at the input here. Input from 1 it has gone to 0, even if there is some change at the input side in the opaque state when the gate voltage or the clock voltage is 0 at a 0 level, we should not have any changes at the output. Let us say this is the input and then this is the clock. The clock is at 0 means it is in a opaque state that means, the output should be retained irrespective of the changes at the input.

Even if the input changes here the output should not change, but rather what happens is due to the sub threshold leakage current which will be in terms of nano amperes. The sub threshold leakage current because the 0 volts applied at the gate side falls into the sub threshold region that is below the V_t. We know that there will be some kind of a leakage current that will be and that is possible from drain to source side.

Although it will be nano amperes there will be a small amount of current that will be going back from drain to source. There will be a drop in $V_{dd} - V_t$ voltage, there is a possibility of a drop of the voltage at $V_{dd} - V_t$. We know that the sub threshold leakage current which is defined by this particular expression. When V_{gs} is even if it is a $V_{gs} = 0V$ here, I have a $V_{ds} = V_{dd} - V_t$.

Even if we say that V_{sb} the source is at 0 the body is at 0 if this is 0 here, we will still get,

$$I_{sub} = I_{off} 10^{\eta(-V_t)/S}$$

Where, η = 0.1 and S = 0.1,

$$I_{sub} = 0.501 I_{off}$$

The I_{off} current is generally around 5.63nA for a NMOS transistor. We are likely to get somewhere around 2.51nA, but still there will be a some amount of the leakage current and if this opaque state remains for a longer duration even the small sub threshold leakage current is likely to have a greater drop in the output voltage.

That is the problem. I cannot actually have the opaque state for a longer duration. That the output should be retained, but it does not get retained and there will be a drop in the output voltage, because of this sub threshold leakage current. That is the reason why it is called

as the dynamic, the output is floating. The output remains floating and can drop due to the sub threshold leakage current during the opaque state.

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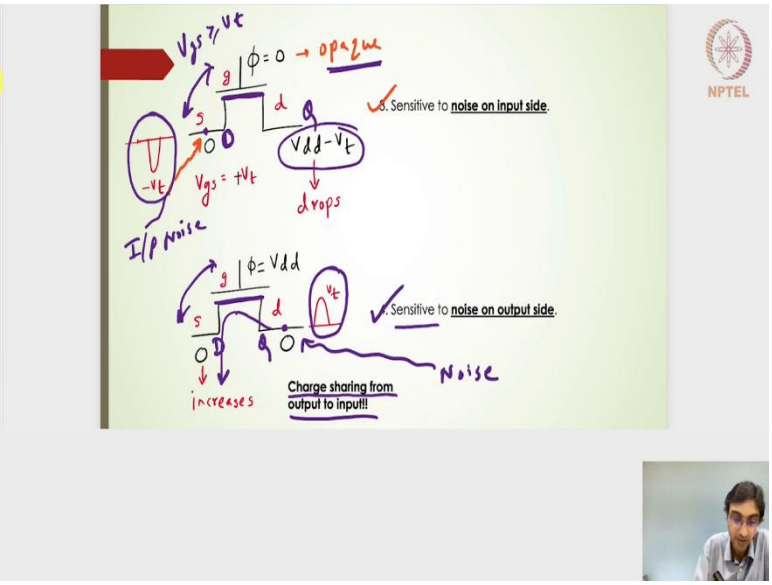

The third disadvantage it is actually sensitive to the noise on the input side alright. What it really means is, let us say that I have an NMOS transistor and then we are using this NMOS transistor for the latch design. Let us say that these are the output states and the input states which it has been reached.

The output state it has been reached is $V_{dd} - V_t$ and then the clock signal has gone to the 0 level. That means, that we should be the latch should be in opaque state. The $V_{dd} - V_t$ should not change now irrespective of the changes at the input side. Let us say the input has changed to 0 and we notice that of course, there will be some kind of a sub threshold leakage current which will make this drop.

But irrespective of the sub threshold leakage current, let us say that at the input side there is an in noise signal, there is a noise signal which get which gets coupled to this input side input of the NMOS transistor. Let me say that this is an input noise. The input noise is of the level of $-V_t$. Let us say that I have a big signal circuit and then close to that and the big signal circuit is then very close to the digital circuit, where the digital circuit has this latch design and we have used the NMOS transistor for designing the latch.

In that case I will have some kind of a coupling effect. The coupling effect is going to have a $-V_t$ voltage this kind of a signal, that will be coupled at the input of this latch and then let us say this is the output. A coupling with the noise coupling at the input here D and if it has a $-V_t$ here or greater than $-V_t$, then I have this V_{gs} value going to be equal to or greater than V_t.

This particular voltage $V_{gs} \geq V_t$ based on this noise signal if it is $-V_t$ or more than $-V_t$ in the sense the magnitude is more than the V_t value. Then in that sense I have this $V_{gs} \geq V_t$. This particular transistor although it was supposed to be in opaque it will be now be on that means, there is a channel that has been created here, the channel allows the further drop of the output voltage.

The output voltage is not retain to $V_{dd} - V_t$ anymore and it gets dropped further. That is why it has been said that it is sensitive to the noise on the input side. The other disadvantage is it is sensitive to the noise on the output side as well, and the reason is very simple if I have it in the transparent state let us say that it has read 0 and it has reach the input was 0 and then the output was 0 and then the clock is at a higher level, it is in a transparent mode. Whatever is the input here will go to the output here, but then at the let us say that this particular the output line of this particular latch is very very close closely coupled to any other circuit and that particular circuit is having an input, having a noise that has been coupled at the output side.

Let us say that the noise is characterized like a positive V_t here. This particular positive V_t here will have an effect on the change in the input side. Let us say that all these values are 0 and 0, but then there is a noise signal of V_t here and $V_{gs} = V_d$. There is always a channel that has been formed in the transparent mode in the transparent state of the Dl of the D latch. This particular transparent the channel here allows any kind of voltage that has been applied at the output side to be shared at the input side.

What happens is if suppose a voltage of V_t comes here the V_t here will get sufficiently discharged to the 0 value here. The V_t it will decrease to $V_t/2$ on this particular side and then $V_t/2$ on this particular side assuming the capacitors on both the sides.

Then there will be a charge sharing effect from the output to the input. Then the charge sharing will have an immediate effect in the output levels. Instead of 0 it will now be

considered as $V_t/2$ on the output side and it will have an impact on the input side as well. It is kind of sensitive to the noise on the output side as well. Hope this is clear. We had four disadvantages of using the NMOS transistor as a latch although the NMOS transistor can be utilized as a latch.

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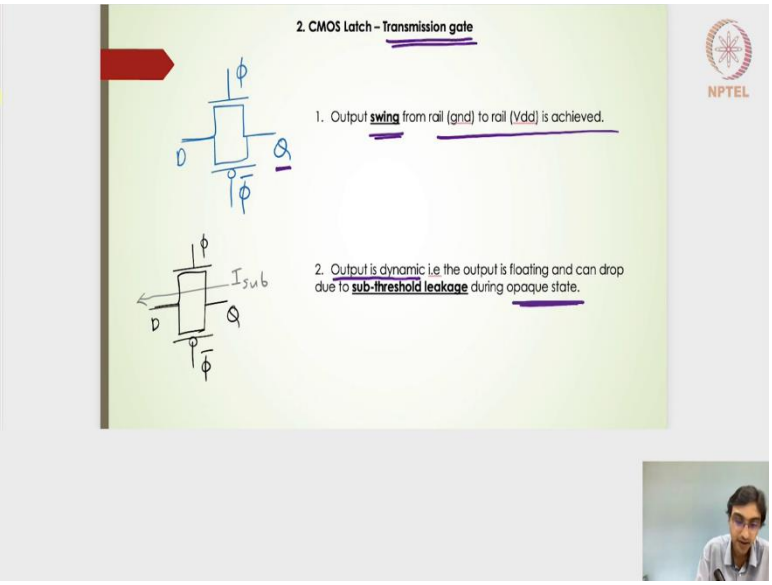

Let us see what happens if I use the transmission gate. If I have a transmission gate that means, that the NMOS and the PMOS transistors are tied together in parallel. One thing is very clear that the output swing is not restricted to $V_{dd} - V_t$ anymore it gives the output swing from 0 to V_{dd}, because either of the PMOS and the NMOS will ensure that will give a successful logic 1 and pass a successful logic 1 or a pass a successful logic 0. I will get a rail to rail voltage is achieved. That first disadvantages is kind of removed by using a transmission gate as a CMOS latch. The second one of the output being dynamic and that is output being floating and due to the sub threshold leakage current it can actually get dropped that still retains, especially during the opaque state that is still remaining in the transmission gate.

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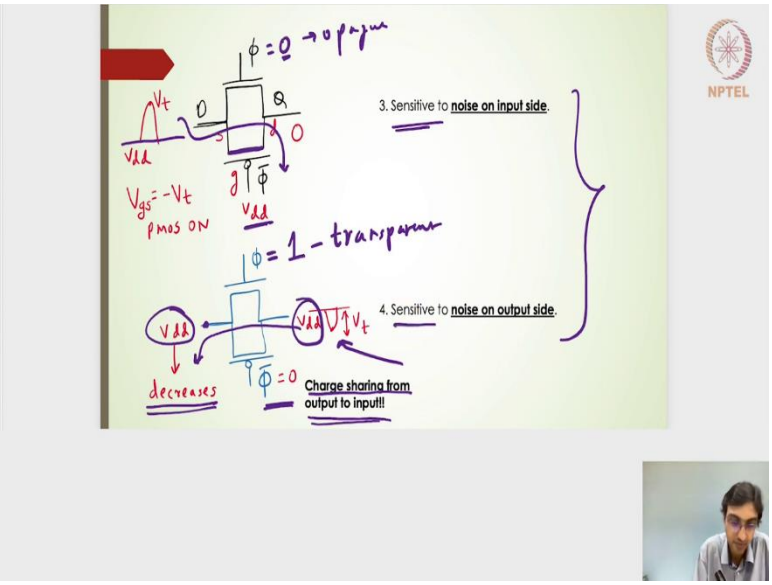

The third and fourth the sensitivity to the noise on the input side as well as on the output side are also retained here in the transmission gates, and we can see one such example here. In the last slide last to last slide especially when we talked about the NMOS transistor here I am going to talk about the PMOS transistor, how is it sensitive to the input noise.

Let us say that the ϕ is 0 that means, it is in opaque mode. In the transmission gate if the NMOS gate is 0, the PMOS gate will be nothing but the complement of 0. It will be its logic level high or the V_{dd} voltage and let us say that the output is now maintained at 0. In the previous state when it was in a transparent mode the output is completely discharged to 0. This particular logic level of 0 is been achieved in the previous transmit transparent state. Let us say that now the input has changed to V_{dd} here, and there is a noise signal that has been coupled at the input side with a noise signal of V_t and above V_t this $V_{gs} = -V_t$ or lower than $-V_t$ will make sure that the PMOS transistor will have a channel here.

With this particular channel we will have some kind of the charge sharing from the input to the output side. That is the reason why the output is kind of very very sensitive to the noise on the input side. That is still remaining the fourth disadvantage of sensitive to the noise on the output side I will take an example here again. Let us say that the ϕ=1, it is in a transparent mode. Whatever is the input the output is going to get reflected and because it is a transmission gate $\overline{\phi}$ =0.

Let us say that it applies at the input side it is 1 logic and then the output has achieved a logic of 1. At the output side if it is coupled with a noise signal of V_t or $<V_t$, then in that case there will be a drop at the input side, this gets coupled into the input side. The input voltage if the other parts of the input voltage does not drive this particular node, then this particular node is now has a possibility of getting it decreased.

Due to the charge sharing from the output to the input, the output the changes or the noise at the output is going to have an effect on the input side. In that sense it is sensitive to the noise on the output side, as well as the noise on the input side and then the second disadvantage which is still there in the transmission gate while we are using the transmission gate as the latch design is due to the sub threshold leakage current, the output node is dynamic and it remains to be floating and there could be a drop in the output voltage due to the sub threshold leakage current.

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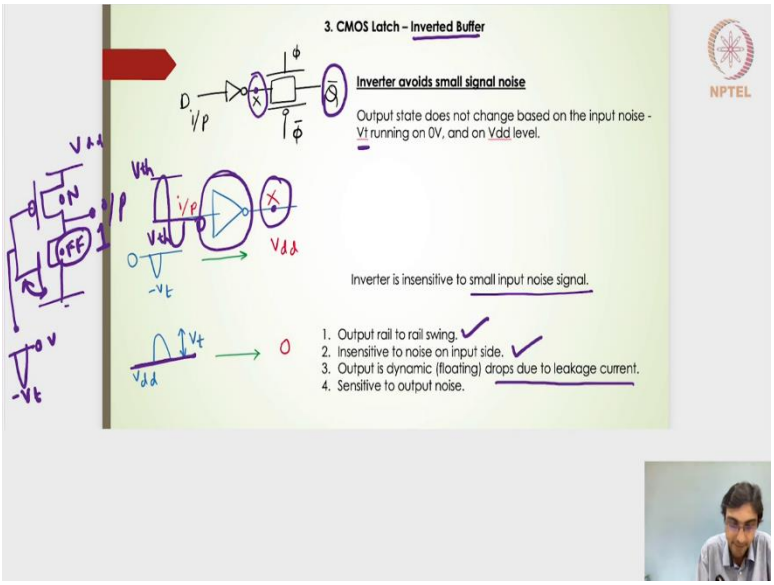

Now, how do we solve this? we need to solve this so that we will get a very robust latch design. Let us say that can we use the inverted transmission gate or an inverted buffer design. Inverted buffer design means, I will have an inverter first and then followed by the transmission gates. The transmission gates with the clock at the gate side, ϕ and $\overline{\phi}$ given to the gate of the NMOS and PMOS transistor respectively, and the input is applied to the inverter. I will actually get a complemented latch output.

Let us say that for time being it is perfectly fine I do not really care about getting a complimented or an un complemented logic. If D = 1 the $\overline{Q}$ = 0 and if D = 0 the $\overline{Q}$ = 1 in a transparent mode. By definition the opaque mode whenever the clock is at low level the $\overline{Q}$ should be retained whatever was the $\overline{Q}$ in the previous high level of the clock it should be retained, because of the transmission gate we know that the output will swing from rail to rail voltage 0 to V_{dd}.

Let us say that the output state does not change based on the input noise V_t running on 0. This particular inverter will ensure that even if I have a noise signal here on the input side as was there in the previous case it is not going to affect the output of the inverter and if the it does not get affected at the X node it will not have any effect on the $\overline{Q}$ signal or the $\overline{Q}$ output which is nothing but the output of the CMOS latch. Let us try to see what the inverter how the inverter makes that difference. Let us say that I have an inverter here at the input and then this is the X. This is the D signal and this is the X signal. The x will go to the transmission gate and then give the $\overline{Q}$ signal.

As previously if I have a $-V_t$ or below $-V_t$ here, because of this transmission gate which is directly taken as the input we used to get the NMOS transistor to be on, because this was said to be 0 and in the opaque state even in the opaque state if the input noise was going below $-V_t$ like my $V_{gs} < V_t$ and then this particular NMOS transistor was turned on and thereby the output might have a change based on the input signal.

In this particular case even if it reaches minus V_t because of the inverter here if I draw the inverter transistor, the V_{dd} and then I have a PMOS and then NMOS and then this is my output. This is my input signal even if the signal goes below -V_t here the NMOS either of this this was anyways on and this was off initially also even when it was 0 volts, and then the output was anyways turn to 1.

Even if it goes to $-V_t$ here this will still remain off, because my V_{gs} value will be negative not only 0, but it is now negative and this negative value will not have any effect on the change in the operations of the NMOS. The NMOS will still be off and then there will be no change in the output, there will be no change in the X value, no change in the $\overline{Q}$ value. Similarly, as was previously seen if I have a noise signal above the V_{dd} then in that case it will not have any effect on the X output voltage, because when it was at V_{dd} we will anyways have the PMOS to be off and then the NMOS to be on and then the output voltage

will be pulled to 0 and a greater voltage than the V_{dd} of V_t with a value of V_t it will not have any effect. The PMOS will still be off and then the NMOS will still be on.

The noise signal on this particular inverter will have an effect only if I get whatever is the input here whether 0 or V_{dd} if it has, if it goes above V_{th} of the inverter whatever is the if the inverter is a skewed inverter if it is an unskewed inverter we know that the threshold voltage of the inverter was around 0.5. If it is the noise signal is above 0.5 the noise signal is below 0.5 for the V_{dd} rail or it is above V_{th} for the 0 voltage level then only this X value will change. Any small level or a small low level noise signals will not have any effect on the inverter side and that is the reason this inverter is going to avoid the small signal noise especially at the input side.

Inverter is insensitive to the small input noise signal, it reaches that because of the transmission gate the output rail-to-rail swing is achieved insensitive to the noise on the input side because of this particular inverter and output still is dynamic floating and it can drop due to the leakage current alright.

Now, one can consider that we have an inverter here, and we have an inverter here and that is going to be driven by either the V_{dd} rail or the ground rail. This X is kind of a driven one. Now, why will the output here of the transmission gate or the latch is going to have a drop or an effect because the X value is anyways driven by the rail voltages. The reason one such case I can give is, let me pick a new slide.

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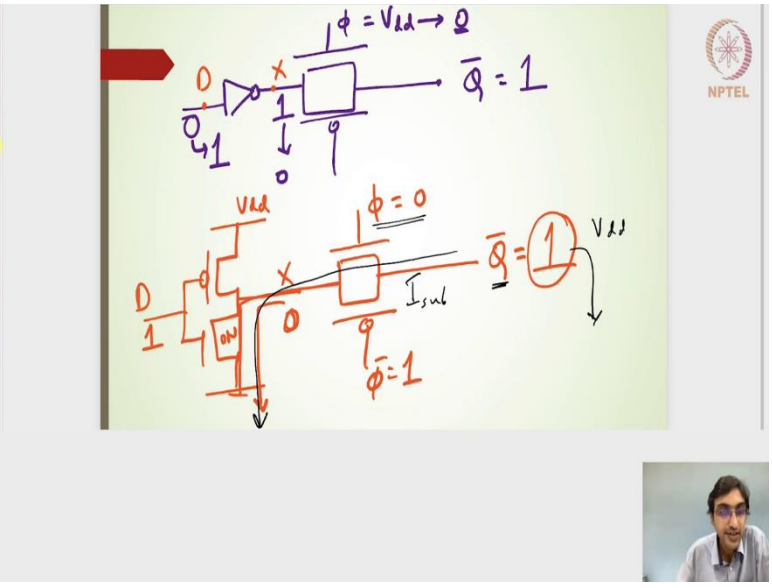

What we have is the inverter followed by the transmission gate and then this is my output signal. Let us say that the output signal in the previous clock cycle has reached 1. This has to be 1 and this has to be 0 in the previous clock cycle this gate voltage was V_{dd} or 1 and now it has gone to the opaque state of 0.

Once it has reached the opaque state of 0, let us say that there is a change in the input from 0 to 1 and then it has reached to 0. If I draw this particular transistor level diagram for the inverter. I will have a V_{dd} here, I will have a ground here, it is now 1 here and that is why this particular I will call this as an X node and this is $\overline{Q}$ and then this is D. I will have a D signal as 1. The X signal is now completely discharged to 0 and then we have this transmission gate. The transmission gate clock or the gate voltage is set to 0 and then $\overline{\Phi}$ will be nothing but 1. Then I will have this output of this latch or the transmission gate which should be retained at the logic level of 1, but because this goes to 0 or rather this particular node voltage is actually driven by this NMOS transistor which is on now alright.

The sub threshold leakage and if it is kept opaque or if it is trying to retain the logic level one for a longer duration, the sub threshold leakage current which will flow towards the ground will slowly keep dropping this voltage values from V_{dd} to a lower value, even in an opaque state because of this sub threshold leakage channel, that there will be a change in the output voltage, if it is maintained for a longer duration. Hope this is clear.

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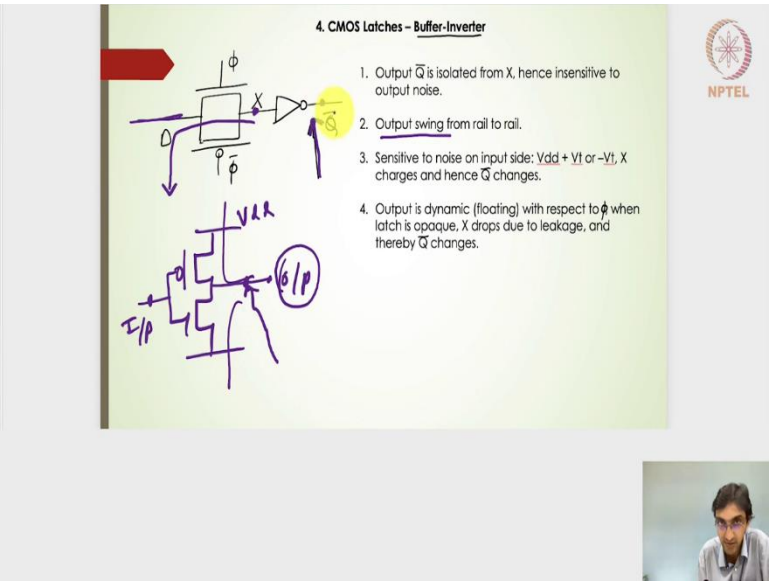

Adding an inverter at the input it makes it insensitive to the input noise signal. Similarly, if I have this is another variant of the CMOS latch. The earlier one was an inverter followed by the transmission gate, here it is a transmission gate followed by the inverter or a buffer followed by the inverter.

There is no inverter at the input side, the inverter is there at the output side. What it does is the output $\overline{Q}$ is now this particular signal is now isolated from the X and what it does is, even if I have a noise signal here if I have a noise coupled at the output signal it will not have any effect on the X input.

Now, it is very simple because if I consider the inverter and then the output here, and then the input here right any kind of the noise that has been coupled in the input will not have any effect on the input signal, because output signal is anyways driven by the V_{dd} or by the ground. Any noise input signal at the output side will not have any effect in the input side.

This inverter is making sure that the output noise signal is not captured into the latch design because is the transmission gate is there the output swings from rail to rail. Then the output is still dynamic the reason is if this is kept for a long duration in the opaque state there will be a drop due to the sub threshold leakage current drop in the X node voltage and will have an effect on the $\overline{Q}$ output signal.

Lastly it is still sensitive to the noise on the input signal. If I have a some kind of an input noise here, which can get reflected with the X node and then this X node changes in the X node will have an effect on the $\overline{Q}$ signal.