Design and Analysis of VLSI Subsystems
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Lecture - 71
Estimating Static Power

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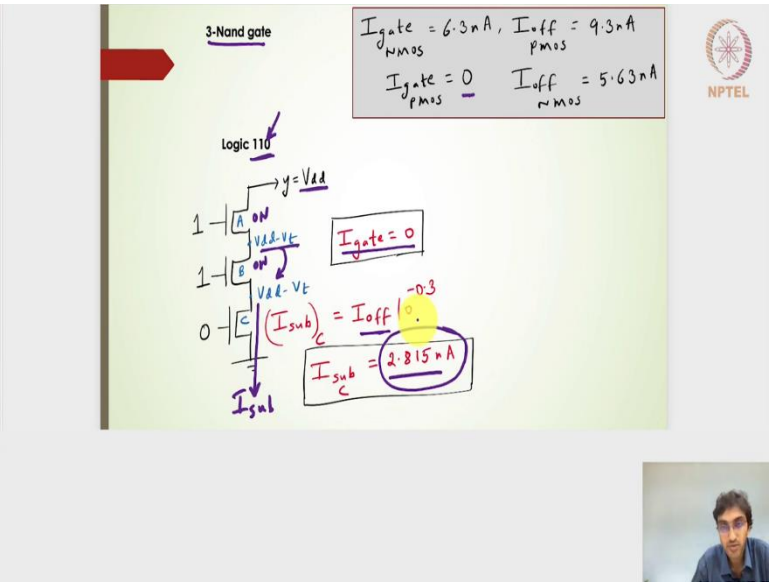

To begin with this particular lecture let us start with the 3 input NAND gate where I will also pick my pointer and the 3 input NAND gate where with logic of 1 1 0. What should be the gate leakage current and what should be the sub threshold leakage current? if it is actually 1 1 0 here, we know that this being on going to act like a pass transistor.

On one side it is V_{dd}, it is going to pass it $V_{dd} - V_t$ here and just being the transistor also being on. It is going to pass the $V_{dd} - V_t$ into the other side of the diffusion. The C transistor is the 1 which is off. I am going to get the sub threshold leakage current coming from the C transistors.

The subthreshold leakage current, where one side it is $V_{dd} - V_t$, the other side it is 0. I will have,

$$I_{subc} = I_{off}10^{-0.3} = 0.501I_{off}$$

$$\text{Where, } I_{\substack{off \\ NMOS}} = 5.63nA$$

$$I_{sub} = 2.815nA$$

The gate leakage current here we need to identify which of the transistors are really on and then try to identify the gate leakage current from that on transistor. These two transistors are actually on, but because my V_{gs} value which turns out to be actually be load very low that is nothing but V_t value.

My gate leakage current in both these cases will be 0. I will have a gate leakage current of 0 here. In this particular logic we will have 1 1 0 we have the even on the PMOS side we will not have any subthreshold leakage current and then the gate leakage component although it is a 0 transistor here which means it is an on transistor on the PMOS side.

The gate leakage current in the PMOS side is considered to be 0. We will not have any gate leakage current, we will not have any subthreshold leakage current coming from the PMOS transistor side or the pull ups circuit. On the pull down circuit we will have a gate leakage current of 0 and then the sub threshold leakage current of 2.815. My static power will be nothing but 2.815 x 1 volts which will be nothing but 2.81nW, hope this is clear.

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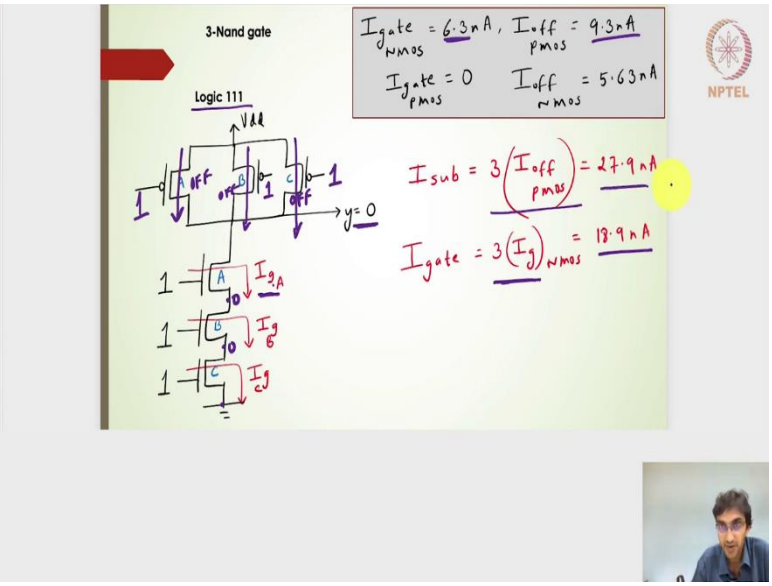

Moving ahead if I have a logic of 1 1 1 then I will have this on the NMOS side I will have all the transistors to be on. My subthreshold leakage current will be 0 and on transistor is going to give me the gate leakage current because the on one side the output terminal node is 0.

All the transistor is going to yield or going to give us the gate leakage current and the gate leakage current because it is 0. I will have a 0 here I will have a 0 here if I consider it to be a pass transistor and then I will get a V_{gs} value for all the 3 transistors to be nothing but V_{dd}.

I will get a gate leakage current for the A transistor for the B transistor and C transistor. The overall gate leakage current on the pull down side will be nothing but the gate leakage current of the A transistor plus B plus C transistors, it will be 3 times the gate leakage current for an NMOS transistor. It is nothing but,

$$I_{gate} = 3(I_g)_{NMOS} = 18.9nA$$

The sub threshold leakage current if I because of the pull down side all the transistors are on. I will not have any sub threshold leakage current coming from the pull down side whereas, on the pull up side I will have all the 3 transistors to be OFF because the logic of 1 is applied here.

I will have an OFF transistor here I will have an OFF transistor here and I will have an OFF transistor on the C transistor on the PMOS side as well. This OFF transistor is going to yield or going to give us the individual because all these 3 PMOS transistors are in parallel. We will have an individual sub threshold leakage current, we will have an individual sub threshold leakage current we will have an individual sub threshold leakage current.

The subthreshold leakage current will be nothing but,

$$I_{sub} = 3(I_{off})_{PMOS} = 27.9nA$$

The total of this will give me the total leakage current and multiplied by $1V_{dd}$ will 1 volts will give us the total static power for this particular logic of 1 1 1.

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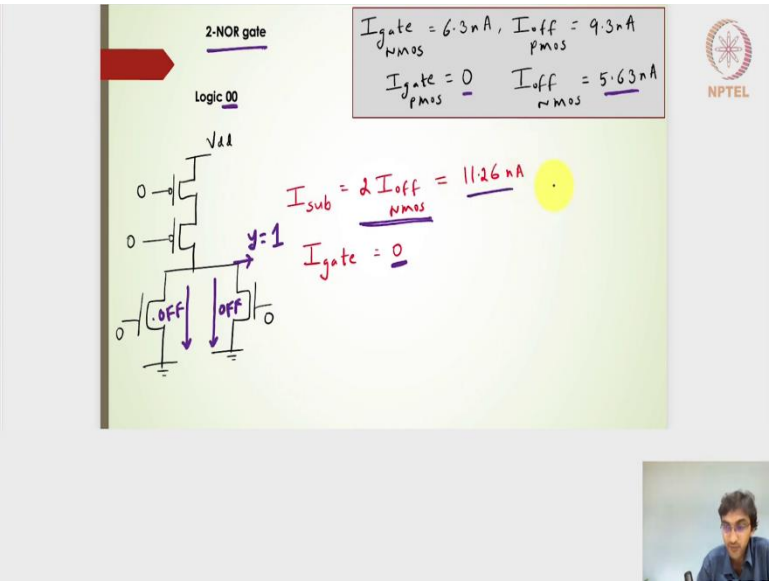

Moving ahead. Let us take a look at the 2 input NOR gate because this will give us some analysis towards the PMOS sides of threshold leakage current and how do we evaluate the static power. For a logic of 0 0 here that means, on the pull down side I have a logic of 0 0, both these transistors are OFF. My gate leakage current will be 0 coming from the pull down side and the gate leakage current on the pull up side is anyway 0 because that is what we have been assuming.

The sub threshold leakage current here will be coming from 1 transistor will be coming from 1 transistor because my output logic here is nothing but 1 because both these transistors are ON and it is going to drive the output logic to a logic level of 1. My subthreshold leakage current will be nothing but coming from 2 independent OFF transistors.

$$I_{sub} = 2(I_{off})_{NMOS} = 5.63x2 = 11.26nA$$

The gate leakage current is anyway 0 because these two transistors on the pull up side are ON, I will not have any subthreshold leakage current coming from the pull up circuit. My overall static power will be nothing but 11.26nA x 1 volts = 11.26nW.

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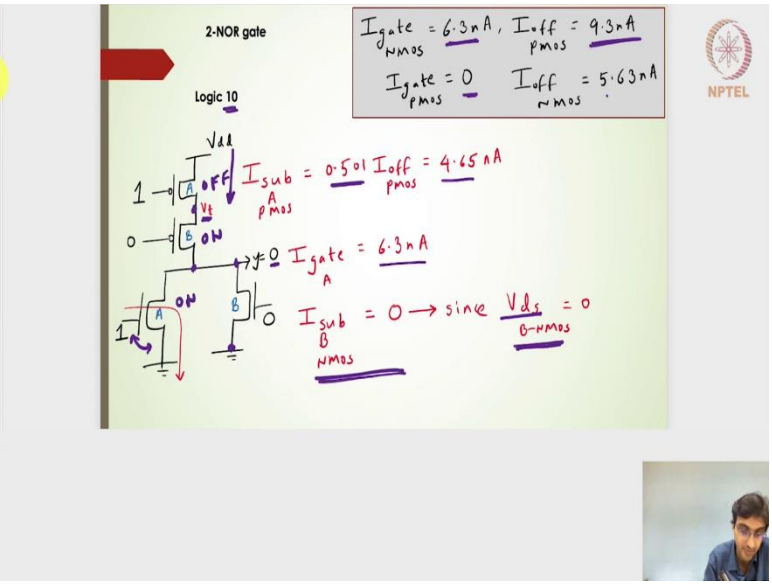

Moving ahead if I have a logic of 1 0, we know that the output will be pulled down. That the output will be 0 here and I will have a gate leakage current coming from this on transistor because the V_{gs} value here is nothing the 1 volts. I will have a gate leakage current that of 5 gate leakage current that of the NMOS transistor which will be 6.3nA. The B transistor is OFF here. I will not have any gate leakage current coming from the B transistor on the pull down side. But even that in the subthreshold leakage current because of the OFF transistor will also not be there because on one side I will have a 0 voltage on the other side also I will have a 0 voltage since the V_{ds} for the B transistor on the NMOS side is 0, I will have the subthreshold leakage current coming from the OFF B transistor on the NMOS side will also be 0.

On the pull up side there is one transistor which is OFF and the other transistor which is ON because of the 1 0 logic and because this is the ON transistor and the other side of the diffusion it is 0. This particular node will be discharged to V_{dd}. If I have a y is equal to V_{dd} and then it is kind of discharge to 0. This particular node value will actually have some particular node higher node voltage and while it is discharging through this, the pull downside it will limit itself to V_t. It cannot reduce more than V_t value otherwise this channel will not be there. It will be limited to V_t and that is what the PMOS pass transistor works like. If it is 0 on this side it is going to have or limit at the voltage of V_t on the other side.

If I have a V_t voltage here then I should be able to find out the subthreshold leakage current which will be nothing but having a potential difference of $V_{dd} - V_t$. On the PMOS side it will give me,

$$I_{\underset{\text{PMOS}}{\underset{A}{sub}}} = 0.501(I_{off})_{PMOS} = 4.65nA$$

The gate leakage current is anyways on the PMOS side is negligible, it is considered to be 0. Finally, I will have a total gate leakage current,

$$I_{\underset{A}{gate}} = 6.3nA$$

If I add this up and then multiply by 1 volts, I will get this static power.

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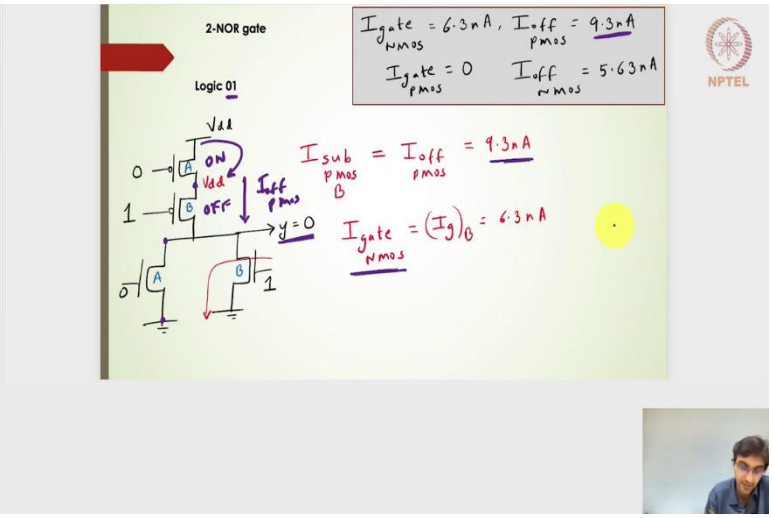

Moving ahead logic of 0 1. If I have a 0 and 1, 0 and 1 here. On the pull down side I will exactly have the same things as set off on the previous slide. The gate leakage current on the NMOS side is now coming from the B transistor. The subthreshold leakage current for the A transistor is anyway 0 because on both the sides of the diffusions it is the same potential. The potential V_{ds} for the transistor A is 0 and hence the subthreshold current will be 0. Now, because this is 0 and 1 here on the pull up side, the 0 makes this a transistor ON and its going to pass the V_{dd} voltage onto the other diffusion side and this particular OFF transistor because it sees a V_{dd} value here and then the output node as 0 here I will get an I_{off} of PMOS as a sub threshold leakage current. The I_{off} of the PMOS is nothing but,

$$I_{\underset{B}{sub}}{}_{PMOS} = I_{off}{}_{PMOS} = 9.3nA$$

My total leakage current will be 9.3 + 6.3 x 1 volt will give me the static power.

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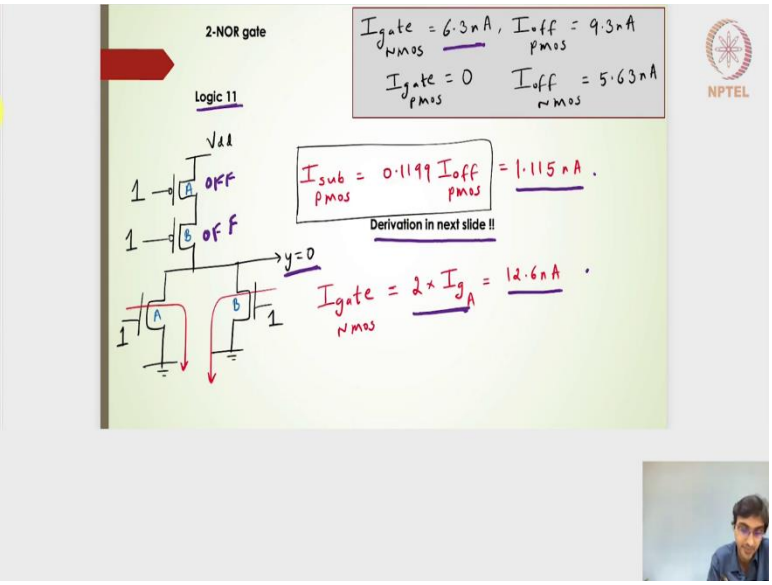

Moving ahead if I have a logic of 1 1 that means, 1 and 1. My output node is pushed or pulled to 0 volts. I have a 1 and 1 here will not have any kind of the subthreshold leakage current on the pull down side. I will have only the gate leakage current and a gate leakage current coming from the two transistors will be nothing but,

$$I_{\underset{NMOS}{gate}} = 2xI_{\underset{A}{g}} = 2x6.3 = 12.6nA$$

Both these transistors are OFF on the pull up side. I will have the subthreshold leakage current coming from the PMOS transistors which is actually derived in the next slide. It turns out to be very very similar to that of the $0.1199I_{off}$, which we had arrived which we have deduced for the NMOS transistors.

$$I_{\underset{PMOS}{sub}} = 0.1199I_{\underset{NMOS}{off}} = 1.115nA$$

The total leakage current will be nothing but this plus this and if I multiply by 1 volts, I will get the static power. Now, in the next slide we will have a look into this particular derivation for the PMOS transistor.

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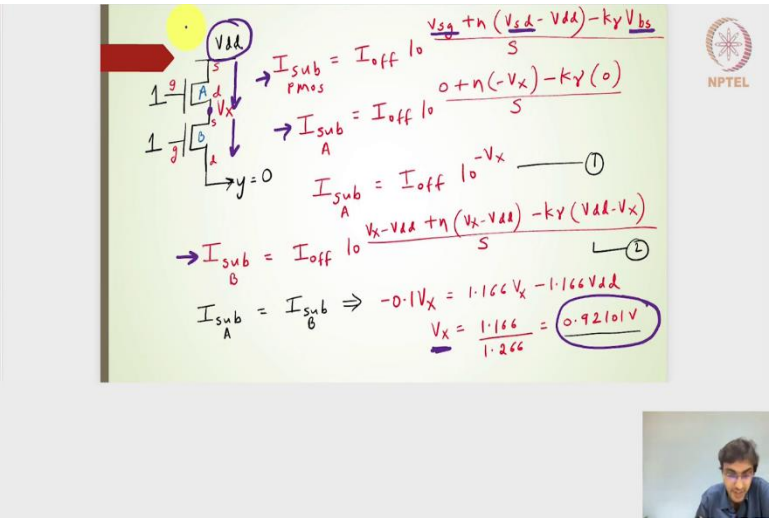

Although it is very very similar to that of the NMOS transistor, I can quickly go over it. The sub threshold leakage current or an expression for the subthreshold leakage current for a PMOS transistor is very very similar to that of the NMOS transistors. If I write the NMOS transistor expression and then compare that for the PMOS transistor instead of V_{gs} it is V_{sg}

$$I_{\substack{sub \\ PMOS}} = I_{off} 10^{\frac{V_{sg}+\eta(V_{sd}-V_{dd})-K_\gamma V_{bs}}{S}}$$

The expression remains the same only thing, the voltage references are been symmetrically opposite. If I have this particular expression for the PMOS transistor then having this particular V_{dd} values and then the stack transistors and then the output node to be 0, we know that this particular subthreshold the leakage current for the transistor A will be same as the sub threshold leakage current for the transistor B.

Applying this particular V_X variable value and then on the logic level of 1 which is nothing but V_{dd} into this particular expressions we should be able to find out the subthreshold leakage current or express the subthreshold leakage current for the transistor A and express the subthreshold leakage current for the transistor B. Equate them and then we should be able to arrive at a $V_X = 0.92101V$ which is kind of very very close to 1 volts. If I remember the two stack transistor for an NMOS transistor we got the V_X value very very close to the 0 volts. Here in the two stack PMOS transistors we will get the V_X value very very close to the V_{dd} value of 1 volts, that is the difference.

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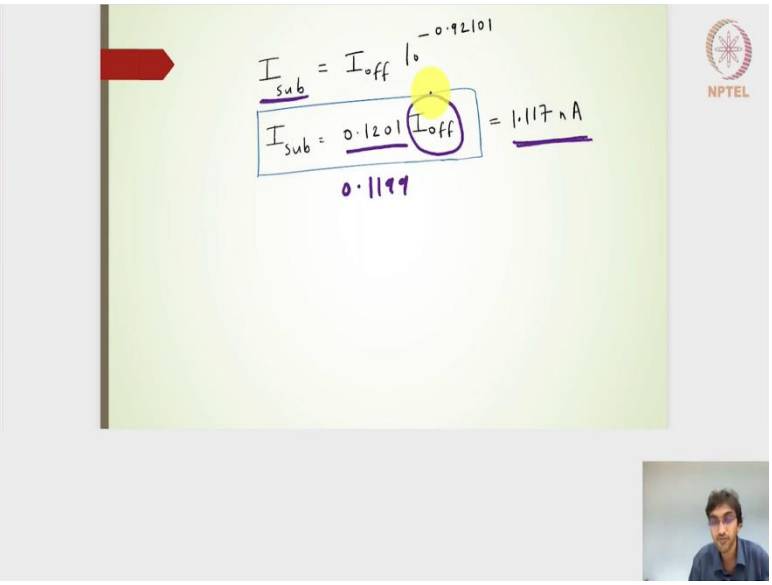

Once I have the V_X value I should be able to find out the subthreshold leakage current putting into one of those equations of I_{sub1} or I_{sub} for the transistor A or I_{sub} for the transistor B turns out to be very very close to 0.1199 of the I_{off} value, it is 1.117nA for the PMOS transistor.

Remember that the I_{off} value of the PMOS transistor is different than that of the I_{off} transistors of NMOS. In fact, the I_{off} of the PMOS transistor is slightly higher than that of the I_{off} of the NMOS transistor.

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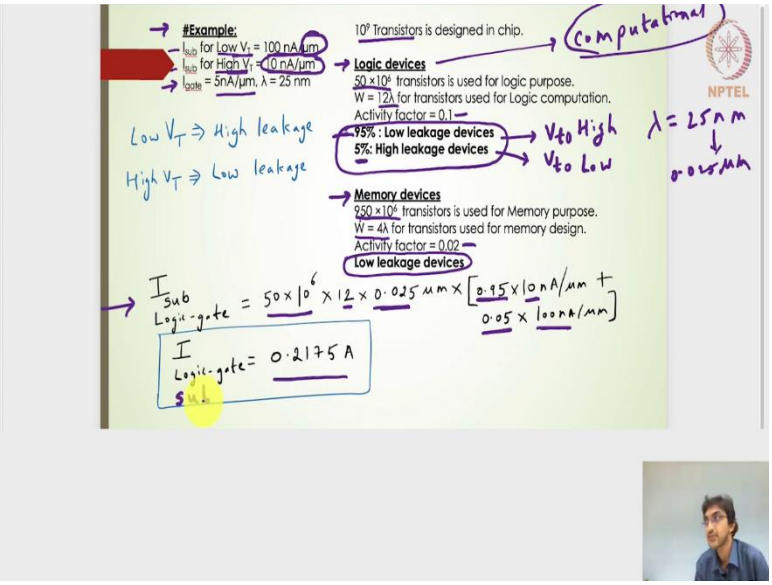

This completes our evaluation for a given circuit how do we evaluate for a different input combinations, what should be the static power. Now let us take an example on a system side. The system side means, we have been given a design wherein we have a 10^9 transistors being used in the chip and in the chip there is two designs, logic devices, logic component and another is the memory device. This logic devices will help is designed for the computational part and then the other set is the memory devices. So, out of this 10^9 transistors we have 50 x 10^6 transistors used for this logic purpose used for designing this computational purpose.

The remaining 950 x 10^6 transistors are used for the memory purpose. The width that has been designed for the transistors is 12λ for the logic purpose, width of 4λ is being used for the memory design and as this width is kind of useful to you know while we are estimating the currents.

I will come to that particular current. The activity factor of 0.1 and 0.02 is given although if you are trying to evaluate the static power the activity factor does not have any role. The activity factor is actually useful only for estimating the dynamic or the switching power not in the static power. The another data is given that in the memory devices all of them are low leakage devices. In fact, low current leakage devices and in the logic devices 95% of the logic devices or the transistors that has been used is of low leakage devices. The low leakage means low leakage current devices that means, I will use or the design has used a higher V_t cell.

The V_t cell is high so that I will get a low leakage current. If you remember the exponential term in one of the previous lectures where we had said that the leakage the subthreshold leakage currents was a function of exponent of $V_{gs} - V_{to}$ where that V_{to} if it was low, I got a high leakage current. If the V_{to} was high, I got the low leakage current.

Similarly the 5% of the transistors that has been used for the logic devices which is 50 x 10^6 transistors out of that 5% is been built using the high leakage devices that means I will have a V_{to} to be low. What it means is this design has been done 95% of the time caters to the low leakage current and then 5% it is very very essential and that is why they have gone for the low V_{to}. Remember that the low Vt0 will give me the current, the long channel current model if I estimate the saturation current and then the linear current will be higher.

But 95% of the time it is at the low leakage current and if I consider the low leakage current it is nothing but 10nA which is for the high V_t cell and for the low V_t cell it is giving me 100nA per width of the transistor. It is actually characterized in terms of the leakage current per the width of the transistor, that is why the micron is given here, 100nA/um.

For a transistor if I want to evaluate if it is a transistor of low leakage devices which has used high V_{to}, the low leakage devices will have 10nA/um multiplied by what is that width of the transistor. The width of the transistor is 12λ, where lambda for the 65nm technology node is nothing but 25nm.

I will have to express this in a micro ampere. So, 0.025uA, alright. Hope this particular statement is clear, the example of the system design is clear. Also one more characteristics is given is the gate leakage current for an NMOS transistor is 5nA/um.

In this particular case let us try to find out what should be the sub threshold leakage current for the logic device first and then try to calculate the sub threshold leakage current for the memory devices and then calculate what is the gate leakage current for all the logic as well as the memory devices and then try to combine both of them and then evaluate the static power. The sub threshold leakage current for the logic device here the logic device is this

$$I_{\substack{sub \\ logic-gate}} = 50x10^6x12x0.025umx\left[\frac{0.95x10nA}{um} + \frac{0.05x100nA}{um}\right]$$

$$I_{\substack{sub \\ logic-gate}} = 0.2175A$$

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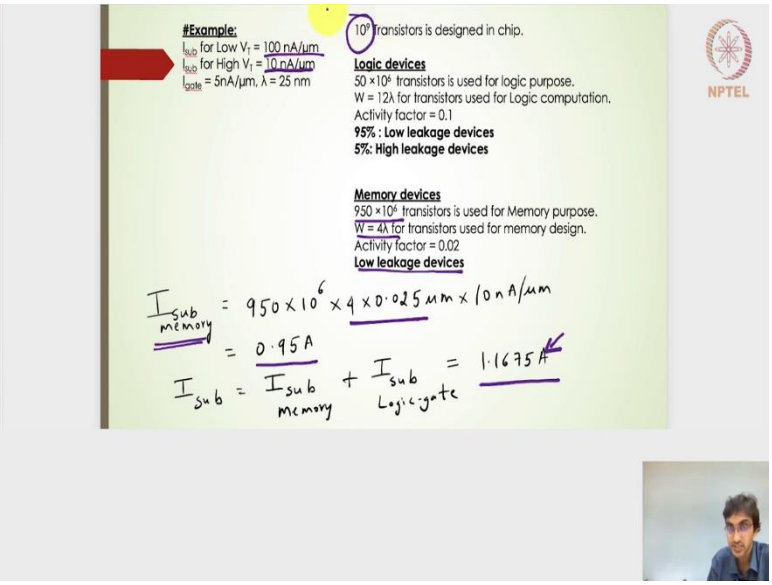

Similarly, if I can evaluate or estimate the memory devices and then the sub threshold leakage current for the memory devices which will be nothing but 950 into 10 raised to 6 and all of them uses the low leakage devices.

$$I_{sub\ memory} = 950x10^6x4x0.025umx10nA/um$$

$$I_{sub\ memory} = 0.95A$$

If I go back, I used to get for the logic devices it was 0.2175 for the memory devices it is 0.95A. The total sub threshold leakage current is nothing but accumulate both of them and we will get,

$$I_{sub} = I_{sub\ memory} + I_{sub\ logic-gate} = 1.1675A$$

Note the unit is amperes because although it is a nA that is what is defined here. It is the number of transistors in the design which essentially accumulates to the ampere value.

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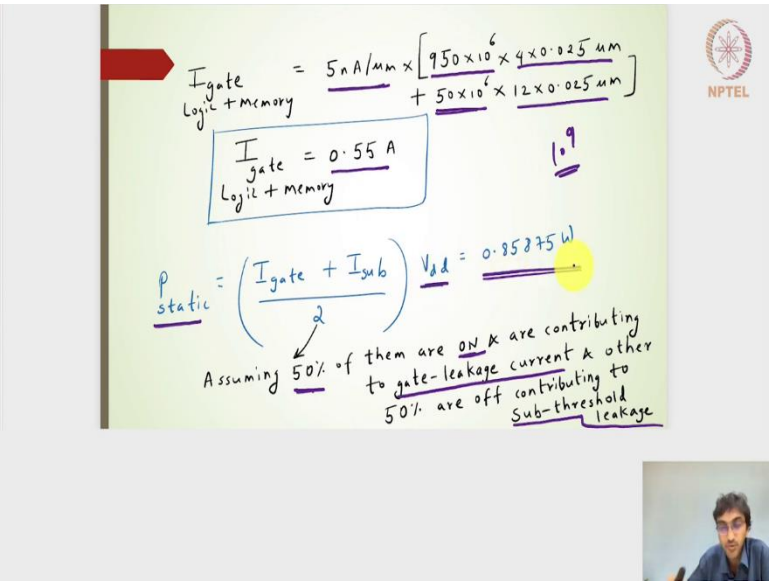

The last one, the gate leakage current for the logic as well as the memory.

$$I_{sub}{}_{logic+memory} = 5nA/umx[950x10^{6}4x0.025um + 50x10^{6}x12x0.025um]$$

$$I_{sub}{}_{logic+memory} = 0.55A$$

Now, I have the gate leakage current and then the sub threshold leakage current for this overall system design which uses 10^9 of the transistors then we should be able to evaluate the static power.

Now, remember that while we are considering the gate leakage current and then the sub threshold leakage current the transistors which are OFF are contributing towards the sub threshold leakage current. The transistors which are ON are contributing towards the gate leakage current. If I want to accommodate both the gate leakage current and then the sub threshold leakage current we have to ensure that we have to assume something. If it is not given. we have to assume something that one assumption that we can make is 50% of the transistors 50% 10^9 transistors which has been used to design this system we can assume that they are contributing towards the gate leakage current that means, that they are ON. The remaining 50% of the transistors of the 10^9 transistors are OFF and they are contributing towards the sub threshold the leakage current.

With that assumption we can estimate the overall total current. The total current turns out to be the gate leakage current 50% of that and then the sub threshold leakage current 50% of that because 50% of them are ON and that they will contribute towards the gate leakage current. The 50% of the transistors are OFF and they will contribute towards the sub threshold leakage current. If I do that multiplied by the V_{dd} I should be able to find out the static power. Static power turns out to be,

$$P_{static} = \frac{(I_{gate} + I_{sub})}{2} V_{dd} = 0.85875W$$