Design and Analysis of VLSI Subsystems
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Lecture - 69
Introduction to subthreshold leakage current model

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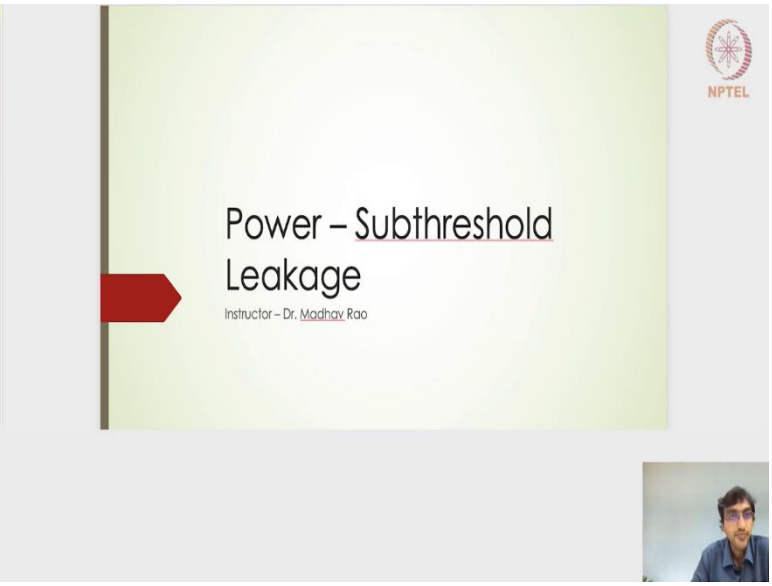

Hello students, welcome to this lecture on the sub threshold leakage part. When we talk about the power, it is not only about the dynamic power or the switching power, but it is also about the static power. I think in this module and in the subsequent modules we will cover this particular aspect of the power which is also an important characteristics while we design the digital circuits.

Static power as the name suggests, it is basically when the circuit is in a steady state conditions and we assume that when we develop the circuit in a CMOS, using the CMOS family of logic circuits once the output voltage reaches a steady state value there will not be any power. But that is not the case, there will be some kind of a leakage current that will be coming from either from the junction in the body to the diffusion node junctions or there will be a sub threshold leakage current that is nothing but the leakage current which will be flowing from the drain to the source side, even when the circuit is in a steady state.

There is one more the leakage current that will be flowing from the gate to the body or gate to the source side, that is also called as gate leakage current. There are basically three aspects of the leakage current and then once we have the leakage current, there will be a voltage drop across the transistor. The current multiplied by the voltage will give us a power and this particular power associated with the leakage currents with all the three components of the leakage currents is termed as this static power.

What we will do is in this particular set of lectures is try to understand the sub the components of the leakage current and we will look into the two important aspects of the leakage current. One is the sub threshold leakage current with which we will start in this particular lecture. Then the subsequently we will have a look into the gate leakage current. The junction leakage currents are a factor less than that of these two leakage currents. Hence, we are not going to look into the junction leakage currents. But we will emphasize more on the sub threshold leakage current and the gate leakage currents.

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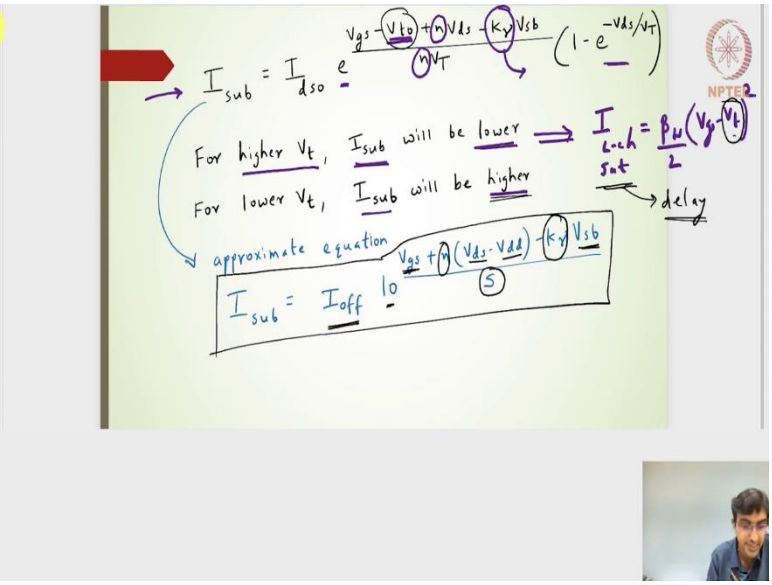

Moving on let me also take the pointer, I have written an expression of the sub threshold leakage current.

$$I_{sub} = I_{dso} e^{\frac{V_{gs} - V_{to} + \eta V_{ds} - k_\gamma V_{sb}}{\eta V_T}} \left(1 - e^{\frac{-V_{ds}}{V_T}}\right)$$

This is an empirical expression that means, after carrying out several experiments an empirical expression or an expression to fit those particular experimental records of the data, this particular expression has been derived. It is an exponential expression and then there is one more exponential term here. There are lot of the voltage references the V_{gs} as we know it is gate to source voltage V_{to} is nothing but the threshold voltage, it is an absolute threshold voltage. The V_{sb} is the source to body voltage V_{ds} is again the drain to source voltage V_t is the thermal voltage which is nothing but $\frac{kt}{q}$.

There are two parameters here or two constants here which one is k_γ and then another is eta. This k_γ is nothing but the body effect or the body effect coefficient and η is nothing but the drain induced barrier lowering coefficient and we will have a look at it in the next slide. One important aspect of this particular expression is the V_{t0}. If I use a typical V_t value of 0.3 volts I will get some current but in generally in the technology node files or the library files we can select different V_t based standard cell libraries.

If I use a higher V_t, that means, this particular V_{to} should be higher. We can choose a V_t of 0.4 or we can also choose a lower value of V_t cells of 0.2 as well. Based on that our sub threshold leakage current will change, because this V_{t0} it is in the exponential term. We will have an exponential increase or an exponential decrease in the sub threshold leakage current. If I choose a higher V_t here, that means, this difference between $V_{gs} - V_t$will be lower and thereby my sub threshold leakage current will be lower, this is I sub threshold will be lower.

If I choose a lower V_t. The lower V_t will give me $V_{gs} - V_{t0}$ to be higher, an exponential to that of the higher value will always give me a sub threshold increase in the substation leakage current, the I sub will be higher. What we really want is to have a lower the subthreshold leakage current. In that sense we will have to use the higher V_t, but there is one problem there. If I look into the driving factor or the current that is there to charge the capacitance or charge the output node or discharge the output node.

If I consider the long channel current and let me pick a saturation current. In that sense it is nothing but, $I_{L\text{-}ch} = \frac{\beta_n}{2}(V_{gs} - V_t)^2$. Of course, there is a two term here, it is $(V_{gs} - V_t)^2$. Now, if I choose a higher V_t here, $(V_{gs} - V_t)$ is going to be less and my long channel saturation current is likely to be dropped. This will have an effect, a lower drop in the

current is likely to have a lower charging or discharging effect and thereby the delay is likely to be increased. A higher V_t is likely to give me a reduced sub threshold leakage current and thereby a reduced static power.

But, it will have an effect in the performance in the overall performance. Similarly if I choose a lower V_t here the current is going to be better its going to be higher and my delay is going to be much less, it is likely to give me an improved performance. But my sub threshold leakage current is going to be higher. Again, there is a compromise here there is one, if we have to cater to one aspect, the other aspect tends to lag or we have to compromise on the other aspect.

In that sense there is always a trade off and based on the design requirements, one will choose the V_t cells. Now, this particular expression turns out to be a little bit complex in applying for the digital circuits and then try to analyze the circuits in terms of the subthreshold leakage current or to evaluate the static power. A better or an approximate equation is been stated and that is this particular expression, whatever I have mentioned here. The I_{sub} is nothing but I_{off} and then it is given in terms of instead of an exponential term here, e term it is nothing but 10 raised to 10 power term, with the expressions of V_{gs}, V_{ds}, V_{dd} and V_{sb} is given here.

Then there is another term here as which is nothing but the sub threshold leakage slope and I will come to that in the next slide and then η is still there in the same and DIBL coefficient which is nothing but the Drain Induced Barrier Lowering and k_γ is nothing but the body. Thus, the source to body coefficient or the source to body effect coefficient and the similar terms V_{ds}, V_{sb}, V_{dd}, V_{dd} is nothing but the rail voltage, V_{gs} gate to source voltage everything remains same. I_{off} is one of the component which we will come in the next slide which I will explain in the next slide.

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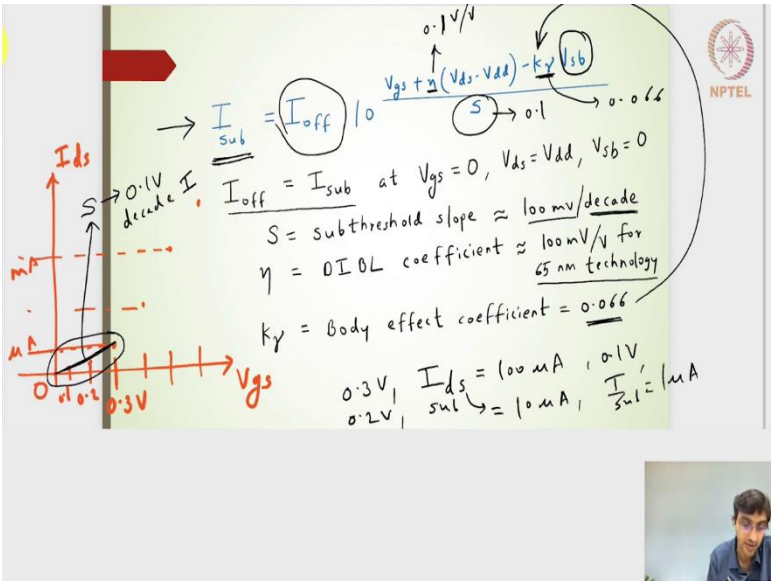

Hope this is clear, moving on this is what the expression we are going to use to analyze the circuit towards the static power or towards the sub threshold leakage current. Let us have a detailed look at it, k_γ what I said was the body effect coefficient and it is given by 0.066. What it really means is if the V_{sb} increases by 1 volts, the source to body voltage increases by 1 volts I will have a k_γ effect of 0.066.

In fact, if you remember if the V_{sb} value increases by 1 volts the k_γ is going to have an increase of 0.066 volts, that will have an improvement or that will have an increase in the V_t of 66 milli volts. An increase in the V_d is likely to have an increase in the V_t is likely to have the decrease in the sub threshold the current as well as the decrease in the overall long channel saturation current or the linear current. That effect has been incorporated. This particular effect k_γ effect has been incorporated directly into the sub threshold leakage current. Instead of going by an increase in the V_{sb}, will have an increase in the V_t and then that V_t component the threshold voltage component is then instead of putting it here we have directly accommodated k_γ V_{sb} in the sub threshold leakage current.

Let us have a look at the η, η is nothing but the DIBL coefficient the Drain Induced Barrier Lowering which is nothing but 100mv/v for the 65nm technology node again these are this constants k_γ S or η it is all the empirical constants arrived for a particular technology node. If I consider the eta here, it is nothing but 100mV/V. What it means is if I change the V_{ds} value for by 1 volts, I will have a drain induced barrier lowering, the channel is likely to

be reduced. The reduced channel is actually have an effect on both the dynamic current as well as on the static or the sub threshold leakage current.

This particular sub threshold leakage current if I have an increase in the η here or rather if I have 100mV/V if that is the constant here, if there is an increase in the V_{ds} I will have the effect in the channel and thereby the subthreshold leakage current is likely to be affected. That has been incorporated in this particular approximate equation in the form of the η. The η will consider for most of our calculation will consider it to be 0.1 which is nothing but 100mV/V. The 0.1v/v k_γ is given as 0.066 as a constant.

The last one is the sub threshold slope and that is 100mv/decade. Let me try to draw a figure here, in the side by, what it really means is if I draw the current versus I know it could be a dynamic current. I am drawing a current of the transistor. I am drawing in fact, a current of drain to source and I am not doing any kind of a partition or a classification between you know it is whether it is a static current or it is a dynamic current.

I am just drawing a current across the V_{gs} voltage. What we knew before was at 0.3 voltage I will get some minimal current and then at 0.4 voltage I will get a higher current and then so on 0.5 voltage will be higher current and then so on. At somewhere here, we said at 0.3 volts that is when the channel will be formed and then after the channel is formed then I will get some amount of current based on the V_{ds} value. If the V_{ds} value is more than the $V_{gs} - V_t$, I will get the saturation current, that is what we used to say.

Let us say that the transistor is in saturation and then I will get some current here and it will be $V_{gs} - V_t$ that is the whole square. I should have a square relationship and that is these are those points, note that here at 0.3 volts I have drawn a non-zero current. This will be a non-zero current this particular point, but it will be very close to the 0 current. What it really means is if these currents are in the range of milliamperes, I will get some kind of a current here in the range of microamperes. But there will be some current, there will be some non-zero microamperes of current right and if I go back to 0.2 volts and then 0.1 volts right, we used to say that the channel is not at all there and then there will not be any current at all.

But that is not the case, there will exist some kind of a channel where the drain to source will still be the drain to source will still be having some negligible amount of current and

that is called as the sub threshold leakage current and that particular current is I can point it out in the form of the dots, this particular slope in the sub threshold region that is below 0.3 volts for our typical V_t values. If I draw this particular line, I can have some kind of a linear line if I consider it for a decade change in the current. I will have some kind of a slope here. What this slope says is I mean this is this sub threshold the slope S. That has been characterized in a way that if I change my V_{gs} value for 0.1 volts, if I change my the voltage values in terms of 0.1 volt, I will get 0.1 volts means 100mv I will get a decade change in the current.

A decade change in the current, what it means is if it is at 0.3 volts, I am going to say that I_{ds} or rather sub threshold current. Let us say that the sub threshold current is 100uA, at 0.2 volts the same current, we will be having a decade change in the current.

I will have at 10uA, at 0.1 volts at 0.1 volts I will have the, I_{sub} threshold current as 1 milliamp or 1uA. I will see a decade change in the current and that is what the slope says here. The slope indicates that the change in the current with respect to the change in the voltage and that is what is incorporated here and we will use this in our approximate sub threshold leakage current equations.

Hope this is clear all the three terms k gamma, S and n are clear. The S we will consider it to be 0.1, because it is 100mv/decade and we will consider it to be 0.1. This η is 0.1 k_γ is nothing but 0.066, hope this is clear.

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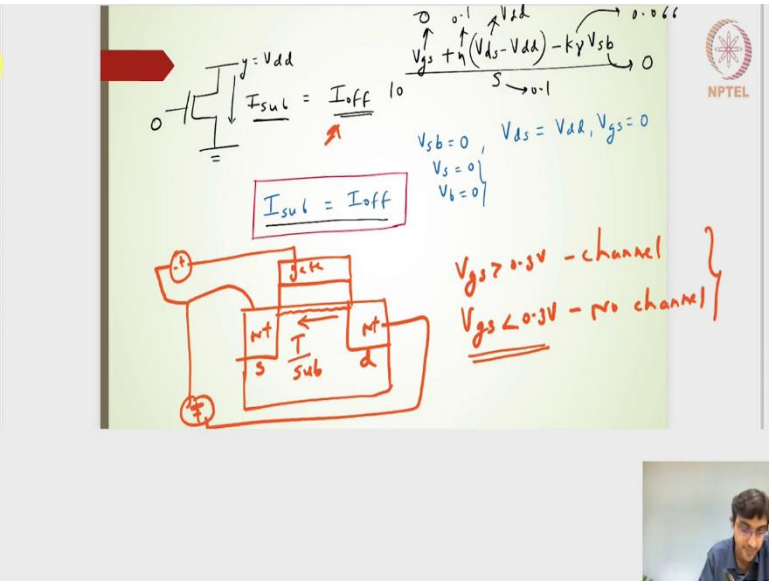

Let us take a single transistor here and I will come to that I_{off} value or in fact, I will just define that I_{off} is stated as nothing but I_{sub} at V_{gs} of 0 volts and V_{ds} of 1 volts or rather V_{dd} rail and V_{sb} is 0. Basically in an ideal transistor where I have the drain to source a potential as V_{dd} rail or V_{dd} and there is no body effect. The V_{sb} is 0 and let us say that the gate side there is a 0 volts, then I will get whatever is that particular current is the I_{sub} or rather whatever is the subthreshold leakage current that is nothing but I_{off}.

This is basically this particular term is nothing but the sub threshold leakage current, when the transistor is completely off. Let us move ahead into this particular transistor, analyze this particular single transistor and then try to find out the subthreshold leakage current.

In this particular transistor of an NMOS we have this V_{ds} as V_{dd}, the V_{gs} has 0. If I put it in this particular expression of 10 raised to V_{gs}, V_{gs} is anyways 0, η that it is 0.1. The sub threshold is 0.1, k_γ is 0.066 V_{ds} in this case it is nothing but V_{dd} and V_{sb} it is we will consider it to be 0, if it is not given or if it is not given will anyways assume the body for an NMOS transistor to be connected to the ground and body of the PMOS transistor to be connected to the V_{dd}.

In that sense V_{sb} will be 0, if I have all these components all the numerator will be 0.

$$I_{sub} = I_{off} 10^{\frac{V_{gs} + \eta(V_{ds} - V_{dd}) - k_\gamma V_{sb}}{S}}$$

$$I_{sub} = I_{off}$$

Indeed in our definition of I_{off}, which is nothing but I_{sub} when the transistor is completely off that means, the V_{gs} is 0 is indeed correct. I will also like to reiterate here what you know at a cross sectional level, when I draw the NMOS transistor what we used to say is I had a diffusion pocket and this is oxide and then this is the gate, what we used to say is whenever this is the gate to source. This is my source, this is my drain and let us say that I have some potential here. The Drain to source and then some potential here a gate to source.

We used to say that V_{gs}, only when it is greater than 0.3 volts I will have the channel. I will have some channel here and if V_{gs} is smaller than 0.3 volts, there will not be channel. I say there is a no channel, which is incorrect. We cannot have this kind of a demarcation

in a transistor. Now, the channel will appear and then channel will disappear at 0.3 volts if it is greater than 0.3 volts I will have a channel.

If I have 0.299 volts I will not have a channel. That is kind of a slight approximation which we are done to find out this channel and then the current through the channel. Which is generally in the range of 100s of uA to mA. But when the channel is not there, that is when the V_{gs} value is in the below 0.3, that is it is below the threshold voltage also called as the subthreshold region. We will still have some kind of a current that will be flowing from the drain to source.

This we call it as the sub threshold leakage current and what we have seen here is using this particular expression of the approximate equation, we should be able to find out given the values of V_{gs}, given the value of V_{ds}, given the V_{sb} value using these constants. The etas, the k_γ and then the sub threshold slope, we should be able to find out the sub threshold leakage current for the transistors. Hope this is clear, moving on.

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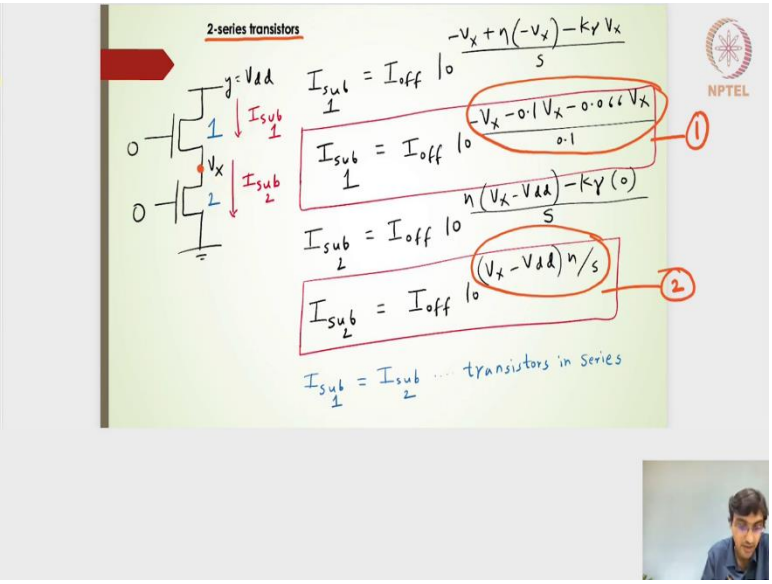

Let us say that if I have two series of transistors. There are two series of transistors and both of them are off that means, it is not about the threshold. The V_{gs} for this transistor 1 and V_{gs} for the second transistor both of them are below 0.3.

We will have it is already in the subthreshold region and then we should be able to calculate what is the sub threshold using this particular expression. If I say that this is transistor 1

and 2, I need to find out what is V_{gs}, V_{gs} turns out to be if I write this particular inter node voltage as V_X this particular $V_{gs} = -V_X$. The $V_{ds} = V_{dd} - V_x$ for the second transistor $V_{gs} = 0$, for the second transistor $V_{ds} = V_X$.

If I put those particular parameters into this sub threshold current and because these two transistors are in series, I know that in the series that currents even the sub threshold leakage current will be the same. I should be able to find out I_{sub1}, I should be able to find out I_{sub2} or rather express this I_{sub1} and I_{sub2} and then equate it. Then I should be able to find out this particular node voltage.

Now, to express I_{sub} the sub threshold leakage current for transistor 1 and then subthreshold leakage current for transistor 2, I will use this approximate equation

$$I_{sub1} = I_{off} 10^{\frac{-V_X + \eta(-V_X) - k_\gamma V_X}{S}}$$

$$I_{sub1} = I_{off} 10^{\frac{-V_X + 0.1(-V_X) - 0.066 V_X}{0.1}}$$

$$I_{sub2} = I_{off} 10^{\frac{\eta(V_X - V_{dd}) - k_\gamma(0)}{S}}$$

$$I_{sub2} = I_{off} 10^{\frac{\eta(V_X - V_{dd})}{S}}$$

I will have these two expressions number 1 and expression number 2. If I want to equate these two, that I should be able to find out the V_X values. We know that this current and this current are equal and I_{off} is also equal. I can cancel this on both the sides and if I take the log on both the sides I should be having the only the expressions or in terms of V_X on the numerator and denominator side and then similarly here. I should be able to equate this particular expression with that of this particular expression because the transistors are in series, because the sub threshold leakage currents are same.

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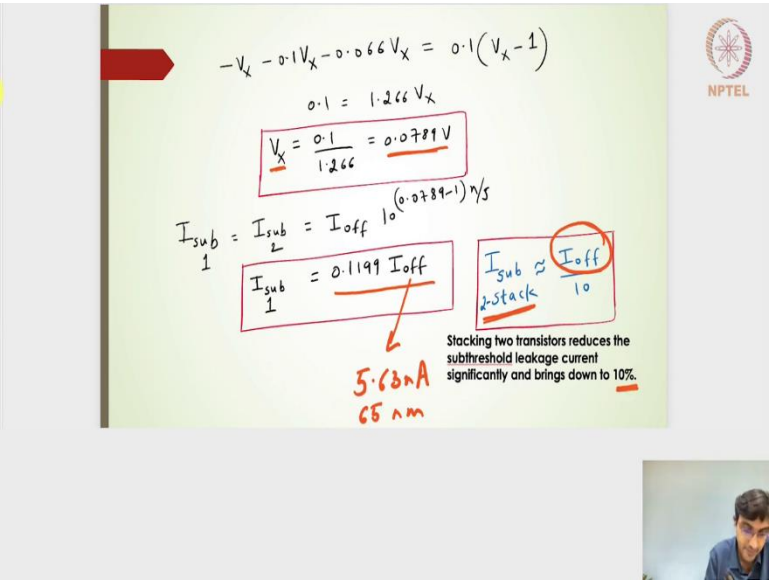

$$-V_X - 0.1V_X - 0.066V_X = 0.1(V_X - 1)$$

$$0.1 = 1.266V_X$$

$$V_X = \frac{0.1}{1.266} = 0.0789V$$

I will have a very minor amount of the leakage current in terms of micro amperes or less than microamperes. It is going to have, even if there is a steady state flow of the leakage current coming from the V_{dd} rail to the off transistor of transistor 1 and the second off transistor and then going to the ground. Because of this minute of current, the voltage that has been developed due to this minute current will be very very small, that will be 0.0789 volts.

Once I have the V_X value, I should be able to find out the actual substantial leakage current. The subthreshold leakage current putting into that one of these equations

$$I_{sub1} = I_{sub2} = I_{off}\,10^{\frac{(0.0789-1)n}{s}}$$

$$I_{sub1} = 0.1199I_{off}$$

The I_{off} current is generally for an off transistor we say that it is kind of somewhere around 5.63nA for an NMOS transistor. If I do that it will be 0.5nA, for a 65nm technology this

is something we will use in the future slides. The I_{sub} threshold, the leakage current or the subthreshold leakage current, if I have two stacked transistors, two transistors which are in series turns out to be $I_{\substack{sub \\ 2-stack}} = I_{off}/10$. This is 0.1199. If I can approximate it to 0.100, I will get $I_{off}/10$, stacking two transistors reduces the sub threshold leakage current significantly and to an effect that it brings down to almost 10%.

Now, which is very very nice. If we have a way to reduce design specifications to reduce the substantial leakage current, now we can always use a foot transistor, a foot transistor which is off. The stacking of the transistor will help in reducing the sub threshold leakage current, the sub threshold leakage power and in directly it will have an impact on the static power. Hope this is clear.

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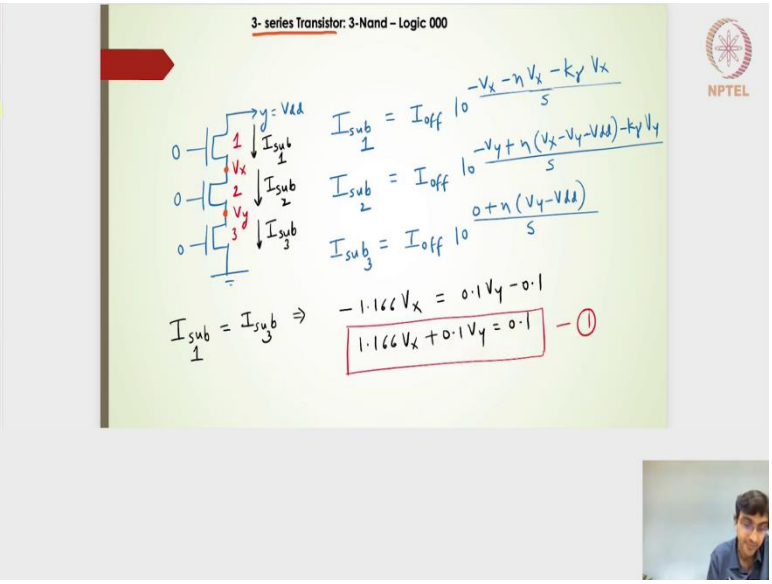

Moving ahead, now what if I have three series transistors, in the last case we had seen two of the transistors in series. Here now, it is three transistors in series. Now, I have to find out the node voltages V_X as well as the V_y the two node voltages, because the three transistors are in series I will have the subthreshold leakage current to be the same. I can write at the sub threshold or express the subthreshold leakage currents in terms of this node voltages. Write the subthreshold leakage current for one transistor, for the second transistor and third transistor and equate it one with that of the third sub threshold leakage current of the first and the third transistors will give me one equation here.

$$I_{sub1} = I_{off} 10^{\frac{-V_X + \eta(V_X) - k_\gamma V_X}{S}}$$

$$I_{sub2} = I_{off} 10^{\frac{-V_y + \eta(V_X - V_y - V_{dd}) - k_\gamma V_y}{S}}$$

$$I_{sub3} = I_{off} 10^{\frac{0 + \eta(V_y - V_{dd})}{S}}$$

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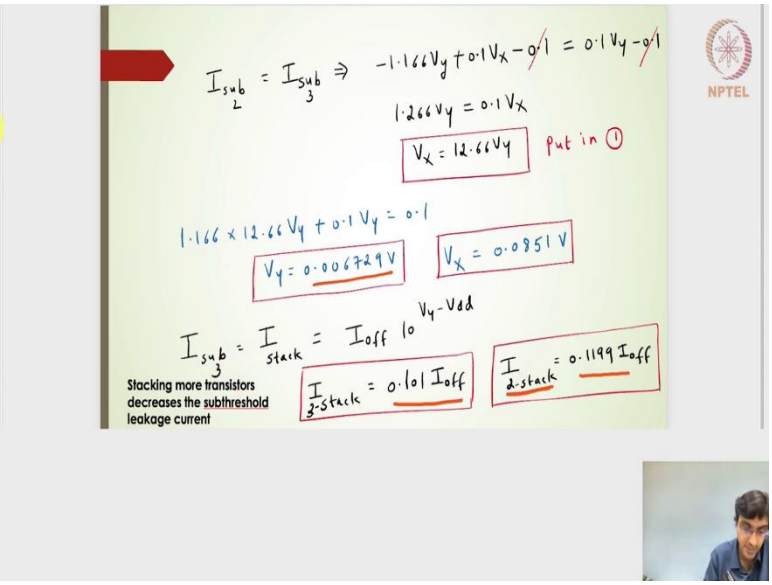

Similarly, if I equate the subthreshold leakage current coming from the second and the third transistor, if I equate it I should be able to find out the second equation.

$$I_{sub1} = I_{sub3}$$

$$-1.166V_x = 0.1V_y\text{-}0.1$$

$$1.166V_x + 0.1V_y = 0.1$$

$$I_{sub2} = I_{sub3}$$

$$\text{-}1.166V_y + 0.1V_x - 0.1 = 0.1V_y - 0.1$$

$$1.266V_y = 0.1V_x$$

$$V_x = 12.66V_y$$

$$1.166 \text{ x } 12.66V_y + 0.1V_y = 0.1$$

$$V_y = 0.006729V$$

$$V_x = 0.0851V$$

If there are two equations and a two unknown node voltages V_x and V_y, I should be able to calculate that putting this particular equation in the first one, we should be able to estimate the V_y and V . If looking at this particular values of V_y and V_x it is 0.006729 and V_x is 0.0851.

The V_x is higher than that of V_y and just to confirm our calculations, V_x is higher than V_y makes sense because if only if I have a node voltage higher than the other one then only I will have the current that will be flowing from the drain to source. If it is the other way, then there is some problem in our equations solving or in our assumptions. In this case what we have assumed is the transistor 1, 2 and 3 there will be a current that will be flowing. Thereby we identified V_x and V_y and it turns out that the V_x potential is slightly higher than that of V_y. Our assumption of the subthreshold leakage current that will be flowing from V_{dd} to ground makes sense.

Also notice that the V_x value and V_y value are in the sub voltage level that means, that it is either in the form of 0.0851 or it is 0.0006729 volts. It is actually very very low again which brings to our attention that the separation leakage current is actually very very minute or very very low, compared to our dynamic current or the transient current which we generally use it to estimate the delay and the power in the dynamic power characteristics.

In that sense the subthreshold leakage current, if I know the node voltages I can put it back into those the sub threshold leakage current expressions and find out the overall sub threshold current which turns out to be 0.101. It is in fact, it is even lesser than when we had the two stack transistor which was 0.1199. It is actually coming very very close to the 10 percent. The 0.101 which is lower than 0.1199 or phi off, stacking more transistors decreases the sub threshold leakage current.

If I have four transistors stacked together the sub threshold leakage current is naturally going to be reduced compared to the three series transistors and the 2 series transistors right hope this is clear, going forward.

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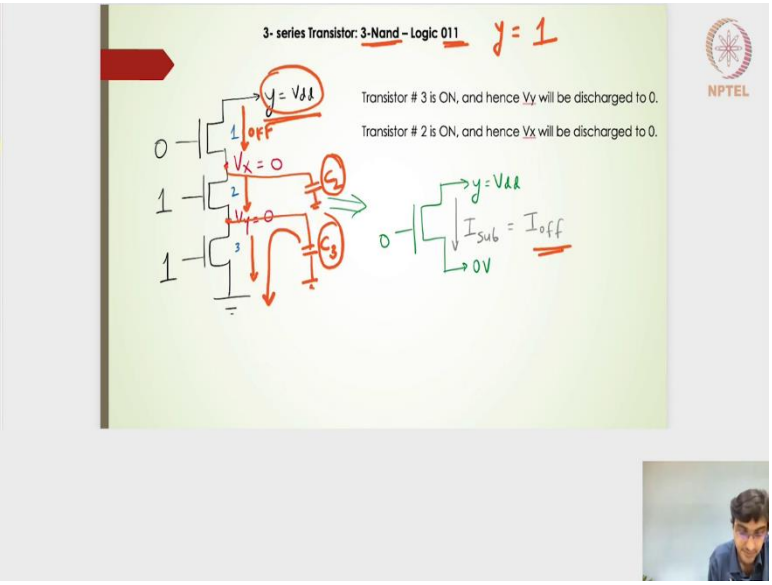

Let us take a you know the question is where are we going to use this stacking effect and how do we how do we use those stack transistors in our evaluation of the static power. If I consider the 3-input NAND gate and with a logic of 011 and I am looking at the pull down circuit, if it is the logic is 011, we know that the output will be 1. That means, that the pull up circuit will be on and the pull up circuit the PMOS transistor is going to ensure that the output is charged to the V_{dd} value. The output starts to V_{dd} value here and in 011, I know that if it is 0 this transistor number 1 will be off. It will be in subthreshold region that means, it should drive the subthreshold leakage current.

The second and third transistor although this is on, because this transistor is off, if this supplies the subthreshold leakage current this is going to take this the supply of the subthreshold leakage current and then put it into the ground.

Now, to analyze what should be the sub threshold leakage current in this particular case, we can consider this particular transistor and then this particular on transistors are both the on transistors to behave like a pass transistor. The reason is if this is connected to the ground and if I have a capacitance here, this capacitance because this is counted in because

this is on, this is anyway is going to get discharged to the ground. My V_y voltage will always be 0.

Similarly, if I consider this there is a capacitance here, C_3 and C_2 I will write. The C_2 capacitance is also well know because this is a non-transistor and we can consider it to be a pass transistor. The C_2 capacitance whatever value it will be charged, there is a path there is a discharging path from this on transistor from this on NMOS transistor and the on another end master transistor which will get connected to the ground. My V_X value can also be considered to be 0. Now, the question is what should be the sub threshold leakage current, the subthreshold leakage current will be estimated by this off transistor.

Now, with these three transistors, we can consider it to be 1 single an equivalent of 1 single transistor, 1 single off transistor where 1 node voltage is connected to V_{dd}, because this is kind of driven by the pull up circuit for the 3-input NAND gate and on the other side the V_X is actually 0 volts. My I_{sub} threshold leakage current is nothing but I_{off}. This will be the subthreshold leakage current, which is going through all the 3 transistors. The I_{sub} threshold leakage current for the transistor 2 and transistor 3 is going to help in complete discharge of the C_2, the diffusion capacitances of the C_2 and C_3, hope this is clear.

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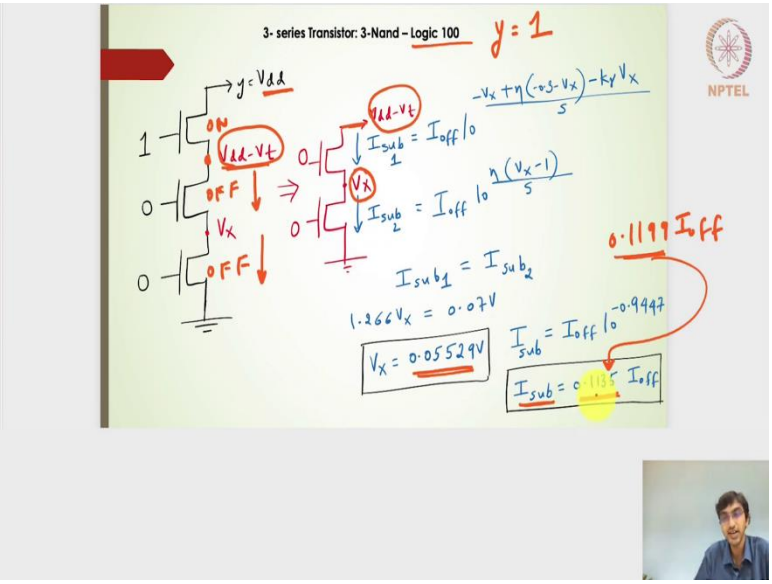

Moving ahead what if I have a logic of 100, again the output if the logic is 100. The output will be 1 that means, that the pull up part of this 3-input NAND gate will be active and will be driving this output node voltage to V_{dd}.

If I have 100 here, these are off transistors, this is going to determine the sub threshold leakage current and this is an on transistor. The subthreshold leakage current is this one and this one, which will be determined by this two of transistors. This one being a non-transistor and if y is held at V_{dd}, I can consider it to be a pass transistor and the other side of the node will be charged to $V_{dd} - V_t$.

If I can actually make these three transistors into two off transistors, where one side it is $V_{dd} - V_t$. on the other side it is grounded, the two of transistors and of the time and both the off transistors are in series. The sub threshold leakage current of this transistor and this transistor should be same. We should be able to use this $V_{dd} - V_t$, use this V_x value in the sub threshold leakage current equate the subthreshold leakage for the first transistor and then the second transistor equate it out and we should be able to find the Vx value,

$$I_{sub1} = I_{off} 10^{\frac{-V_X + \eta(-0.3 - V_X) - k_\gamma V_X}{S}}$$

$$I_{sub2} = I_{off} 10^{\frac{\eta(V_X - 1)}{S}}$$

$$I_{sub1} = I_{sub2}$$

$$1.266V_X = 0.07V$$

$$V_X = 0.05529V$$

$$I_{sub} = I_{off} 10^{-0.9447}$$

$$I_{sub} = 0.1135 I_{off}$$

If I have a $V_{dd} - V_t$ on one side and then 2 stack transistor and then a ground then this V_X value turns out to be slightly lower. The reason is the subthreshold leakage current is slightly lower than our 0.01199 I_{off}, when the two transistors were stacked on one side it was the real voltage of V_{dd}, on the other side it was ground, because of the third transistor we are having this particular node as $V_{dd} - V_t$. In that sense because of the slightly lower voltage here, my current is slightly decreased from 0.1199 it is been decreased to 0.1135 also makes sense, because the voltage is slightly less and thereby the current should be slightly less. My sub threshold leakage current for the two stack transistors, if I see a rail

if I see a voltage of $V_{dd} - V_t$ on one side and the ground on the other side I will get 0.1135 of the I_{off} current.