Design and Analysis of VLSI Subsystems
Dr. Madhav Rao
Department of Electronics and Communication Engineering
International Institute of Information Technology, Bangalore

Lecture - 66
Energy expression in terms of delay

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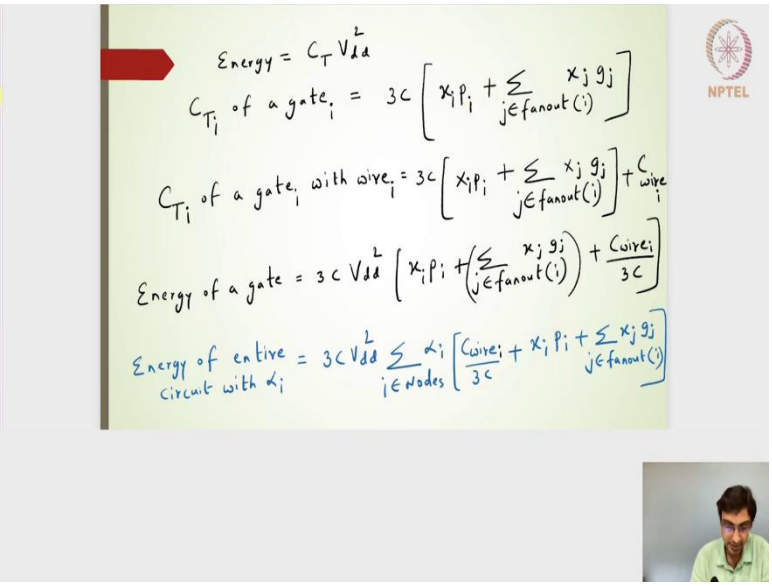

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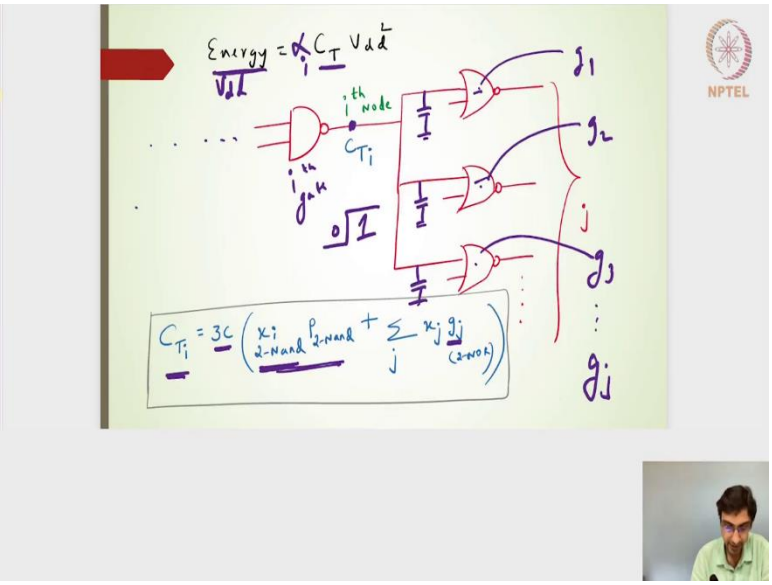

We had actually left in this particular slide and showcasing that the total capacitance can be identified using the driving factor. If the driving factor is mentioned in the gate design

or we can evaluate the driving factor. Then driving factor multiplied by the parasitics multiplied by 3C should be should given us the overall absolute parasitic capacitance.

The driving factor multiplied by the logical effort should be able to give us the input capacitance and of course, multiplied by 3C should be able to give us the absolute input capacitance coming from the next or the subsequent stages alright.

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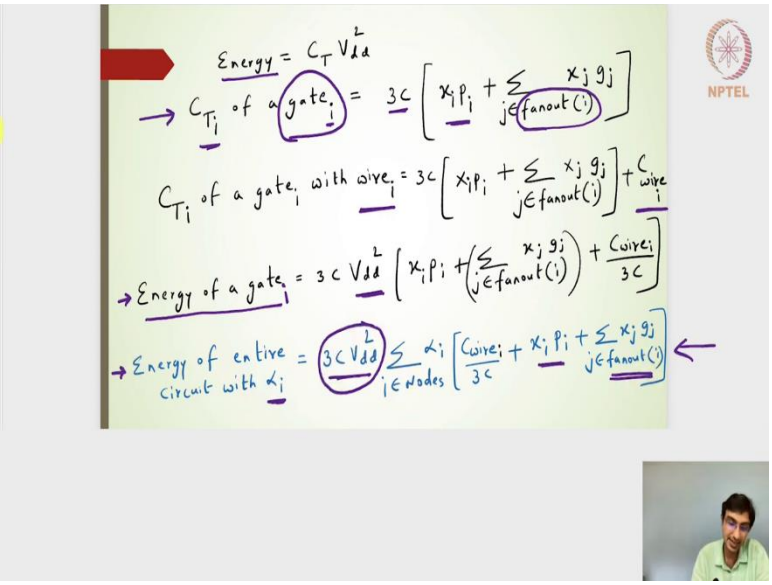

Taking this particular thing forward, let us say that the energy term. The energy is nothing but,

$$\text{Energy} = C_T V_{dd}^2$$

If I am considering about the particular gate$_i$, let us say I have a higher order circuit or a large amount of circuit you know its a higher order digital design.

In that particular design there are lot of gates and there are a lot of nodes which is nothing but the output of the gates. If I pick the i^{th} node or the i^{th} gate, the output of that particular gate i can be represented in the form, of the driving factor multiplied by the normalized parasitic factor will give me the parasitic capacitance. Then if it is kind of branched, if it has multiple branches based on the fan out value, also it could be fan out of i could be 4 5 or whatever the number of branches it can have. Based on that the input capacitance coming from the different branches and then getting accumulated at that particular node i

could be stated in the form of the driving factor multiplied by the logical effort. Of course, it has to be multiplied by 3 C. So, as to give us the absolute value.

$$C_{Ti} \text{ of a gate}_i = 3C[x_i p_i + \sum_{j \in fanout(i)} x_i g_j]$$

This being particular expression gives us the total capacitance at the output of the $gate_i$. Now, if I incorporate the wire capacitance also, the gate i is connected through the gate i + 1 with an interconnect or a wire then I need to accommodate the wire capacitance also. That is what is accommodated in this second expression. The C wire of i represents the output of the $gate_i$ that is been connected to the next gate.

$$C_{Ti} \text{ of a gate}_i \text{ with wire}_i = 3C[x_i p_i + \sum_{j \in fanout(i)} x_i g_j] + C_{wirei}$$

Finally, if I want to find out the energy of that particular $gate_i$ or the output node of the $gate_i$, then it will be multiplied by V_{dd}^2. The $3CV_{dd}^2$ and then we have this particular expression gives us the input capacitance of the subsequent stage and then this one will give us the wire capacitance.

$$\text{Energy of a gate}_i = 3CV_{dd}^2[x_i p_i + \sum_{j \in fanout(i)} x_i g_j + \frac{C_{wirei}}{3C}]$$

Now, if I want to find out the energy of the entire circuit, the entire circuit will be nothing but,

$$\text{Energy of entire circuit with } \alpha_i = 3CV_{dd}^2 \sum_{i \in Nodes} \alpha_i \, [x_i p_i + \sum_{j \in fanout(i)} x_i g_j + \frac{C_{wirei}}{3C}]$$

This particular expression talks only about the energy of the $gate_i$. Here if I want to find out the energy of the entire circuit, with the activity factor at each of the output nodes, at each of the output of the gates that has been there in the entire circuit.

In that case I need to accommodate the alpha also in that case it will be $3CV_{dd}^2$ and then there will be a summation to accommodate all the nodes in the circuit. Within this particular summation I will have an activity factor, that will be the activity factor of the individual gate outputs. The α_i and then multiplied by the entire capacitance will be nothing

but $\frac{C_{wirei}}{3C}$ plus the parasitic at that particular node i and then the input capacitance that has been reflected at the node i, due to the number of branches we have.

In that sense I will have this particular expression as the energy of the entire circuit accommodating the α_i. Now if I can easily modify, I can easily normalize this energy term by taking it out $3CV_{dd}^2$, because I know that could be a constant. I can actually divide it by $3CV_{dd}^2$ and then this becomes a normalized energy and that is what we have in the next slide.

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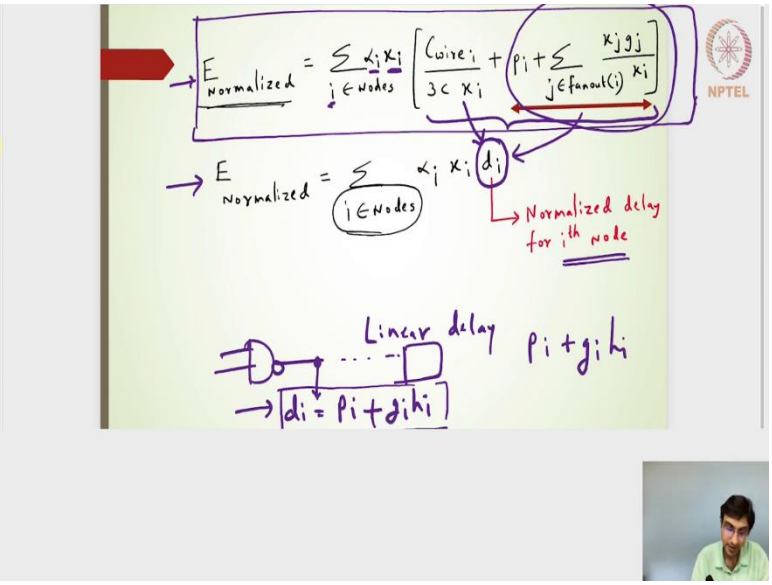

The E normalized, if you identify the E normalized value then multiplied by $3CV_{dd}^2$ will give me the absolute energy. To have an expression of E normalized, I will take away the $3CV_{dd}^2$ and then the remaining expression is nothing but the E normalized expression. Which is nothing but the energy of the V_{dd} energy delivered by the V_{dd} and that is normalized.

$$E_{normalized} = \sum_{i \in Nodes} \alpha_i x_i \left[\frac{C_{wirei}}{3Cx_i} + p_i + \sum_{j \in fanout(i)} \frac{x_i g_j}{x_i}\right]$$

Now, this particular expression is true for the whole circuit. Whole circuit having the i gates starting from the i covers, all the nodes of the circuit. Starting from the node number 1 to whatever number of nodes the circuit will have and inside that each of this will have the parasitic capacitance and then the input capacitance.

In this particular case what I have taken out is α_i anyways it is out of this particular expression and I have also taken out x_i value which is the driving factor of the i^{th} gate. It is the driving factor of the i_{th} gate and that has been taken out. In that sense I will have $\frac{C_{wirei}}{3Cx_i}$ because x_i is taken out.

Remember our linear delay expression says that it is p_i plus g_i h_i. If I consider the output of any particular two input NAND gate at this particular point, if it is connected to other circuits, other combinational circuits. At this particular point what we say is the delay of this particular gate will be nothing but di is nothing but parasitic of this particular gate, which is a two input NAND gate plus the logical effort g_i and h_i.

If I actually closely watch into this particular expression pi plus summation of $\frac{x_i g_j}{x_i}$ and I have stated this as nothing but the di expression. Somewhere our linear delay expression and then this particular expression, especially this particular expression should match alright. Although I have stated the wire capacitance here and I have directly in the next expression in this particular expression I have stated,

$$E_{normalized} = \sum_{i \in Nodes} \alpha_i x_i d_i$$

Although I have stated that $d_i = p_i + g_i h_i$. This should resemble the linear delay model, but the question is where is the $\frac{C_{wirei}}{3Cx_i}$ going? What it means is this di actually accommodates this wire capacitance or the delay due to this particular wire capacitance. That is also accommodated, so the entire thing is actually nothing but di.

But leaving aside the wire capacitances. The question is whether this $p_i + \sum_{j \in fanout(i)} \frac{x_i g_j}{x_i}$ whether it validates to our a linear delay model, which is nothing but $d_i = p_i + g_i h_i$.

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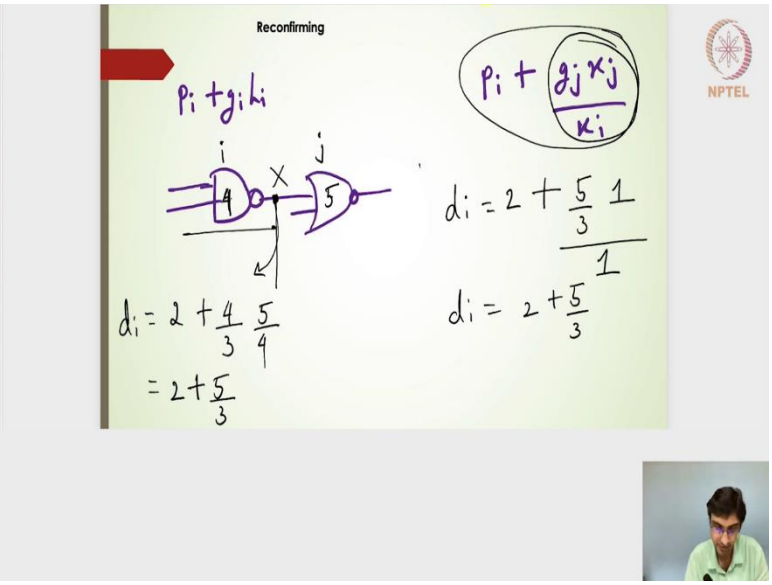

To have a look at it, let us rewrite the both the expressions. One expression says that it is nothing but the $p_i + g_i h_i$. Another expression says that it is nothing but $p_i + \frac{g_i x_i}{x_i}$. If I have only one branch I can take out the summation term.

If I have multiple branches this summation term it should be there. Now, let us take a very simple example. Let us say that I have a NAND gate and I have a NOR gate. A two input NOR I can have multiple of them, but just for a simple example let us try this. If I want to find out the delay for this particular term that means, this particular output node.

The delay for this particular output node will be using this linear delay model $p_i + g_i h_i$ will be nothing but 2 plus this is a 2-input NAND gate. It will be $\frac{4}{3}$ and hi is nothing but the electrical effort or the fan out. I need to have some kind of the input capacitance here and then the input capacitance of this. In that sense if I know the input capacitance here. Let me consider some value here 4 and 5 which gives us the driving factor of one, but in both the cases.

$$d_i = 2 + \frac{4}{3}\frac{5}{4}$$

$$= 2 + \frac{5}{3}$$

If I consider the same circuit for our new expression of delay. It will be nothing but for the same output node, let us say this is the x output node. The delay di from this new expression turns out to be pi which is nothing but,

$$d_i = 2 + \frac{5}{\frac{3}{1}}$$

$$= 2 + \frac{5}{3}$$

In this previous expression. Let me go back to the previous expression. What I said was this particular energy term now, actually is turned out to be a function of the delay di. The energy normalized term is now a function of the delay at the i^{th} node and in this particular circuit let us say we have a lot of nodes then we need to estimate the delay at the output of all the nodes and then use that for our energy estimation.

Hope this is clear. Now, if I look into this particular expression of $p_i + \frac{g_i x_i}{x_i}$ it is a very interesting expression. Now, the question is inherently the question is why is this driving factor this particular expression which we use the driving factor which we used for the energy expression is ultimately converted into a delay expression. The reason is this particular portion of $g_j x_j$. If I look into this particular portion, let me use another slide.

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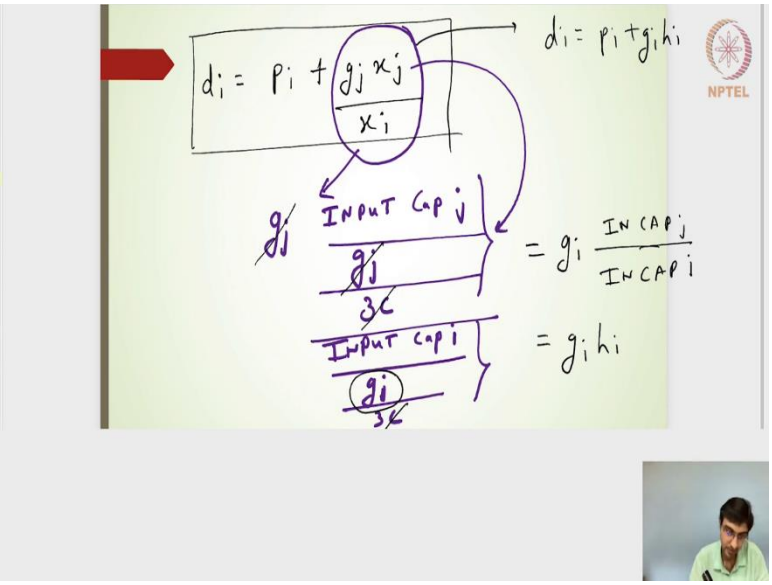

What we were telling is what we are talking about is the delay expression which is nothing but the new expression of delay which is,

$$d_i = p_i + \frac{g_i x_i}{x_i}$$

If I closely look into this particular expression and if I want to evaluate this, let us say what is the I mean by substituting the definition of the driving factors. I will have the logical effort g_j. The definition of x_j is nothing but the input capacitance of the j^{th} node divided by the logical effort of the jth node and then divided by 3C.

$$= \frac{g_j \dfrac{\text{Input cap j}/g_j}{3C}}{\dfrac{\text{Input cap i}/g_i}{3C}} = g_i \text{ Input capj/Input cap i } = g_i h_i$$

The delay term is nothing but this particular expression is nothing but d_i it turns out to be nothing but $p_i + g_i h_i$.

It turns out to be the same as nothing but the linear delay model. The only thing is because we are using the driving factor expression. If we have the driving factor of a gate already available with us then we can go ahead with this particular delay model, hope this is clear both these delays are the same.

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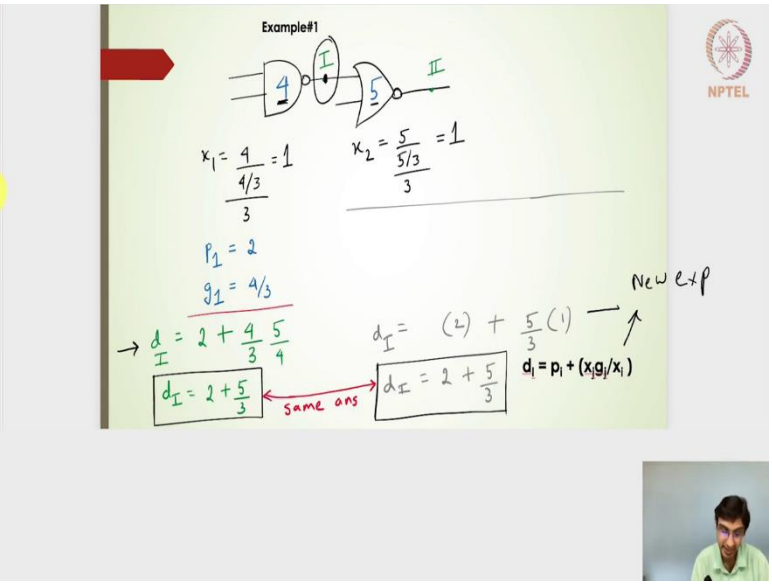

Moving ahead let us take an example here. Let us say that I have an NAND gate of the gate size of 4 and a gate size of 5. Let us take an example where I need to find out the delay of this particular node.

$$x_1 = \frac{\frac{4}{4}}{\frac{3}{3}} = 1$$

$$x_2 = \frac{\frac{5}{5}}{\frac{3}{3}} = 1$$

$$P_1 = 2$$

$$g_1 = \frac{4}{3}$$

Using the linear delay expression that is what we had seen earlier is nothing but,

$$d_I = 2 + \frac{4}{3}\frac{5}{4}$$

$$d_I = 2 + \frac{5}{3}$$

This is our new expression using the driving factor. The $p_i + \frac{g_i x_i}{x_i}$. It turns out to be nothing but,

$$d_I = 2 + \frac{5}{3}$$

It is the same example which we had seen in the previous slide.

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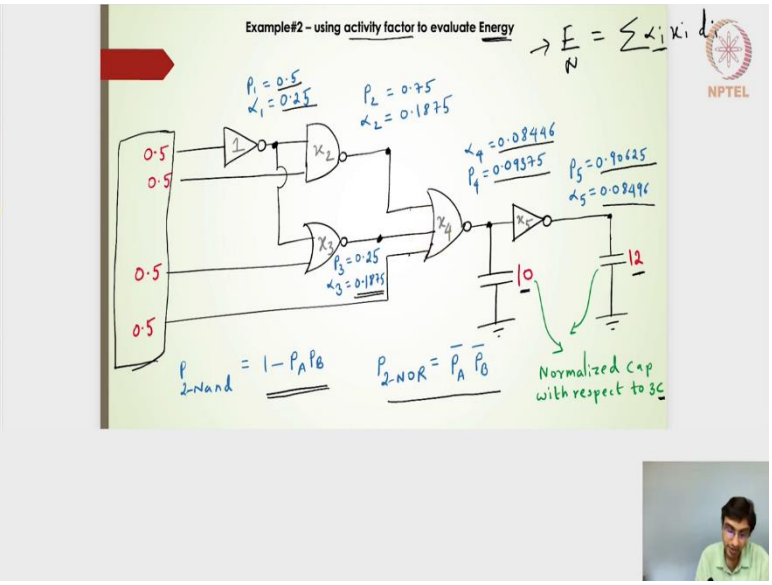

Moving ahead let us take a bigger example. Let us try to evaluate the energy in terms of the activity factor. Let us try to evaluate the energy. What it means is if I want to find out the normalized energy term, it will be nothing but,

$$E_N = \sum \alpha_i x_i d_i$$

That is one way of doing it the other way of doing it is finding out the capacitances at each of this nodes, at each of the output nodes multiply with that of the activity factor.

Of course, once you have all those things all the capacitance multiplied with that of the activity factor do the summation for all the output nodes and then multiply with that of the V_{dd}^2. That will give me the average energy delivered by the V_{dd}. Let us try to do employ both the methods and try to find out the expressions and whether try it and try to validate whether both the expressions are same.

In this particular case, let us try to understand this particular circuit at this point of time. We have the probability, the input probabilities is given as 50% of 0.5. All the inputs A B C D are having the probability of 0.5 meaning that the inputs having a logic 1 is having a probability of 50% and that is means fed to the gates.

The inverter output and its probability being 1 turns out to be nothing but 0.5. I should be able to find out the activity factor which is nothing about 0.5 multiplied by the complement

of $p_1 = 0.5$, $\alpha_1 = 0.25$, let us try to find out the activity factor of this particular gate at the second gate which is nothing but having a driving factor of x_2. Remember that in this particular example the driving factors are mentioned in the along with the gates.

The A value of 1 here represents it is the driving factor of 1, x_2 is the driving factor of this 2-input NAND gate, x_3 is the driving factor of this 2-input NOR gate x_4 is the driving factor of this 3-input NOR gate and then on the capacitance of 10 and 12 are used, what it really means is it is nothing but the normalized capacitance with respect to the 3 C. So, the absolute value of these capacitances will be 10 x 3C or 12 x 3C, where 1C is represents the 1 NMOS unit NMOS transistors capacitance.

If I actually want to find out the activity factor of individual nodes. Let us try to evaluate the activity factor of this output of the 2-input NAND gate where the driving factor is x_2. We need to find out the probability at the output of this 2-input NAND gate, one probability is 0.5 here the other probability is coming from the input 0.5. The probability at the output of the 2-input NAND gate is given by $1 - P_A P_B$. I will have 1 - 0.5 x 0.5 = 0.75.

My activity factor will be 0.75 x 0.25 = 0.1875, NOR gate if I want to find out the activity factor of this I know what is the probability coming at the input side and the probability coming on the other input. The probability at the output of the two input NOR gate is given by this particular expression. It turns out to be nothing but $\overline{P_A}$ which is 0.5 multiplied by $\overline{P_B}$ is 0.25 and its activity factor will be nothing but point 0.1875.

For a 3-input NOR gate the output expression for a 3-input NOR gate will be very very similar to the 2-input NOR gate, it will be nothing but $\overline{P_A}$, $\overline{P_B}$, $\overline{P_c}$ and we know the probability of individual inputs here going to the 3-input NOR gate which is nothing but 0.75, 0.25 and 0.5. Its complement will be 0.25, it is complement to be 0.75, its complement will be 0.5 and if I do the multiplication I should be able to establish P_4 = 0.09375 and the activity factor at the output of this 3-input NOR gate turns out to be 0.08446 and once I have the probability here, I should be able to find out the probability at the output of this inverter, which is also the final output of this particular circuit. Turns out to be nothing but the complement of this because it is an inverter logic. I will have 0.90625 and its activity factor will be nothing but the same as this one 0.08496.

Now, that I have the activity factor I can actually use any of these energy expressions. One expression is going ahead with that delay expression, the another one is estimating the capacitances using the driving factors, estimating the overall capacitances at this particular output node by calculating the parasitic capacitances here the input capacitances coming from the subsequent gates and then multiplying with the activity factor, doing the summation for all the nodes and then multiplying with that of the V_{dd}^2.

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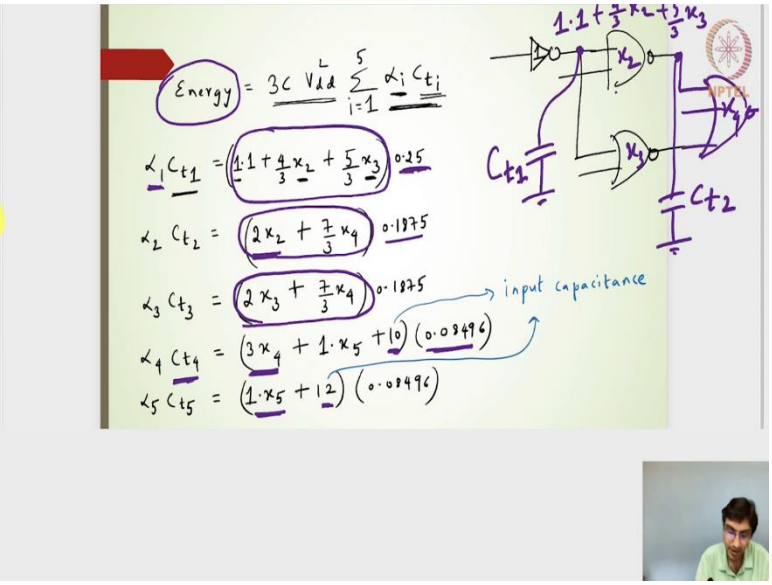

Let us do that, the first method we will use is the evaluating the capacitances at each of the nodes and we have 5 nodes here.

$$\text{Energy} = 3CV_{dd}^2 \sum_{i=1}^{5} \alpha_i C_{ti}$$

If I do that let us start doing that, the C_{t1} the total capacitance at the output of the node 1 using the driving factor is,

$$\alpha_1 C_{t1} = \left(1.1 + \frac{4}{3}x_2 + \frac{5}{3}x_3\right) 0.25$$

Similarly, I can actually estimate the overall capacitance and then multiply with the activity factor. For alpha $\alpha_2 C_{t2}$, the total capacitance seen at the node 2 which is nothing but this one,

$$\alpha_2 C_{t2} = \left(2x_2 + \frac{7}{3}x_4\right)0.1875$$

$$\alpha_3 C_{t3} = \left(2x_3 + \frac{7}{3}x_4\right)0.1875$$

$$\alpha_4 C_{t4} = (3x_4 + 1x_5 + 10)0.08496$$

$$\alpha_5 C_{t5} = (1x_5 + 12)0.08496$$

Now, I have estimated all the α into capacitance that means, I have estimated the activity factor, the product of the activity factor and then the total capacitance seen at the individual nodes. We can add it together up and then multiply by $3CV_{dd}^2$ should be able to give me the energy delivered by the V_{dd} and that is an average energy delivered by the V_{dd} per clock cycle.

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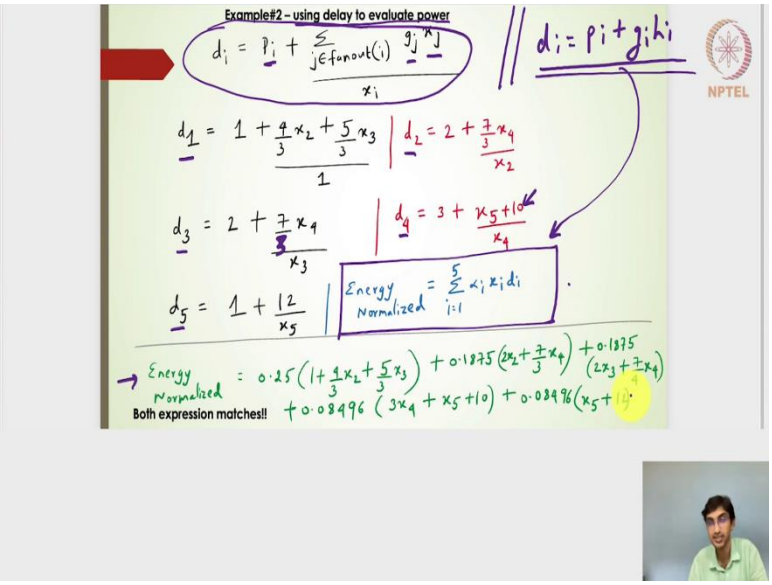

If I use a different method, if I use a delay method remember that we had evaluated the energy expression in terms of energy expression as a function of delay. If I use that, if I find out the delay at each of the output nodes and then use that in our alpha i xi di expression for 5 nodes. Whether my expression calculated the energy expression from this particular method will resemble to the one which we had calculated in the previous slide.

For doing that I need to find out the delay at each of the nodes. The d_1, d_2, d_3, d_4 and the delay expression says that is nothing but,

$$d_i = P_i + \frac{\sum_{j \in fanout(i)} g_j x_j}{x_i}$$

It is nothing but the logical effort of the next stage multiplied by the driving factor of the next stage divided by the driving factor of the previous stage. We can also actually calculate the delay using the linear delay model with $P_i + g_i h_i$ and then that also can be accommodated into our energy expression.

In this particular case, I have taken this particular expressions because we have anyways derived it. It will also become a good example for us or a good exercise for us to solve this using this new expression, because we are anyways adapted or used to this particular expression. Why not use this particular expression and see that and then apply that for our energy expression.

One could actually use this expression also, if I use this particular delay expression, the d1 will be nothing but the inverter, the first gate is the inverter. The parasitic of one and then we have the g_j and x_j of the subsequent stages, wherever it is kind of branch. Remember that the output of the inverter is kind of branch 2, the 2 gates one is a 2-input NAND gate and another one is a 2-input NOR gate.

$$d_1 = 1 + \frac{\frac{4}{3}x_2 + \frac{5}{3}x_3}{1}$$

d_2 the delay of the output of the 2-input NAND gate which is nothing but,

$$d_2 = 2 + \frac{\frac{7}{3}x_4}{x_2}$$

Similarly, d_3 I will have a similar expression,

$$d_3 = 2 + \frac{\frac{7}{3}x_4}{x_3}$$

The 3-input NOR gate and its output and then I want to find out the delay or at the output of that 3-input NOR gate is nothing but,

$$d_4 = 3 + \frac{x_5 + 10}{x_4}$$

Finally, I will have the parasitic the output of the last stage which is again an inverter,

$$d_5 = 1 + \frac{12}{x_5}$$

If I use this particular delay expression and put it into an energy expression, then I am going to get this particular expression.

$$\text{Energy}_{\text{normalized}} = 0.25\left(1 + \frac{\frac{4}{3}x_2 + \frac{5}{3}x_3}{1}\right) + 0.1875\left(2 + \frac{\frac{7}{3}x_4}{x_2}\right) + 0.1875\left(2 + \frac{\frac{7}{3}x_4}{x_3}\right) + 0.08496\left(3 + \frac{x_5 + 10}{x_4}\right) + 0.08496\left(1 + \frac{12}{x_5}\right)$$

Turns out that both the expression which we calculated earlier in the previous slide and this particular expression turns out to be the same.