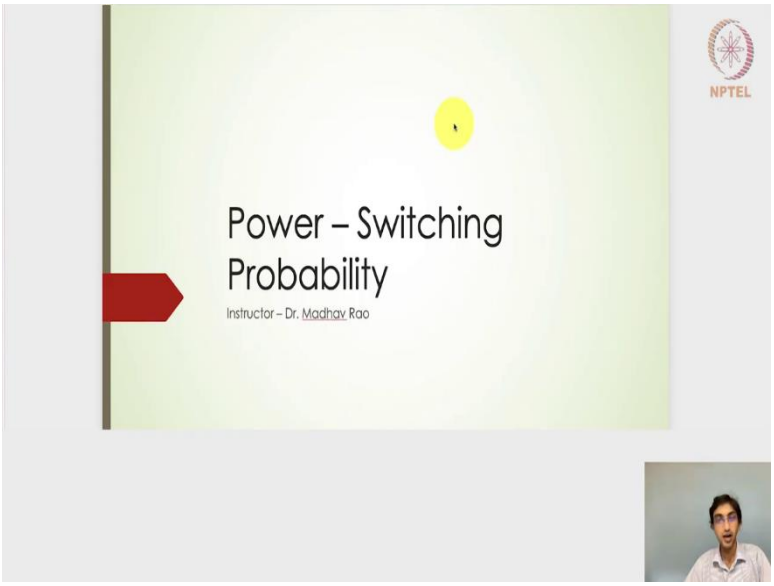
Design and Analysis of VLSI Subsystems
Dr. Madhav Rao
Department of Electronics and Communication Engineering
International Institute of Information Technology, Bangalore

Lecture - 63
Activity factor and estimating dynamic power for a combinational circuit design

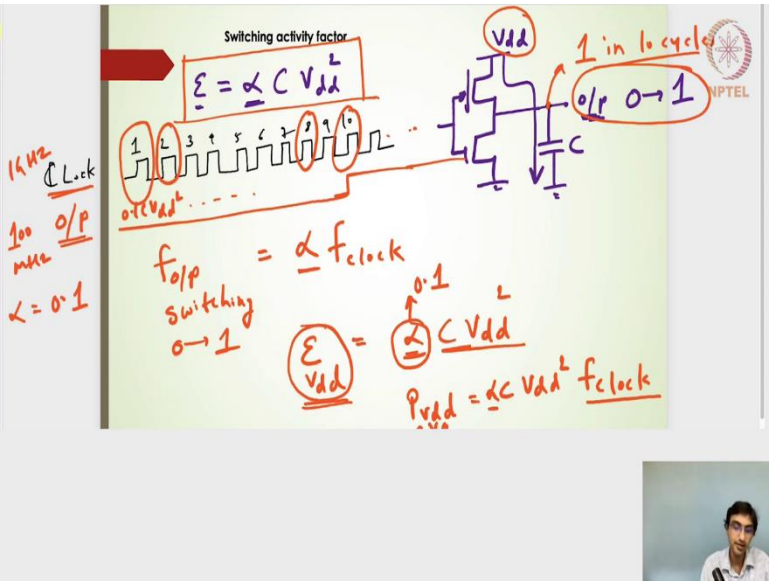
(Refer Slide Time: 00:16)



Hello students. Welcome to this lecture on the topic of power and in this particular lecture we will look at more in depth analysis on the switching probability and arrive at is the switching activity factor, which will be useful in estimating the overall power of the larger digital circuit.

What we will do is first is try to understand the activity factor and then try to establish a kind of a relationship between the activity factor and then the logical gate. If I have a logical gate then what should be the activity factor of that particular logical gate and then apply that particular activity factor to estimate the one set of example consisting of the digital logic gates. Then we will also try to estimate the power, the switching power or the dynamic power estimation using two different kinds of an architecture.

(Refer Slide Time: 01:22)



To start with, this is an empty slide what it means is I have to draw something, what I have stated in this particular slide is a switching activity factor. Let me try to summarize what we have learned so far. The energy which we had estimated was αCV_{dd}^2, where C is nothing but the total capacitance that is seen at that particular output node. If we can take a simple example of an inverter and the inputs are connected and then this particular output is this one.

The capacitance C is nothing but this particular capacitance, this could be the C load capacitance. Based on the input I will get the output to be switched and then this energy is nothing but coming from the V_{dd} rail. The energy delivered by the V_{dd} rail is nothing but the energy, this for the capacitor to get charged that means, at the output to be doing the transition from 0 to 1. Now, this particular alpha value is actually coming from how many, I mean what is the frequency of the output node getting switched from 0 to 1.

This α is actually relating this output node, switching frequency with that of the clock frequency. Let me draw a simple example, if I have a clock frequency of let us say 1Ghz, I am going to draw 10 cycles. The 1Ghz means each time period will be nothing but 1 nanoseconds. This will be my clock 1, 2, 3, 4, 5, 6, 7, 8, 9, 10 and let me say that this is my clock, this is my clock signal.

Let us say that based on the input here the output is going to switch and the output is going to switch 1 in 10 cycles, I am just throwing an example here. The 1 in 10 cycles that means,

that the output of this particular inverter circuit, I am going to write it as an output and this is going to have 0 most of the times, only at the 10th cycle, 1 in 10 cycle I will have an output going high alright and then so on.

If I actually draw this continue this in the 20th cycle in between 10 to 20th cycle I will have this the output going high again. This is basically the output of the gate or in this particular case is an inverter output which is going from 0 to 1 or which is doing the transition from 0 to 1. If I actually can relate this particular output frequency with respect to the clock frequency. If I say that this is my output frequency or you can also call it as nothing but the switching frequency from 0 to 1.

The number of transition is just from 0 to 1. That the capacitor has to be charged that is when the V_{dd} will deliver the energy of the CV_{dd}^2. If this frequency can be related in terms of alpha with respect to the clock frequency. In this particular case I have the clock frequency set to 1Ghz and then the output is doing the frequency in 1 into every 10 clock cycle. That means, the output frequency should be somewhere around 1 by 10th of the clock frequency.

I will write it as 100Mhz, the clock frequency is set to 1Ghz, let us say my alpha in this particular case will be nothing but 0.1. In that particular case, if I have an α characterized or calibrated for this particular circuit in my chip. Where the output node is doing the transition from 0 to 1 for every 10 clock cycles it is doing the transition of 0 to 1 once. In every 20 clock cycles I will have the transition from 0 to 1, 2 times and then so on.

I can have my α related like this, the overall energy. This particular energy term here is nothing but the energy delivered by the V_{dd}, I am writing it as αCV_{dd}^2. What it says is, it is nothing but the average energy that has been delivered, the energy delivered for one transition at the output node from and doing the transition from 0 to 1 will be nothing but CV_{dd}^2.

This α for this particular circuit which is calibrated to have a value of 0.1, what it implies is if I consider one clock cycle, the average energy that is being delivered by V_{dd} is 0.1 CV_{dd}^2. The energy delivered in the 2nd clock cycle is 0.1 CV_{dd}^2, the energy delivered in the 8th clock cycle it is 0.1 CV_{dd}^2, 9 clock cycle it is 0.1 CV_{dd}^2, 10th clock cycle it is 0.1 CV_{dd}^2.

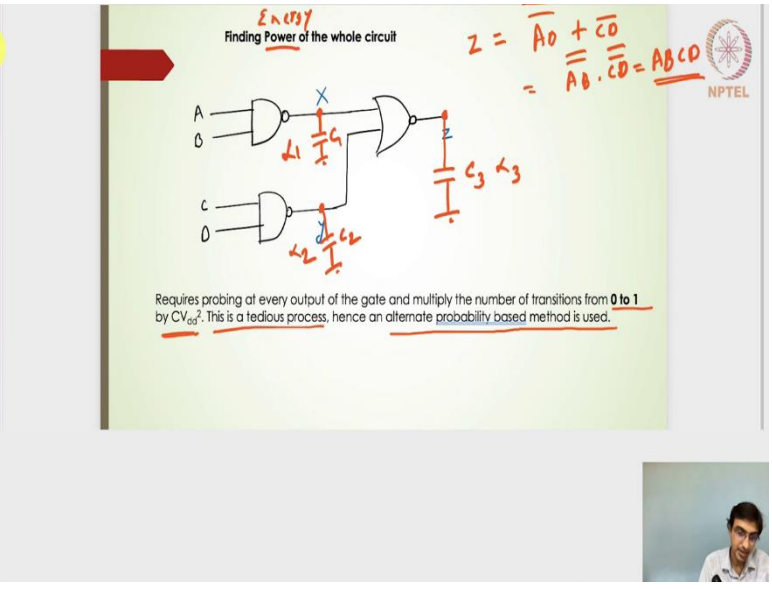
From the clock cycle of 1 to 10 the overall energy that has been delivered by the V_{dd} turns out to be $0.1CV_{dd}^2$ which is nothing but CV_{dd}^2. What it does is this particular energy term is nothing but the average energy delivered by the V_{dd} for 1 clock cycle, that is where this alpha is coming. In the sense alpha is nothing but it shows an average energy that has been delivered by the $V_{dd}\alpha$ is also used to find out the power.

The power delivered by the V_{dd}, it can be is nothing but CV_{dd}^2 and then α here and then I will write the clock, it is nothing but the $CV_{dd}^2 f_{sw}$ or the f output, instead of f switching I can write it as fα clock alright. This will give me the instantaneous power that has been delivered by the V_{dd} or rather it can give me the average instantaneous power that has been delivered by the V_{dd}.

Across this particular clock cycles, at any point of time I will get an average value of the power as nothing but $\alpha CV_{dd}^2 f_{clock}$. In this particular case α=0.1 that means, that the output node is switching actually 10 percent of the clock frequency. We actually want α to be actually be lower and lower.

If it is lower and lower, the overall energy that has been delivered by the V_{dd} will be less and the overall energy that is consumed by the circuit or delivered by the V_{dd} rail in our design will be actually be less.

(Refer Slide Time: 08:37)



Let us take an example here. I am saying that let us try to find out a power or whatever energy. I can say that, if I can find out the average energy that is delivered by the V_{dd} rail and if I can get that $\alpha C V_{dd}^2 f_{clock}$ will give me the average power. In this particular case, I have got this particular circuit and let us see what is the logical output of this particular circuit given the input A B C D.

Here the $X = \overline{AB}$, $Y = \overline{CD}$ and then the NOR of it.

$$Z = \overline{\overline{AB} + \overline{CD}} = \overline{\overline{AB}}.\overline{\overline{CD}} = ABCD$$

This is the logical expression for this particular circuit. Now, if I want to actually find out the overall average energy of the overall circuit, then I actually need to probe the energy here, I need to probe the energy here, I need to probe the energy here. Assuming I will have the parasitic capacitance, here I need to find out what is the capacitance, the total capacitance here, which we can find it out if I know the input capacitance based on the width of this particular gates.

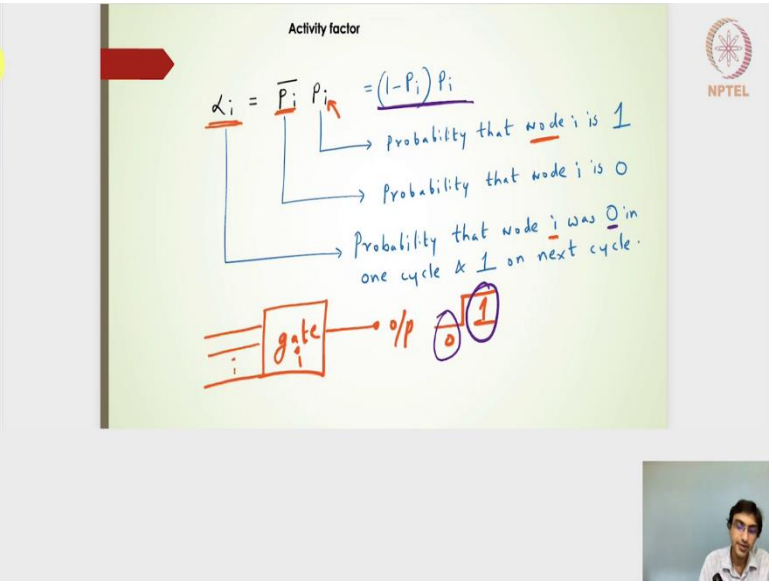
Similarly, here I should be able to find out the overall capacitance here based on the width of this particular gate and assuming that this is not loaded, we do not have any kind of a load connected to this particular output. If it is floating we will have only the parasitic capacitance of this particular gate, knowing C_1, C_2 and C_3, I should be able to find out what is the capacitances is known, but I need to also find out what is α_1, α_2 and α_3 here.

For finding out the activity factor, it requires the probing at every output of the gate and multiply the number of transitions from 0 to 1 by the CV_{dd}^2. If I have to do $C_1 V_{dd}^2 \alpha_1$, I can only find it out if I know the f_x switching frequency of f_x output node, switching frequency of the y output node, switching frequency of the z output node and then related to that of the clock frequency. Then I should be able to find out α_1, α_2, and α_3 here and then put it across that particular equivalent capacitance and then find out the overall energy at each of this node. But this is a very tedious process now. What is the tedious process? finding the number of transitions at individual nodes is a very tedious process. Hence an alternate probabilistic base method is used.

If I have a larger circuit, it is only 3 gates here. If I have millions of gates, if I have 10^6 or 10^9 such gates or the transistors forming the gates then I need to probe at each every each and every point. Probing at each and every point of the gates and then evaluating the

switching the transitions or the switching or the activity factor each of the output nodes becomes a very tedious process and is to avoid that what we will do is go to the probabilistic method.

(Refer Slide Time: 12:08)



Let us see what is that probabilistic method. The probabilistic method says that all the logic gates have a logic functionality. Whether it is a NAND gate or a NOR gate or whatever other gates combinatorial circuits, if there is a logical expression. We can actually write the output in terms of the input and the activity factor at each of the outputs of this logic gates can be defined as nothing but the conditional probability where it includes two probabilities.

One is the probability of it being the output of the gate being 1, the other probability is that the probability that the output node i is equal to 0. What it says is it is nothing but,

$$\alpha_i = \bar{P}_i P_i$$

The probability that the node i for a gate i. Let us say that I have an gate here there are millions of gates. If I pick one of this case, this I will say that this is the gate i, whatever its a number of inputs here and here this will be the output, there could be multiple outputs I will pick one of the outputs and this particular output node is doing the transition from 0 to 1. What it means is I need that particular output node being at 0 in the previous clock

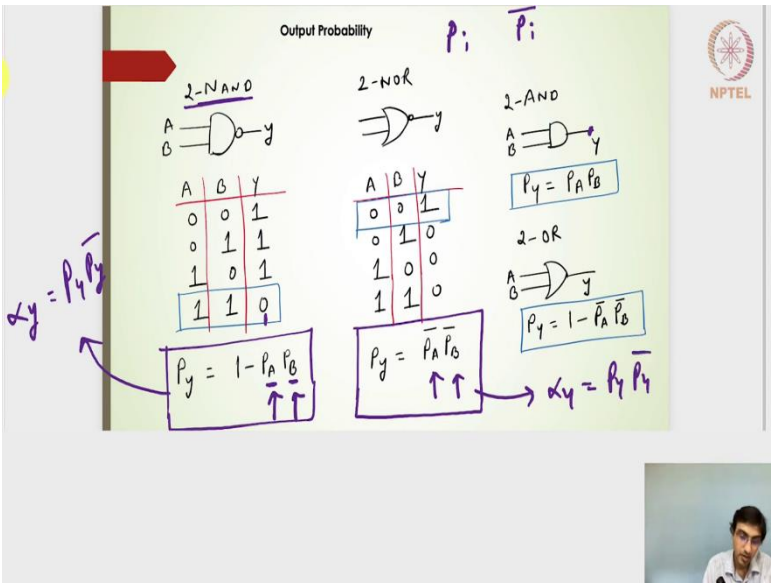
cycle and being at 1 in the next clock cycle. In 1 clock cycle in the previous clock cycle it should be 0 and in the next clock cycle it is 1.

That is why it is P_i the probability of that particular gate output or the node to be at 1 and $\overline{P_i}$ is nothing but the probability that the gate output node is at 0. It is written as,

$$\alpha_i = (1 - P_i)P_i$$

This is by definition activity factor and it is a very theoretical approach, which helps us to do a rough calculation of the overall power estimation or the energy estimation of the overall higher order digital circuit.

(Refer Slide Time: 14:25)



Moving ahead, now what is this probability? What is this P_i? how do I calculate P_i? Then if I calculate P_i I should be able to find out what is $\overline{P_i}$. Let us take up a 2 input NAND gate. I have 2 inputs to the NAND gate and then the output is y. If I do input NAND gates there I can form the truth table. If it is 0 0 I will have 1, if it is 0 1 I will have 1, if it is 1 0 I will have 1, if it is 1 1 I will have 0.

In this case if I take this particular lasts input combination 1 1, giving an output of 0, I can write my probability for this particular logic gate which is a 2 input NAND gate as,

$$P_y = 1 - P_A P_B$$

This is 0, that is why it is 1 and then what is the input probability it is being 1, that is why $P_A P_B$ alright. The output of this NAND gate given, the input probability of A and B, I should be able to find out what is the output probability of this the output node being at 1. Based on the input I know input probability being at 1, I should be able to find out the output probability this is the output of the 2 input NAND gate being at 1. The probability the output of the 2 input NAND gate being at 1, I should be able to evaluate based on the inputs being at the probability of the inputs being at 1. It will be $P_y = 1 - P_A P_B$.

Let us take a look at the 2 input NOR gate. For the 2 input NOR gate based on the input combinations again we will have 4 combinations, all of them are 0 except the first combination which is where the input are 0 and 0, I will get a 1. This the output node y being at 1 is nothing but,

$$P_y = \overline{P_A}.\overline{P_B}$$

P_A will give me the output being, the input of this particular 2 input NOR gate being at 1 and P_B will give me the input the other input being at 1, but we need 0 and 0, that is why it is the $\overline{P_A}.\overline{P_B}$.

Now I have the output probability of the two input NAND gate and the output probability of the two input NOR gate given the input probabilities. Input probabilities means P_A $\overline{P_B}$ is given, then I should be able to find out the output node probability, especially for the 2 input NAND gate and 2 input NOR gate.

Let us take a look at the other standard gates, in this case 2 input AND gate and 2 input OR gate I have given, what I have mentioned here, based on the A and B I will get a y output for the 2 input AND gate is nothing but,

$$P_y = P_A P_B$$

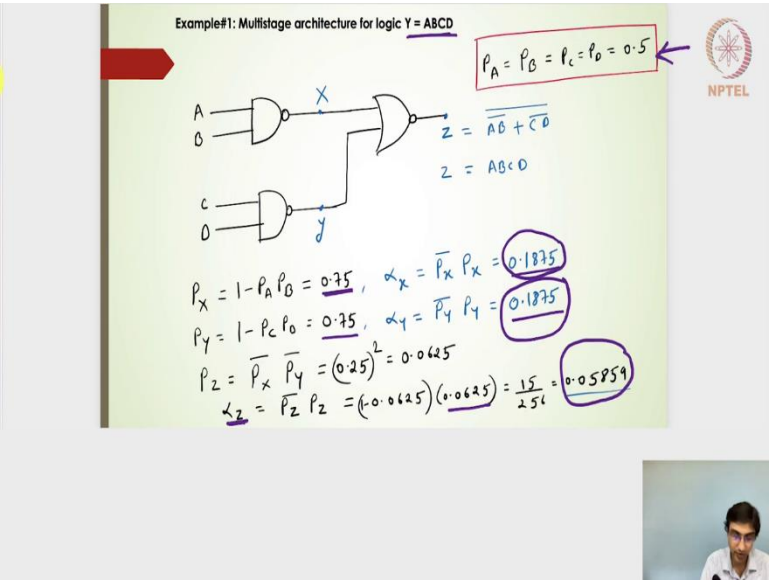
Similarly for the 2 input OR gate will be nothing but,

$$P_y = 1 - \overline{P_A}.\overline{P_B}$$

In our next example, we will try to use these two probability nodes to find out the probability at the output node, the output not being at one I should be able to find out, if I have a two input NAND gate and if I have a two input NOR gate.

The output of the two input NOR gate being at 1 we should be able to evaluate using this particular expressions. The $1 - P_A P_B$, another one is $\overline{P_A}.\overline{P_B}$ and use this to find out what is the activity factor. If I want to find out the activity factor of the 2 input NAND gate, I should be able to use this and then find out saying that alpha activity factor is nothing but P_y and $\overline{P_y}$. For a 2 input OR gate, I should be able to find out the same thing $P_y\ \overline{P_y}$. This is what we had seen in the last slide, hope this is clear at this point of time.

(Refer Slide Time: 18:31)



Moving ahead let us take an example of this multi stage architecture design for the logic,

$$Y = ABCD$$

This is what we wanted this is where we are started from. We had a 2 input NAND gate in the single stage and then followed the output of that is going to the next stage of the 2 input NOR gate. So, that the $Z = ABCD$, let us say that the input probabilities are characterized and given to us saying that P_A, P_B, P_C, P_D = 0.5.

What it really means is the probability of this inputs whatever the 4 inputs are there that being at 1 is 50%, that being at 0 is also 50%. We are giving a kind of an equal distribution for the logic 0 as well as logic 1 input. If I consider that I should be able to evaluate the

probability at the x node, at the y node, at the z node and then find out what is the activity factor at x, y and z and then find out what is the overall energy delivered by the V_{dd} for 1 clock cycle.

I will say that it is an average energy that is being delivered by the V_{dd}. Once I have the energy I should be able to multiply that with that of the clock frequency and then find out the overall power or whatever the average power also called as the dynamic power. Hope this is clear at this particular point of time. Let us go ahead, let us proceed and then try to evaluate the probabilities at this particular nodes x y and z.

$$P_X = 1 - P_A P_B = 0.75$$

Where, P_A and P_B are 0.5,

$$\alpha_X = \bar{P_X} P_X = 0.1875$$

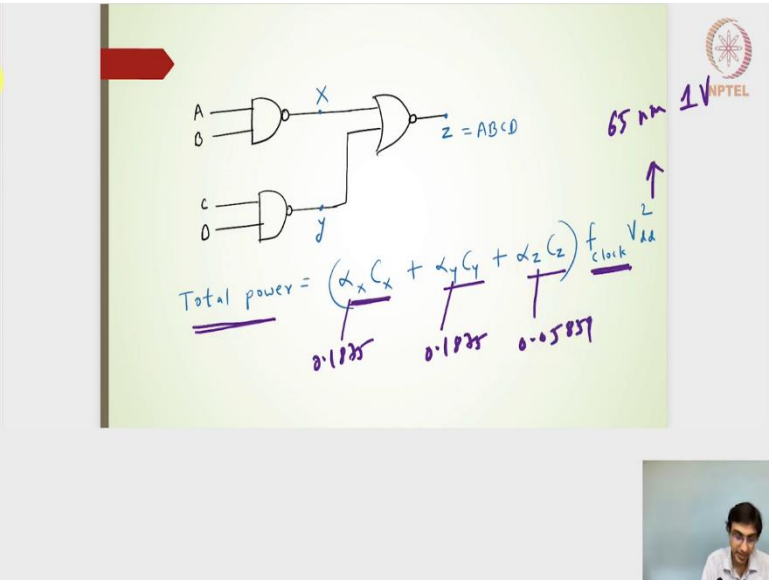
$$P_Y = 1 - P_C P_D = 0.75$$

$$\alpha_Y = \bar{P_Y} P_Y = 0.1875$$

$$P_Z = \bar{P_X}\bar{P_Y} = (0.25)^2 = 0.0625$$

$$\alpha_Z = \bar{P_Z} P_Z = (1 - 0.0625)(0.0625) = \frac{15}{256} = 0.05859$$

(Refer Slide Time: 21:55)



Moving ahead, the total power which will be nothing but if there is a power term I will just multiply the energy term with that of the f_{clock}. The total power will be nothing but alpha multiplied by the individual capacitances and then I have 3 output nodes. I will have the 3 such $\alpha\ f_{clock}V_{dd}^2$.

If I can consider this to be a 65nm technology node. I can have it as 1 volts, as a rail voltage. Now, I should be able to find out easily what is $\alpha_X = 0.1875$ and $\alpha_y = 0.1875$, $\alpha_Z = 0.05859$.

$$\text{Total Power} = (\alpha_X C_X + \alpha_Y C_Y + \alpha_Z C_Z) f_{clock} V_{dd}^2$$