Design and Analysis of VLSI Subsystems
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Lecture - 61
Introduction to Power

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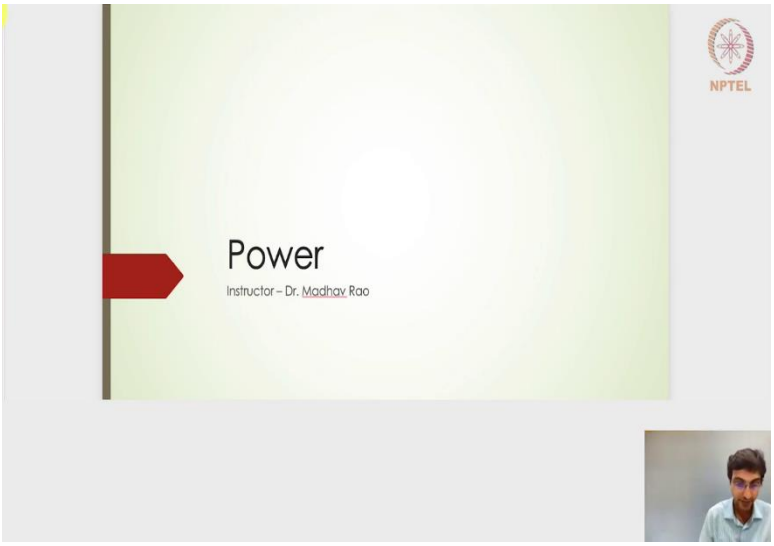

Hello students. Welcome to this lecture and in this particular lecture and then going forward in the lecture series we will do an in-depth analysis of the Power. Power for a circuits and the energy for the circuits especially for the digital circuits because anyways we are looking into the digital component in this particular course.

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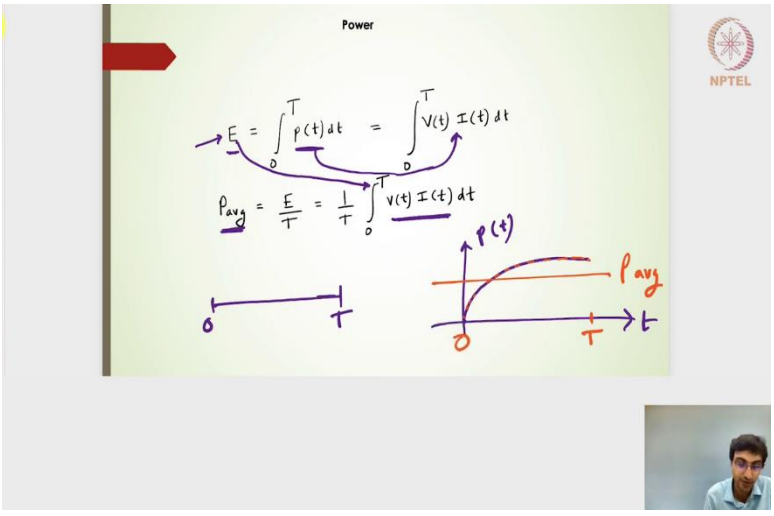

Let us begin further let us move further. Let me take my pointer as well. For the definition for the energy consumed by a particular component or by a particular circuit it is defined as nothing but the instantaneous power that has been consumed by the component or it is been dissipated by the component over a period of time or over a duration of time

It is basically an integral component. It is defined as energy that is consumed by the power or dissipated by the consumed by the component or the dissipated by the component is actually defined as an integral of the instantaneous power across the time duration. What it really means is if I have a discrete point of time then it is nothing but the summation of all the power across the time duration. That is why in an very analogous term we will consider it to be nothing but an integral component.

$$E = \int_0^T P(t)dt$$

Instantaneous power is actually defined in the form of,

$$E = \int_0^T V(t)I(t)dt$$

If this is the energy that has been defined or this is the energy that has been estimated for the component or for the circuit that is been designed by us over a time duration of T, then I can also estimate what is the overall average power for I know if this is particular energy for a duration of 0 to T.

That particular average power across the time domain of 0 to T can be given as nothing but,

$$P_{avg} = \frac{E}{T} = \frac{1}{T}\int_0^T V(t)I(t)dt$$

Remember that this P of t is an instantaneous power that is nothing but the power released or dissipated or consumed at that particular time instance and P average is nothing but whatever is the average power across this time duration of 0 to T. If I have the instantaneous power as something like this then this is my P of t across the time domain t, then I will have an average power which is nothing but an average of across all these points.

I will have somewhere like this. This might be my average power that is consumed or dissipated or released by that particular component over the time duration from 0 to T. Hope this particular first level definition of the power and energy is clear to everyone.

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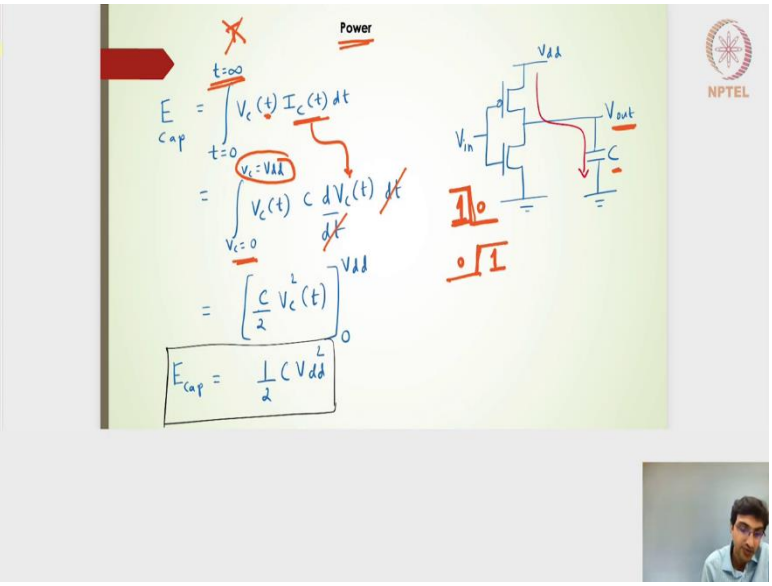

Going forward now, let us try to apply or extract the power parameters and then the energy parameters for our digital circuits. The most primitive digital circuit turns out to be the inverter, I have designed an inverter here with an input here and then a capacitance it could be a parasitic or it could be an input capacitance coming from the next stage. We can consider this to be nothing but a C value which is nothing but a load capacitance connected with a output node.

Now, I have drawn this particular an arrow showing that the capacitor is actually charging through the PMOS transistor and the we will say that the NMOS will be OFF considering the input is nothing but a step input 1 to 0 then I will have the PMOS to be ON, NMOS to be OFF, if I have the 1 to 0 or rather 0 to 1, I will have the NMOS to be ON and PMOS to be OFF and then the capacitor will be discharging.

For the capacitor to charge we will try to evaluate what is the energy that is being consumed by the capacitor, while it is actually charging and while it is starting, we know that for a step input we will have the PMOS to be ON and NMOS to be OFF. Thereby I will have the current going from V_{dd} and then through the PMOS and then charging the capacitance.

As per the definition the energy consumed by the capacitor or by the component in this case the capacitor is a component, we are interested in is nothing but for t is equal to 0 to infinite. I have taken the t is equal to infinite because we really do not know at what time the capacitor completely charges and after it is completely charged that we will not have any current. After it is completely charged the capacitor current will be 0, but till a point where it charges completely, we will have some kind nonzero current.

It is nothing but the energy, the energy for the capacitor to charge. The energy that is consumed or stored in the capacitor for it to be completely charged to V_{dd}. In that sense this definition is t is equal to 0 to infinite and not equal to t. That will not be there it will be nothing but infinite because this t value we really do not know.

In that case for the capacitor to completely charge or stored the energy it will be nothing but,

$$E_{cap} = \int_{t=0}^{t=\infty} V_c(t) I_c(t) dt$$

Where $V_c(t)$ is nothing but the instantaneous voltage across the capacitor which is nothing but the output voltage and $I_c(t)$ is nothing but the instantaneous current that will be flowing across the capacitor.

This will be it and if I consider $I_c(t)$ of the capacitor the current flowing along the capacitor will be nothing but,

$$E_{cap} = \int_{V_c=0}^{V_c=V_{dd}} V_c(t) C \frac{dV_c(t)}{dt} dt$$

For t is equal to 0, I know that the V_c is actually 0. We can assume that the capacitor is not at all charged and then based on this once it is 1 to 0 the step input is given, when the PMOS transistor turns on then only the capacitor starts charging. When the input is 1 we know that the output will be completely discharged to 0 and it will be holding a logic 0 in a steady state.

The moment the input does a transition from 1 to 0 we will have the PMOS transistor to be on and then will have the capacitor to be charging through the PMOS transistor. In that

sense we have the $V_c = 0$ and $t = 0$ and when $t = \infty$ we know that the Vc will be held at a steady state voltage of Vdd.

If I take that particular limit and now I have,

$$E_{cap} = \left[\frac{C}{2} V_c^2(t)\right]_0^{V_{dd}}$$

$$E_{cap} = \frac{1}{2} C V_{dd}^2$$

This particular energy is now stored in the capacitor while it is completely charged.

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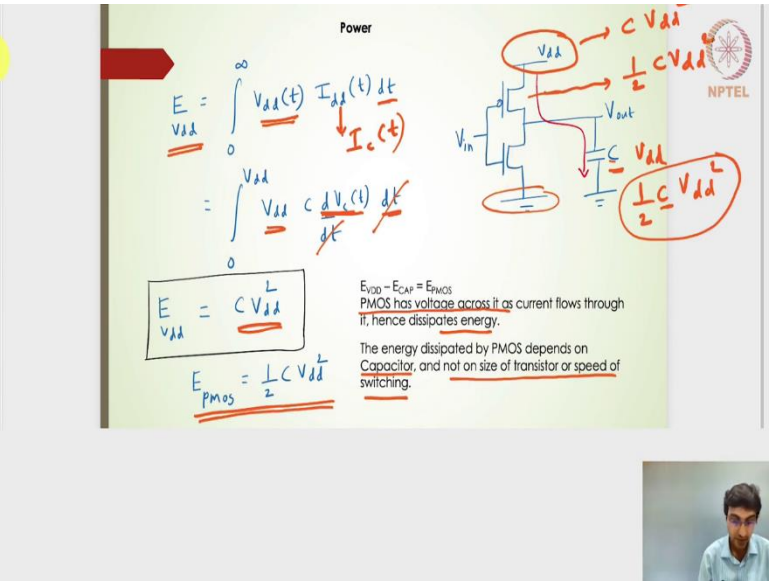

Very interesting to find out that what is actually the energy that will be delivered by the V_{dd} rail. Now, that is very interesting because the capacitor although it charges to V_{dd} the energy that it stores or it is consumes will be nothing but ½ C V_{dd}^2 square.

The energy delivered by the V_{dd} will be,

$$E_{V_{dd}} = \int_0^{\infty} V_{dd}(t) I_{dd}(t) dt$$

$$= \int_0^{V_{dd}} C \frac{dV_c(t)}{dt} dt$$

$$E_{V_{dd}} = CV_{dd}^2$$

It is very interesting the energy consumed by the capacitor is $\frac{1}{2}CV_{dd}^2$ whereas, the energy delivered by the V_{dd} is CV_{dd}^2. The other ½ CV_{dd}^2 is consumed in some other component is either released in some other component, because the energy released by the delivered by the V_{dd} is CV_{dd}^2.

The energy consumed here or stored by the capacitor is $\frac{1}{2}CV_{dd}^2$. The other half is actually spent by this particular PMOS ancestor which is always on when the capacitor is actually charging. This E PMOS transistor is going to use this $\frac{1}{2}CV_{dd}^2$ because it has the voltage across it as the current flows through it and hence it dissipates the $\frac{1}{2}CV_{dd}^2$ continuously.

The E of PMOS, the energy dissipated by the PMOS is $\frac{1}{2}CV_{dd}^2$, the energy dissipated by PMOS depends on the capacitor, of course the capacitive load here whatever is the capacitor size whether it is 20fF or 20nF or pF, based on that it will dissipate this amount of energy. Because, based on this capacitor I will have this energy component or rather I will have this current component which will be helping in charging this particular capacitor.

The energy dissipated by the PMOS depends on the capacitor, depends on this particular load capacitance value and not on the size of the transistor or the speed of the switching. It's a kind of very very important to understand while in a digital circuit, while I am pushing it to 0 to 1 or 1 to 0 here, the output actually switches from 1 to 0 or 0 to 1 and in 0 to 1 while the capacitor is actually charging, it actually switches the output node voltage actually switches.

But, assuming that it switches and it has sufficient time to reach the steady state. The energy released by this PMOS will be nothing but $\frac{1}{2}CV_{dd}^2$ which is actually equal to that of whatever is the energy stored by this particular load capacitance. Then whatever is that energy is does not really depend on whatever is the width of the PMOS transistor or whatever is the width of the NMOS transistor.

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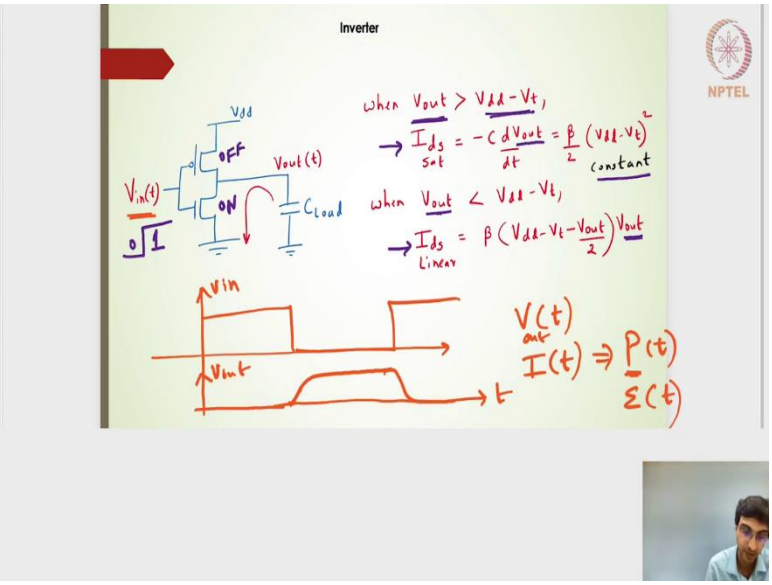

Hope this is clear. Let us take a look at the energy profile and then the power profile with respect to the time domain. What we are really looking into is identifying, what is the power in a transient analysis and what is the energy in a transient analysis.

What earlier we had looked into is based on the input values, if the input was a step voltage how did the output behave. The output while it was down we said that it will be increasing and then while the input was high we said that the output will be decreasing, this is my output profile and this based on the input we said what is the transient response of the inverter circuit. What we really we want to do now is identify the output not only the output profile, but also the current profile. That this current and output profile will help us in giving us the power profile with respect to time.

We want to find out or estimate or derive an profile for identifying the instantaneous power with respect to time domain and finally we need to integrate it and then achieve the energy for the time domain and then come across with the average energy or rather the average power.

Suppose that is the case what we want to see, we have an inverter circuit and then the input is given and let us say that we will start with a step input. A step input of 0 to 1 or 1 to 0 is given, so that the other transistor is completely OFF and the only one transistor out of this PMOS and NMOS will be ON and the output voltage the capacitive load here will either charged or discharged, there is no contention there.

As I just stated here just to reiterate that if, $V_{out} > V_{dd} - V_t$. We will have the NMOS transistor. Let us say that when the output voltage is discharging to ground that means, that the input voltage is actually 0 to 1 a step is supplied. The NMOS transistor will be ON, the PMOS will be OFF.

In that case the output voltage which starts from V_{dd} till it reaches $V_{dd} - V_t$. The $V_{dd} - V_t$ it will be in saturation the NMOS transistor will be in saturation. The saturation current will be used and that will be equated to the discharging profile, the discharging current equation for the capacitor.

$$I_{\substack{ds \\ sat}} = -C\frac{dV_{out}}{dt} = \frac{\beta}{2}(V_{dd} - V_t)^2$$

This is the NMOS transistor current and from there I should be able to find out what should be the output profile, the current profile is nothing but a constant because $\frac{\beta}{2}(V_{dd} - V_t)^2$.

When the $V_{out} < V_{dd} - V_t$ I will have the linear region. The NMOS transistor will be in linear region and in the linear region the current value is nothing but,

$$I_{\substack{ds \\ linear}} = \beta\left(V_{dd} - V_t - \frac{V_{out}}{2}\right)V_{out}$$

I will have an exponentially decreasing profile, here the output profile when the NMOS transistor in saturation it will be the output profile will be a linearly decreasing profile. This is something we had already seen and we will use this, so that we will get the output profile, we will also draw the current profile and then finally draw the power profile with respect to the instantaneous power profile with respect to the time domain.

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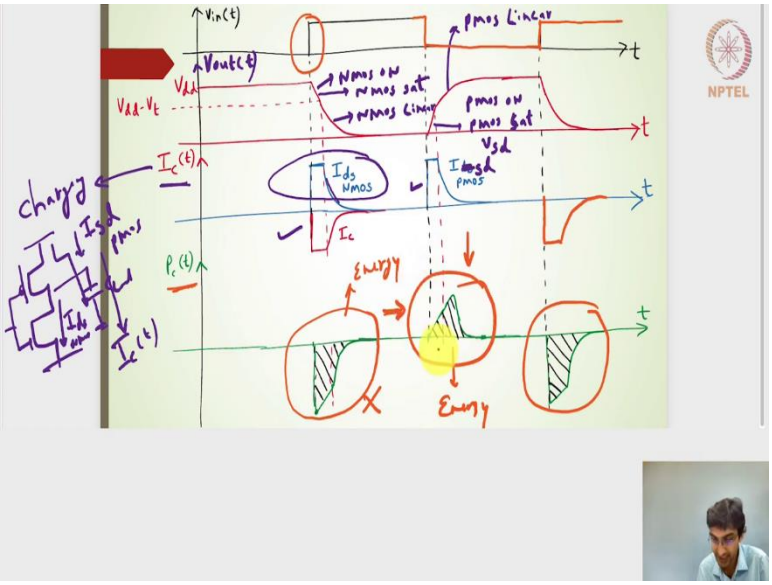

This is what we have, I have an input voltage, it is 0 and then it is the input voltage goes to 1. Whenever it is 0, the output voltage will be 1 steady state voltage and then when it does the transition from 0 to 1, I will get the output voltage doing the transition from 1 to 0. Then while it is doing the transition from 1 to 0 back the output voltage will do the transition from 0 to 1 and then so on.

This is the output profile, the current profile and the current profile I have anyways drawn, just to understand the output voltage profile. Let us take a closer look into it this is a linear profile, it is a decreasing profile. Whenever the step voltage the input voltage is high, we know that the NMOS will be ON. In fact, in both the decreasing profile the NMOS will be ON, the PMOS will be OFF.

Here the PMOS will be ON and that is why we will have the output node voltage charging the capacitor through the PMOS transistor, here the capacitive load or the output voltage decreases through the NMOS transistor. This particular region I have drawn it linear because I am getting the NMOS to be in saturation, I will have a constant current and therefore the output voltage will be a linearly decreasing profile. I am going to say that it is a NMOS in saturation and this one I will say that NMOS is in linear region or triode region.

Similarly, here in this particular case PMOS will be in linear region or rather in saturation region. That is why I have a linearly increasing profile, the output voltage is linearly

increasing and then this particular region is PMOS will be in linear region and that is why we will have an exponential increasing profile. Here when the NMOS is in linear region we will have an exponentially decreasing profile.

This is my output profile, I am going to write it as output of t, hope this is clear. Let us take a look at the current that is flowing across the capacitor. During the linearly decreasing profile here for a step input, while it is doing the transition from 0 to 1 and then when it is held one. We will get the NMOS to be in saturation that means, that the NMOS current is constant, that is why I will have a constant value here.

While it is actually the output voltage is exponentially decreasing, we should have an exponentially decreasing current here of the NMOS current, the reason is very very simple because the output voltage is actually going down. My V_{ds} value for the NMOS is going down and that will have an effect on the current and it will completely decrease.

If I want to find out the PMOS current, the ideas of the PMOS current again during the output voltage being linear here, the PMOS current is in saturation it will be constant. While the output voltage is exponentially increasing that means, that the V_{sd} value for the PMOS is decreasing and thereby the current will be decreasing and then eventually reaches 0.

This particular current profile has drawn it as the ideas of NMOS and ideas of PMOS, but if I want to consider the capacitor current and if I really want to do this particular current has nothing but the charging current. The current direction is nothing but if I consider this as an inverter and this as my capacitive load, let us say that this is my current direction of the capacitor.

If this is my current direction of the capacitor $I_c(t)$, this is an alignment with that of the I_{sd} of the PMOS. This should be nothing but the I_{sd} of the PMOS, this is an alignment. My ideas of the NMOS right, while the capacitor is discharging will be exactly opposite.

What I have done is although I have drawn the profile of ideas of NMOS. This profile for the capacitor current direction I will have it negative, so that discharging profile will be negative, the charging profile will be positive for the capacitor current. I will have the negative profile of the current and then the positive profile while it is charging and negative profile while it is discharging.

Now I have this particular current direction and in this particular current direction and now I want to have a product of this output voltage and then which is nothing but the capacitor voltage and then the capacitor current. So, that I will get the power consumed or stored by the capacitor. The power consumed by the capacitor, if I do the multiplication of this profile and then with that of this particular negative profile, I will get this particular profile a constant is there. The constant with multiplied by a linearly decreasing profile will be a linearly decreasing profile and then I will have this particular decreasing exponential profile multiplied by exponentially decreasing profile, I will get a faster rate in decreasing profile in it will be close to an exponential profile.

For charging the capacitor while the capacitor is actually consuming the power. This is the power while it is actually dissipating, while it is discharging and this particular power of the capacitor while it is charging. It is actually consuming the power, it is actually using that power to store the energy.

In this particular case it is linear here and it is constant. I will have a linear profile here up till this particular point and after that I will have an exponentially increasing profile and then exponentially decreasing profile. What it will do is the multiplication of this particular profile and this particular profile I will have a slight increase after that is going to decrease.

Note that if the PMOS is helping in charging the capacitor and then the NMOS is helping in discharging the capacitor. The energy or the power here whatever the profile here I have got the area under this particular profile. The area under this particular profile of the power should match with that of the area under this particular profile of the capacitor while it is discharging.

This particular power area in the sense in this particular power whatever is that area I calculate and then this particular area whatever I calculate in this particular profile should match and the reason is very simple. The capacitor actually charges through the PMOS transistor and then it discharges through the NMOS transistor.

The area under this particular power curve or the power profile will give me the energy term and then the area under this particular profile is nothing but the energy term. The capacitor can actually store the energy and the same amount of energy is actually released. The capacitor stores the energy through the PMOS transistor and it discharges the whole amount of energy through the NMOS transistors.

What I have done in this particular step input I have once again given a step 0 to 1 here. So, it behaves very very similarly to what we had seen in this particular time domain. It decreases and then we will have the same profile of the current and so I will have the same profile of the power here also.

I started with the step input of 0 to 1 and then 1 to 0 and then 0 to 1. I have three such profiles for the output voltage, for the currents, for the power. From now on what we will do is, we will consider the charging first and then the discharging, we are going to ignore this effect.

What we will do is we will start with this particular profile charging and then of course, the discharging. The input site it will do a transition of 1 to 0 and then that will help in charging the output node, charging the capacitor and then from 0 to 1 it will start discharging.

I will start from here, my time domain or rather in the next figure you will not see this particular figure at all. You will see the power with respect to time domain, the instantaneous power in the capacitor starting from this particular axis or this particular time domain.