## **Design and Analysis of VLSI Subsystems Dr. Madhav Rao Department of Electronics and Communication Engineering Indian Institute of Technology, Bangalore**

## **Lecture - 58 Repeater Designs**

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Hello students. Let us continue with the repeaters section of this particular lecture. In the last lecture we had seen about this particular folded technology and then the conventional CMOS design, whereas in the folded technology we got the normalised parasitic factor to be nothing but  $\frac{1}{2}$ .

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: Capacitance of unit inverte  $R_W$  &  $C_W$  = Resistance &<br>Capacitance of wire pe T-model  $(cw)_{inv} + c u$  $+C_4l + C_6l$  $+$  $\frac{1}{\omega}$  =  $\frac{1}{N}$   $\frac{1}{N}$   $\frac{1}{N}$   $\frac{1}{N}$ 

Moving ahead, my overall segment of the wire with the repeater 1. Let me actually rewrite this particular portion is for the repeater, the one part of the repeater number 1 and then this particular portion is for the input capacitance seen from the repeater number 2.

I am going to write it as a repeater number 2 and in between this particular section is our segment of the wire. I am going to write it as segment. So, this particular segment of the wire I have the resistance  $R_w \frac{1}{N}$  $\frac{1}{N}$  and the capacitance on both the sides of the resistance will be  $C_w \frac{1}{21}$  $\frac{1}{2N}$  and then  $C_w \frac{1}{2N}$  $\frac{1}{2N}$  represents our  $\Pi$  model, that is what I have written here.

The repeater number 1, I will have the switching resistance of  $\frac{R}{W}$  and then the parasitic capacitance of  $C_w \rho_{inv}$  it could be 1 or 0.5 as per the design technology node and the input capacitance of the repeater number 2 is  $C_w$ . We have the capacitances, we have the switching resistance of the repeater number 1 accommodated, this is for one particular segment.

The R the switching resistance or the capacitances or the resistance of the wire everything kind of involved in this one particular segment of the wire which starts from the repeater number 1 and then ends at the input of the repeater number 2.

Similarly, if I have the length of the wire segmented into N segments. The N multiplied by this particular RC circuit representation for one segment, if I actually multiplied by n times I should be able to represent the whole length of the wire with an inserted repeaters.

We will be able to have the overall representation. Now considering this particular one segment of representation let us now try to understand the delay aspect. The delay for the 1 segment, the delay of the 1 segment to the propagation delay I have not written it as falling or rising it could be and the considering both of them will be the same.

I am considering the propagation delay for 1 segment of the wire and if I consider that I will have this as a source node, it could be connected to  $V_{dd}$  or to the ground. In that sense if I consider the l model delay.

$$
t_{1-\text{segment}} = \frac{R}{W} \left( \text{cw} \rho_{\text{inv}} + \frac{C_w l}{2N} + \frac{C_w l}{2N} + CW \right) + R_w \frac{l}{N} \left( \frac{C_w l}{2N} + CW \right)
$$

This becomes the overall one segment of the wire and its propagation delay.

If I have N segment of the wire then I will have the everything multiplied by N. That is what I have written here,

$$
t_{\text{N-segment}\atop \text{wire}} = \frac{NR}{W} \Big( CW\rho_{\text{inv}} + \frac{C_w l}{N} + CW \Big) + R_w l \Big( \frac{C_w l}{2N} + CW \Big)
$$

What next now that we have estimated, we have expressed the overall delay for the N segments or the wire of length l in between the each of the segments we have added the repeaters. In this particular case we have added the inverters, inverters in the form of the repeaters.

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Let us try to identify what should be that optimum W or what should be the optimum width of the repeater. Remember that this is the scaling of the repeater and it is not the width of the wire, it is the scaling now how wide the repeater or the inverter in this particular case should be, so that I will get the minimum delay?

If I make it is equal to 0 then I should have used that particular previous slide expression and then differentiate with respect to w and then equate it to 0,

$$
\frac{\partial \mathbf{t}_{\mathrm{pd}}}{\partial \mathbf{W}} = 0 - \frac{\mathbf{R} \mathbf{C}_{\mathrm{w}} \mathbf{I}}{\mathbf{W}^2} + 0 + \mathbf{R}_{\mathrm{w}} \mathbf{I} \mathbf{C} = 0
$$

$$
W_{\text{min,delay}} = \sqrt{\frac{RC_{\text{w}}}{R_{\text{w}}C}}
$$

Where this  $C_w$  and then  $R_w$  are the properties of the wire per unit length.

This is the wire per unit length will give me the  $C_w$  and  $R_w$ ,  $C_w$  is nothing but the capacitance per unit length and  $R_w$  is nothing but the resistance per unit length. The R and C are the nothing but the switching resistance and then the capacitance of the inverters or the repeaters here.

In this case the R value is nothing but the unit inverters switching resistance and then C value is the unit inverters parasitic capacitance or whatever the input capacitance. The  $C_w$ and  $R_w$  is nothing but the characteristics of the wire because it is actually  $C_wR_w$  of the units per unit length of the wire. I should be able to find out what should be the scaling of the repeater what should be the scaling of the inverter here, so that we will get the minimum delay.

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Now I can also have, if I look into that particular previous expression, this particular expression for the N segment of the wire which means for all the overall length of the wire connecting between the driver and the receiver, it is a function of W as well as it is a function of N, it is a function of N, it is a function of N.

If I go back and if I make the differentiation of the propagation delay with respect to the N and equate it to 0 I should be able to find out the best actually l by N factor, although I have done the differentiation of N assuming that the l is a factor. If I do that particular differentiation with respect to the N, I should be able to find out the best N value and I can redefine it in terms of l/N.

$$
\frac{\partial t_{\text{pd}}}{\partial N} = 0
$$
  
RC $\rho_{\text{inv}} + 0 + RC - \frac{R_w C_w l^2}{2N^2} = 0$   
RC(1 +  $\rho_{\text{inv}} = \frac{R_w C_w}{2} \left(\frac{l}{N}\right)^2$ 

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The best l/N for the minimum delay turns out to be,

$$
\frac{1}{N_{\min, delay}} = \sqrt{\frac{2RC(1 + \rho_{\text{inv}})}{R_{\text{w}}C_{\text{w}}}}
$$

I can remember the  $R_w$  and  $C_w$  is the characteristics of the wire, R and C are nothing but the switching resistance and then the parasitic capacitances or the input capacitances seen at the off the unit inverter and in the square root of that.

L is the length of the wire and N is the number of segments in the wire that is being made. The number of segments of the wire that is being made and then we have inserted the repeaters and generally if I have N segments I will have N - 1 repeaters.

This N is the number of segments and l is the length of the wire, the best l/N, that I will get the minimum delay is nothing but given by this particular expression and the best W that is the size the scaling of the inverters to form the repeater is given by the square root

$$
\mathrm{of}\,\sqrt{\frac{RC_w}{R_wc}}\,
$$

Now, let us take a look at this particular unit inverter, its a unit inverter driving 4 unit inverters. I have a capacitance of c and I have a capacitance on the gate side of each of the 4 unit inverters is nothing but 1C 1C 1C 1C. The overall capacitances seen at this particular node is nothing but 5C. The propagation delay of 5C and then the switching resistance of R will be nothing but R x 5C, that is 5RC.

Now, why it is important is Fo4, we will normally get the characteristics for a particular technology node in the form of, if I design a chip here and somewhere here I will have a Fo4 circuit. The objective of an Fo4 circuit is to characterise the objective here is to say that what is the characteristics of this Fo4 and one of the characteristic parameters is the delay which is nothing but turns out to be 5RC and what is that particular value?

Generally when we design the chip, we will have small Fo4 circuits and around the space of the corners where there are some space in the chip and then we design the Fo4 circuit and then identify what is a delay. Generally the chip whenever it is characterised according to the technology node whether it is a 65nm technology node or a 45nm technology node, we will get the first and foremost parameter will be the Fo4 value in terms of the delay.

If I have an Fo4 value which is nothing but 5RC, now can we rewrite this particular l/N parameter or W parameter, if it is possible in the form of Fo4. The W parameter I think it is very difficult to write in the form of an Fo4. We do not write it, but the l/N parameter because it is 2RC, I can easily convert it into 5RC which is nothing but Fo4.

The l/N as a function of a Fo4 I can write it and you know this is the expression. So, instead of 2RC twice the R C to minimum nothing, but Fo4 which is nothing but 5RC. If I want it Fo4 in terms of 2RC.

The 2RC turns out to be  $\frac{F\sigma 4}{5}$  x2 =  $\sqrt{\frac{0.4 F\sigma 4 (1 + \rho_{inv})}{R_W C_W}}$  $\frac{R_W C_W}{R_W C_W}$ . Fo4 is nothing but fan out of 4 circuits. The reason it is called as a fan out is the fan out of the electrical effort turns out to be actually be 4. An inverter driving a unit inverter driving the 4 other unit inverters. Hope this is clear.

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Moving ahead, my propagation delay for the N segment of the wire is actually given by this particular expression which is taken from our earlier slides. It is nothing but,

$$
t_{pd} = N \left[ RC (\rho_{inv} + 1) + \frac{C_w l}{N} \frac{R}{W} + R_w \frac{1}{N} \left( CW + \frac{C_w l}{2N} \right) \right]
$$
  

$$
\frac{t_{pd}}{l} = \frac{N}{l} \left[ RC (\rho_{inv} + 1) + \frac{RC_w l}{W} \frac{1}{N} + R_w CW \frac{1}{N} + \frac{R_w C_w}{2} \left( \frac{l}{N} \right)^2 \right]
$$
  

$$
\frac{t_{pd}}{l} = \frac{RC (\rho_{inv} + 1)}{l/N} + \frac{RC_w}{W} + R_w CW + \frac{R_w C_w}{2} \frac{l}{N}
$$

Notice that what I have done is  $\frac{t_{pd}}{l}$  expression. The delay per unit length is written in the form of l/N, w, w and an l/N and to find out the best delay per unit length of the wire, the best delay per unit length of the wire we have got the optimum w, optimum w's and we have got the optimum l/N.

The expression for the optimum l/N and then the expression for the w optimum w if I put it here, I should be able to find out what should be the minimum delay per unit length of the wire. If I have n segments and if I have repeaters inserted each of the N segments of the wire.

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$$
\frac{\left(\frac{t_{\rho}\lambda}{\lambda}\right)}{\frac{1}{\lambda}} = \frac{RC(1+\text{lim})}{\frac{(k/\nu)_{\text{min}}\lambda}+\text{lim }_{\omega}\omega_{\text{min}} + \text{lim }_{\omega}\omega_{\text{min}} + \frac{RC\omega_{\text{min}} + \frac{RC\omega_{\text{min}}}{\lambda}}{R\omega_{\text{min}}}}}{\frac{RC(1+\text{lim})}{\frac{RC\omega_{\text{min}} + RC\omega_{\text{min}} + \text{lim }_{\omega}\omega_{\text{min}} + \frac{RC\omega_{\text{min}} + RC\omega_{\text{min}}}{\lambda}}}{\frac{RC(1+\text{lim})}{\frac{RC\omega_{\text{min}} + RC\omega_{\text{min}} + \text{lim }_{\omega}\omega_{\text{min}} + \frac{RC\omega_{\text{min}}}{\lambda}}}{\frac{RC\omega_{\text{min}} + \text{lim }_{\omega}\omega_{\text{min}} + \frac{RC\omega_{\text{min}}}{\lambda}}{2RC\omega_{\text{min}}}}}
$$

Doing that I should be able to find the minimum delay per unit length of the wire. The minimum delay per unit length of the wire by substituting this optimum l/N and w parameters.

$$
\left(\frac{t_{\rm pd}}{l}\right)_{\min, \text{delay}} = \frac{RC \left(\rho_{\rm inv} + 1\right)}{\left(\frac{l}{N}\right)_{\min, \text{delay}}} + \frac{RC_{w}}{W_{\min, \text{delay}}} + R_{w}CW_{\min, \text{delay}} + \frac{R_{w}C_{w}}{2}\left(\frac{l}{N}\right)_{\min, \text{delay}}
$$
\n
$$
= \frac{RC \left(\rho_{\rm inv} + 1\right)}{\sqrt{\frac{2RC(1 + \rho_{\rm inv})}{R_{w}C_{w}}}} + \frac{RC_{w}}{\sqrt{\frac{RC_{w}}{R_{w}C}}} + R_{w}C \sqrt{\frac{RC_{w}}{R_{w}C}} + \frac{R_{w}C_{w}}{2}\sqrt{\frac{2RC(1 + \rho_{\rm inv})}{R_{w}C_{w}}}
$$
\n
$$
\left(\frac{t_{\rm pd}}{l}\right)_{\min, \text{delay}} = \sqrt{R_{w}C_{w}RC}(\sqrt{2(1 + \rho_{\rm inv})} + 2)
$$

This is an expression for a wire from A to B where I have a driver circuit and I have a receiver circuit and where it is kind of there is N such segments and each of the segments has an inverter which acts like a repeater.

This is an expression for the overall delay per unit length of the wire and it is in terms of  $R_w$  C<sub>w</sub>, the characteristics resistance and then the capacitance of the wire. Then we have R and C which is nothing but the unit inverters switching resistance and then the unit inverters capacitance. Then we also have this the delay per unit length as a function of the normalized parasitic factor for the inverter, it could be 1 and it could be also be less than 1 using the folded technology. One thing I wanted to mention here is what we have finally evaluated is this particular delay per unit length of the wire.

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 $RC(Hlim)$ 

What it means is if suppose I have a long length of the wire starting from A to B, on A side we have a driver circuit in the form of an inverter or any other combinational circuit. Then on the B side I have a receiver circuit that could be also be a combinational circuit and earlier we had seen in inverter circuit, but what we have done is we have actually divided this into N segments and in each of these N segments we have inserted N inverter.

We have an inverter inserted in each of this particular points, I have an N segments. Each of this segments I can call it or we can label it and then form it as an N segments and we have added an inverter in each of this segment point, we have an N - 1 inverter.

We added this inverter in the form of a repeater, so that at the end of the wire B we will get a very good signal strength, that is one purpose. The another purpose is if I have the long length of the wire from A to B without any repeaters, we know that the delay in this particular case will be directly proportional to the square root of the length of the wire.

In this particular case because now we have got l/N as an optimised number, now the delay with segmented wire with the segmented as well as with addition of repeaters. I will call it as a wire with repeaters, the l/N becomes a constant and my overall delay in this particular case will be directly proportional to the length of the wire.

We tend to believe that if I have a long length of the wire A to B with the repeaters in each of this segmented part or the demarcation part. Then it will have the overall delay of not only the length of the wire, but also the propagation delay of all this repeaters or all this inverters which are added as a form of the repeaters.

My overall delay for the wire with the repeaters we tend to believe that will be more than that of the delay with respect to the wire AB. But, that is not the case remember that we have added the inverters or the repeaters here and we have optimised the w value. The w value optimised parameter will help us in driving the current for each of these segments of the wire. For each of these segments of the wire we will have a good driving current because the repeaters are added.

The repeaters are added in, then intention that we will get a good signal strength at particular point B, but also the driving current will help to ensure that the overall delay for each of the segments of the wire, will be very very less. Thereby the overall delay for the segment for the length of the wire A to B will also be actually be reduced, then when we compare that with the wire delay without the repeaters.

Essentially, we have reached to a point where the delay per unit length or the propagation delay per unit length of the wire which we have expressed for the minimum delay tends to be actually be less than for the delay of the wire with no repeaters.