Design and Analysis of VLSI Subsystems
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Lecture - 56
Transient analysis in Crosstalk

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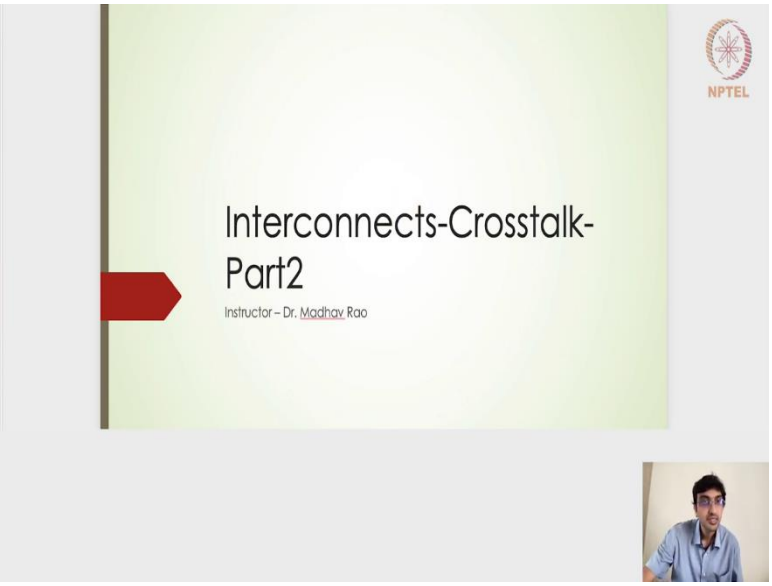

Hello, students. Welcome to this lecture on Interconnects and in this particular lecture we will talk more about the Crosstalk effects. In that sense we will talk about the crosstalk in a manner where there is one aggressor wire which is affecting the other victim wire, where the victim wire is actually held to a constant voltage and we will see what is that transient respond or a transient analysis for the victim wire.

What is that magnitude of the transient response, if the drivers of both the wires, if the drivers of the attacker as well as the drivers of the victim wires if it is of a particular size we will then try to estimate what should be the effect of the crosstalk on the victim wire, moving further let us go to the next one.

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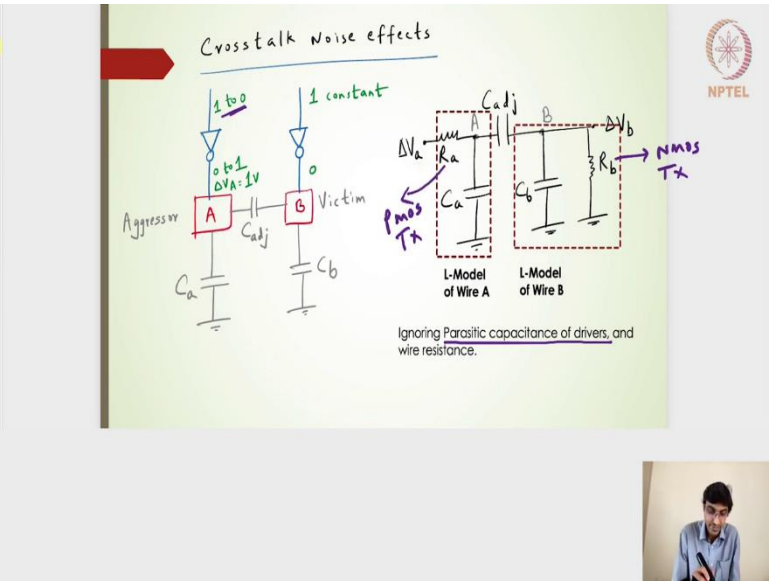

Here in this particular slide I have just done a schematic of the crosstalks. I have just shown the wire A and B where the wire A is driven by the inverter here and the wire B is also driven by an inverter. The wire A and wire B has its own characteristics capacitance and then a resistance.

The capacitance C_a and C_b its own characteristics capacitance which is seen here because the wire A and B are close to each other, then we will say that we also incorporate the adjacent capacitance or a coupling capacitance here. I am saying I am labelling the aggressor for the wire A and then the victim for the wire B.

The changes here made for the wire A or rather the changes made here in the driver circuit is going to drive the changes in the wire A and that is going to get coupled to some extent to the wire B which is held constant. An input to this wire B is a inverter driver circuit is held constant to a logic level high, the output will be held constant to 0.

That means this particular wire which is connected to the output node, the output node is actually pulled down to the ground via the NMOS transistor via the on NMOS transistor. In that sense this particular wire is kind of connected to the ground via the NMOS transistor.

Here there is a change in the input 1 to 0 and that is why there is a change in the output from 0 to 1 and we need to know what kind of an effect it will have on the wire B, although the wire B is connected to the ground via the NMOS transistor.

Again C_a and C_b and C_{adj} are the capacitances associated with the dimensions of the wire A, B and its the neighbouring dimensions in the sense the spacing between the wire A and B will be able to characterize this C_{adj} capacitance, hope this is clear.

If I want to represent this wire A and wire B in terms of the RNC circuit. I will use a very simple model L model on both the wire A and B and in between there is a coupling capacitance or an adjacent capacitance, this dotted box are represents the same. It is an L model of the wire A and then another dotted box is the L model of the wire B inside the dotted boxes we see the resistance R_a and then the capacitance C_a.

Similarly, for the wire B we have the capacitance C_b and then the wire R_b is actually connected to the ground. What it means is this particular switching resistance of the R_b, but this particular resistance is nothing but the NMOS resistance and then connected to the ground, that is what this R_b represents. This is basically the NMOS1, NMOS transistor switching resistance.

For the wire A here it is actually changing from 0 to 1. That means, assuming that it is a step input at the input side. We will get 0 to 1 that means, the PMOS transistor is actually on and then the NMOS transistor is off. This could be considered as the switching resistance of the PMOS transistor and then C_a, C_b and then C_{adj} is anyways taken from this particular schematic diagram, what I have ignored here is the parasitic capacitances of the driver.

The inverters parasitic capacitance we say that it is very very less than that of the wire capacitances hence that has been ignored and the wire resistance which is of a pretty long length of the wire that is also kind of ignored. The resistance of the wire is kind of ignored, but we have accommodated the resistance of the inverter.

In fact, this particular resistance R_a and R_b could also accommodate for both the inverters switching resistance as well as the long length of the wire, that is also possible.

But, in this particular scenario what we say is R_a and r_b it is just the switching resistance of the of the driver circuit. Hope this particular diagram is clear.

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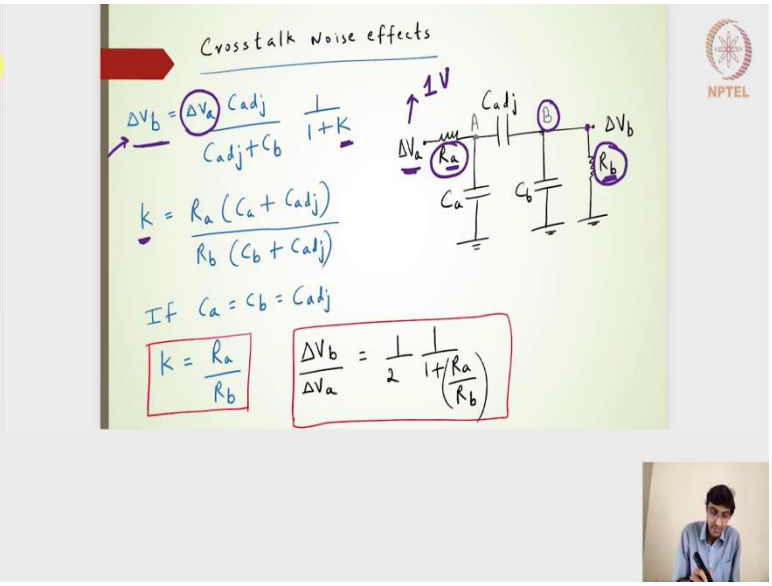

Moving ahead if suppose I have this particular R_c circuit and if there is a ΔV_a. Which is generally in this particular case will be nothing but 1 volts. A change in the input will give me a change in the output for a digital circuit I will have a one volts change for a 65nm technology node. What will be it is effect on the other side of the wire B, at this particular point B point?

That is given by this particular expression, ΔV_b the change in the B node or rather we can say it is the victim node and aggressor is the A wire the victim is the B wire.

$$\Delta V_b = \frac{\Delta V_a C_{adj}}{C_{adj} + C_a} \frac{1}{1 + K}$$

Where, $K = \frac{R_a(C_a + C_{adj})}{R_b(C_b + C_{adj})}$

It is basically turns out to be a time constant factor. A ratio of the time constant for the wire A and its associated capacitance, and then similarly the time constant for the wire B which is resistance and associated capacitance. Just for our simplification if we consider all,

$$C_a = C_b = C_{adj}$$

$$K = \frac{R_a}{R_b}$$

$$\frac{\Delta V_b}{\Delta V_a} = \frac{1}{2}\frac{1}{1 + \frac{R_a}{R_b}}$$

This is my overall expression a very simplified expression considering the capacitances are equal. It becomes this particular function or the ΔV_b, the change in ΔV_b with respect to the change in ΔV_a becomes a function of the driver switching resistance between the R_a and R_b.

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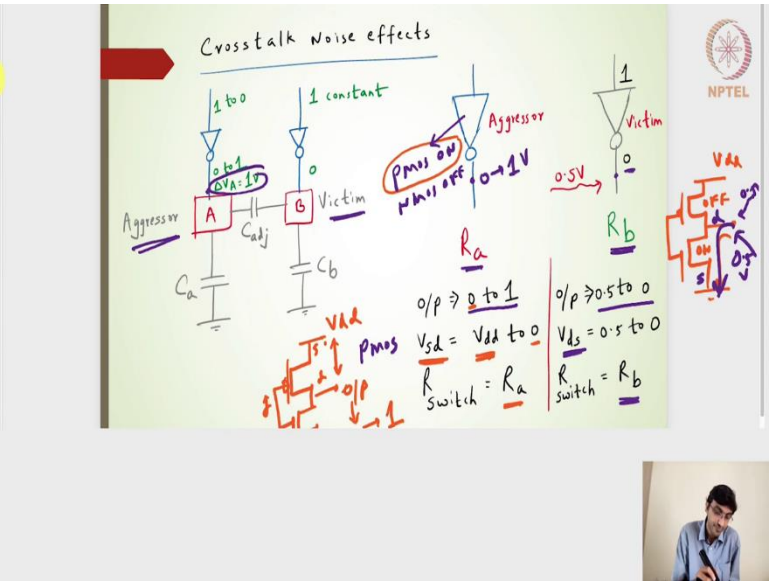

Let us say this is my aggressor wire and then this is a victim wire. Let us say there is a change in the voltage ΔV_a is 1 volts here because of the coupling effect the change here in 0 to 1 volts let us say that it is getting 0.5 volts.

I am just assuming some particular voltage and I am saying that because it is a change in 1 volts and C_{adj} and C_b everything is same. We will have the change here if at all there is a change here the maximum change in the wire B or rather the maximum change in the voltage with respect to the wire B will be 0.5.

If 0.5 goes here at the output side because of the coupling capacitance, although it is held at 0 because of the NMOS transistor which is connected to the ground. This 0 voltage is

constantly pulled to the ground, but because there is a 0.5 voltage that is kind of coupled from the neighbouring wire. What should be the switching resistance of R_b or the driver B and what should be the switching resistance of the driver A?

In this case the drivers are nothing but the inverter circuit. We need to find out what is the switching resistance of the inverter on the A wire and what should be the switching resistance on the inverter that is there on the wire B. To find out the switching resistance what we need to know is what is the output voltage changing from.

In this aggressor line the output voltage is actually changing from 0 to 1 volts. In the victim line the change in voltage is actually 0.5, it is actually held constant at 0 volts, but because of this coupling capacitance we will get a 0.5 voltage line and then this 0.5 voltage gets should be discharged to 0 volts.

The output voltage is actually 0.5 to 0 in this case because on the A side it is a PMOS transistor which is making this change from 0 to 1 volts at the output side. If I consider the inverter here the PMOS is ON and the NMOS is OFF and that is the reason why we are getting the output voltage from 0 to 1 volts.

In that sense if the PMOS is ON the switching resistance is with respect to the PMOS transistor and if that is the case then the V_{sd} of the PMOS the output is 0. Let me draw the PMOS circuit and then the NMOS circuit and let us say that this is my driver on the A side. This is my output on the A side and the output is actually changing from 0 to 1.

The V_{sd} so, the source here and then the drain here and then the gate here. The $C_{a_{sd}}$ of the PMOS when it was at 0 volts the output was 0 volts, we got the V_{sd} as V_{dd}, that is what it is and then when it became 1 the V_{sd} was 0, that is the change here V_{dd} to 0.

If I try to find out the switching resistance for the PMOS transistor on the A side on the aggressor line we can note it as R_a and similarly if we do the same thing here on this side, but on this side it is actually the NMOS transistor. Let me draw the inverter V_{dd} and here the output is actually constantly going to the connected to the ground because the NMOS is ON and then the PMOS is OFF, but because it sees 0.5 line here at the output line 0.5.

There is a 0.5 voltage coming which are coupling from the wire A side. Let me know instead of this one I will say that this is 0.5 volts. The 0.5 volts is going to get discharged

to 0 volts. My output is at 0.5 volts and then it will go back to 0, that means, at the V_{ds} value V_{ds} of the NMOS V_{ds} will be 0.5 to 0 and my switching resistance is considered as R_b.

Now, what we have done here in this particular slide is we estimated the switching resistance for the aggressor line. The driver on the aggressor line and estimated the switching resistance on for the driver on the victim line and the switching resistance for the driver on the aggressor line turns out to be R_a and the switching resistance for the aggress for the victim for the driver on the victim line turn is stated as R_b.

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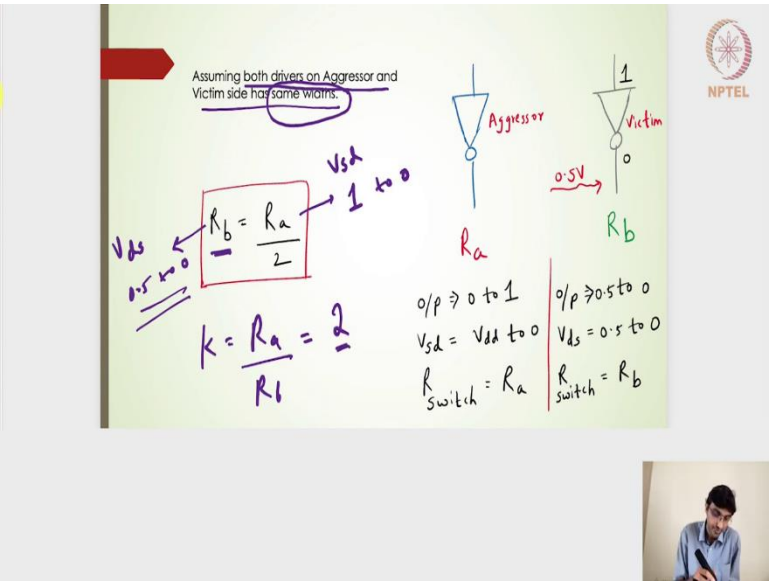

Let us say both the driver widths are same. On the aggressor and victim side has the same widths. If I have the same width here just at the output voltage is different and thereby my V_{sd} value and V_{ds} value are different, my R_b is going to be half and approximately I am taking a very approximate measure because the voltage for the B side is actually 0.5 to 0 volts and here on the A side it is actually 1 volts to 0 volts, if I am talking about V_{sd} on the PMOS side and then V_{ds} on the NMOS side.

The change in voltage is actually exactly half from the B side to that of the A side. We can consider that the,

$$R_b = \frac{R_a}{2}$$

If the sizes are the same if the width of the both the inverter circuits or the driver circuits are same. What we have is $R_b = R_a/2$ if the widths are same. In that sense the $K = \frac{R_a}{R_b} = 2$ if it is of the same size. If it is different size we will have a different ratio.

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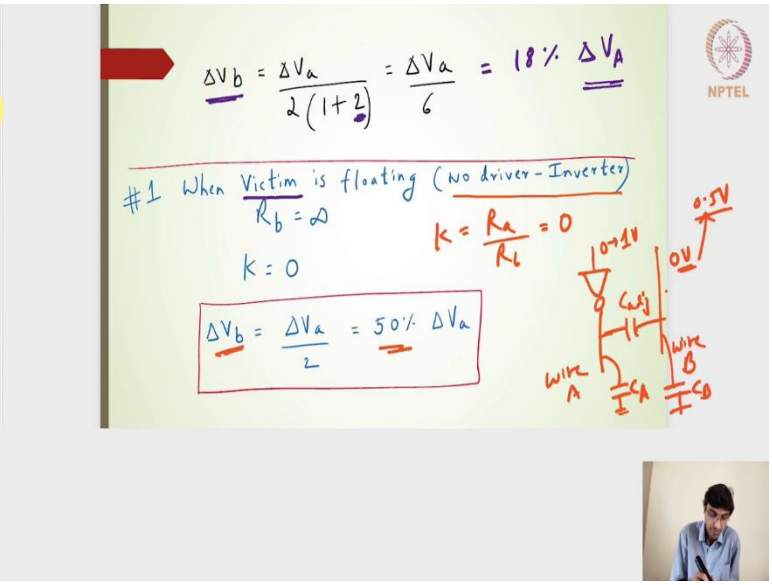

In that sense ΔV_b which was nothing but as a function of ΔV_a or

$$\frac{\Delta V_b}{\Delta V_a} = \frac{1}{2(1+K)}$$

$$\Delta V_b = \frac{\Delta V_a}{2(1+2)} = \frac{\Delta V_a}{6} = 18.88\%\ \Delta V_a$$

A change in 0 to 1 volts on the A side on the aggressor side will have an effect of 18%, 0.18 volts on the victim side.

Now let us take case by case and also see some cases where we have a different width on the driver side for both the aggressor and then the victim line. Let us say that when the victim is floating that means that there is no driver inverter circuit at all. We will have $R_b = \infty$. The switching resistance when it is actually floating there would not be any switching resistance and in fact, we can say that it is an $R_b = \infty$, it is an open circuit kind of thing.

If $R_b = \infty$, $K = \frac{R_a}{R_b}$. In that sense the $K = 0$ represents,

$$\frac{\Delta V_b}{\Delta V_a} = \frac{1}{2(1+K)}$$

$$\Delta V_b = \frac{\Delta V_a}{2(1+0)} = \frac{\Delta V_a}{2} = 50\%\ \Delta V_a$$

This is the case one when the victim is floating what it really means is it is not connected by any driver circuit.

What I can draw one figure for the line, this is the wire A and then the wire B will be something like this. There is no driver circuit that is connected and it is like that it is a simple wire, but it has the coupling capacitance C_{adj} and this wire will have C_a capacitance and then this wire will have C_b capacitance.

In that case if it is not driven by any inverter circuit or any circuit here any logic gates here, then we will have that the voltage due to the change here from the on the wire A side which is driven by this particular inverter turns out to be 50% of the ΔV_a.

Remember that this 50% because it is held floating, we will have a constant 50% voltage here. This particular if it was held at 0 volts, this is going to jump to 0.5 volts here if it is the change of 0 to 1 volts here on the wire A side on the aggressor side. We will have 0.5 volts and this will be held constant.

We had seen the last case if it was driven by another inverter, then the NMOS was constantly ON and even though if it reaches whatever voltage it should come back to the 0 volts. Hope that is clear.

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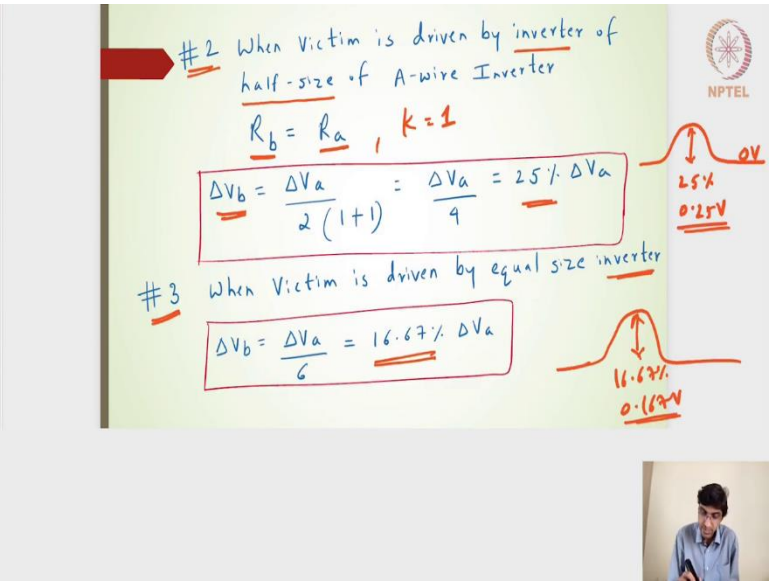

Let us say the 2nd case when the victim is driven by an inverter, a victims inverter is half the size of the wire A. The size is less that means, that the resistance with this particular half the size should be equal to will be more than that of the resistance when it was of the same size. In that sense $R_b = R_a$.

In that case the $K = 1$ and I will have,

$$\Delta V_b = \frac{\Delta V_a}{2(1+1)} = \frac{\Delta V_a}{4} = 25\% \, \Delta V_a$$

ΔV_b the change in the voltage in the victim line side will be 25% to that of the change in the aggressor side. You will have a 25%, but because there is an inverter which is constantly driving this wire, even though there is a 25% change it should come back to 0 volts.

This change will be the maximum change will be nothing but 25% of the change in the aggressor side which will be one volt. It is 0.25 volts is what we should be able to get as the maximum change. 3rd case when the victim is driven by the equal size inverter and this is what we had seen.

$$\Delta V_b = \frac{\Delta V_a}{6} = 16.67\% \, \Delta V_a$$

$\frac{\Delta V_a}{6}$ for the change in the voltage and if it is given by the inverter then again its change will be 16.67%, it will be 0.16 volts will be the maximum if the change on the aggressor side is 1 volts.

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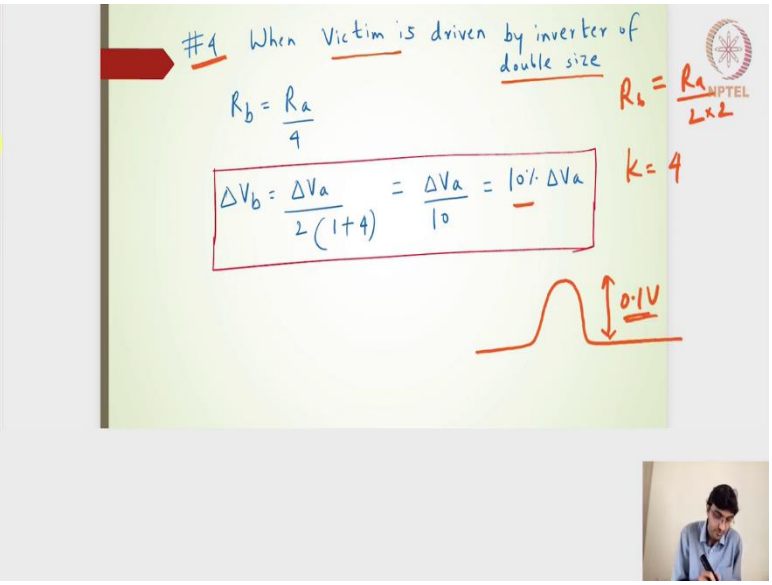

Lastly, when the victim is driven by the inverter of double the size, that means, my R_b is actually very very small now. If it was of the same size we had $\frac{R_a}{2}$ now if the size itself is double. We should have a much lesser resistance and by the long channel model we can easily scale it and then say that it is $\frac{R_a}{4}$.

My $K = 4$,

$$\Delta V_b = \frac{\Delta V_a}{2(1+4)} = \frac{\Delta V_a}{10} = 10\% \, \Delta V_a$$

The 10% means I will have a change of 10% and then coming back. This change will be 0.1 volts, if the aggressor line voltage change is 1 volts.

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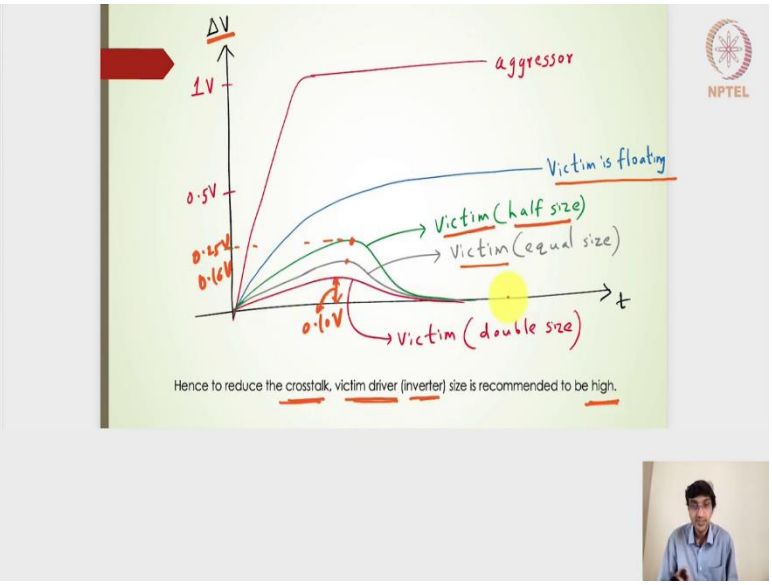

Finally, what I have drawn here is for different cases of the victim for the different cases of the inverter or the driver circuit that is designed on the victim side not on the aggressor side, on the victim side what is the transient response. This is the Δ voltage change on the y-axis and then the t time because it is a transient change, we need a time factor on the x-axis and 1 volts and 0.5 volts and then so on.

If actually aggressor is changing from 0 to 1 volts what will be the change on the victim side. If the victim wire is left floating there is no driver circuit then as I said earlier it will be held constant to 0.5 volts. Once it reaches to 0.5 it will be held constant because there is no other driver circuit which makes it pull down or pull high.

It is not connected to the NMOS transistor and then connected to the ground, in that sense the wire is floating and that is why it will get charged to 0.5 volts and it will be held constant. When the victim is half the size, let me go previously when the victim is half the size $R_b = R_a$, K = 1 and then we got to 25%.

This particular change is a 25% line. If I draw this, this will be 0.25 volts. Here you see that it goes to a maximum of 0.25 volts and then comes back to ground voltage comes back to 0 voltage because it is driven by an inverter of half the size. There is an inverter which ensures that the wire is constantly connected to the ground voltage through the on NMOS transistor.

Similarly, when the victim is of equal size we got 16.67% of the change from the aggressor line changing the voltage and if that is 1, we will get this 0.16 voltage here if the victim driver circuit is of the equal size and lastly if the victim is of the double the size we will get even lesser voltage which is around 10%, this change maximum change is 0.10 volts.

Hence to reduce this magnitude of the crosstalk effect cand also called as crosstalk noise effects coming from the aggressor line to the victim line we say that the victims driver circuit or whatever the inverter size in this particular case it could be a NAND gate, it could be a combinational gate, make sure that the gate size is considered or recommended to be very high. In that sense if the gate sizes are made higher, then we will have a lesser switching resistance and that is likely to give a lesser effect onto the victim line.