Design and Analysis of VLSI Subsystems
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Lecture - 55
Introduction to crosstalks in interconnects

Hello students, welcome to this lecture on the interconnects and especially in this particular lecture we will talk about the crosstalk effects between the interconnects on the same layer. We have multiple layers in a silicon on chip design and if especially we have a lot of stacked metal layers, but in this particular lecture we are going to talk about the interconnects in the same layer and its how it affects the other interconnects even if it is not switching or if it is switching.

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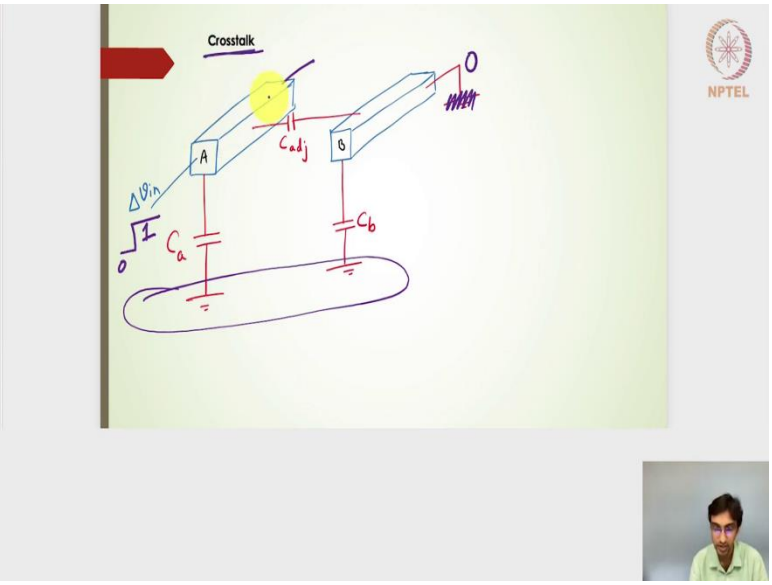

Let us begin with this particular lecture. Here I have just drawn a block diagram representation showing 2 wires the wires A here and then the wire B here and individual wires will have its own capacitance with respect to the another layer of metal I have just represented it in the form of a ground layer or a ground plane.

That is why these two are indicated as a ground symbol and it will have its own resistance the wire A will have its own resistance the wire B will have its own resistance and it will have its it can be characterised with a capacitance as well. A C_a capacitance for the wire A and a C_b capacitance for the wire B.

Between this wires the wire A and B there is a dielectric and which gives an adjacent capacitance between the wire A and B and that is why I have drawn or denoted an adjacent capacitance as well between the wires A and B and I have said that this particular wire is kind of connected to the ground, that is perfectly fine.

What we are seeing here is if there is a small change or rather in a digital circuit if there is a change from 0 to V_{dd} or to logic 1 here. I will have a change in the wire A that will be kind of propagated from the 1 side of the wire to the other side, but because of this coupling capacitance or the adjacent capacitance there will be an effect on the wire B as well alright. Even if the wire B, if it is not holding the ground if it is at logic 0 and let us say that it is not being driven by any of the circuits its having a floating voltage of 0, a change here in the wire A will have a coupling effect or a crosstalk on the wire B. I will have some kind of a change in the voltage for the wire B and that is called as a crosstalk effect.

It is named as a crosstalk because it is actually the communication between the wire A here transferring the signal the change in the logic here from one end to other end which is unnecessary getting coupled into the wire B and wire B does not have any intention of the change in the voltage here it is getting the coupling effect from the wire A and that is the reason why it is called as kind of a crosstalk, it is hearing whatever the wire A is communicating or talking and that is why it is called as a crosstalk effect.

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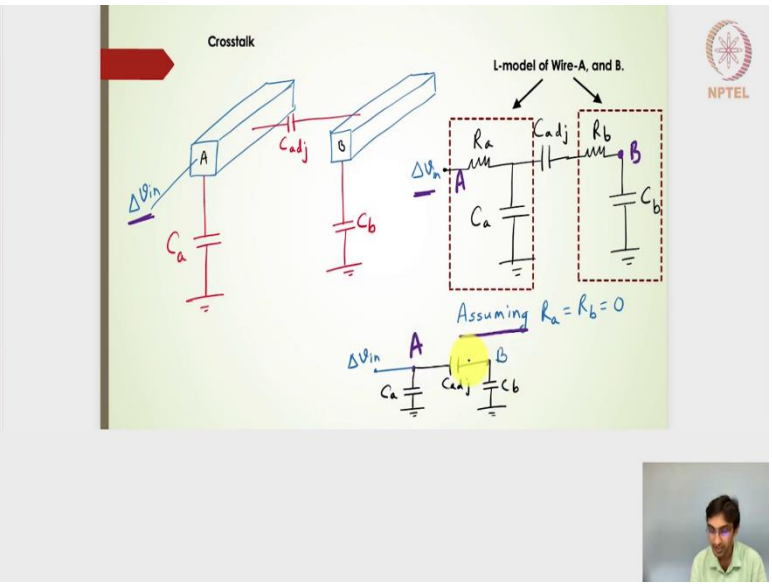

Moving ahead. Let us say that this wire B is not connected anywhere it is not driven by any other circuit. I have this particular capacitive representation of this two wires A and B between they have there is a adjacent capacitance and wire A has a small change in the form of delta v input.

If I actually represent this in an L model for the wire A and B and in between there is an adjacent capacitance this is how the overall circuit looks like. The delta Vin applied to the wire A which can be represented in the L model as R_a and then C_a and then we have this C adjacent and then the wire B which could be represented in the L model. The Rb and C_b, C_b is connected to the ground and this particular node is kind of left floating. The question is if this is the point B and then let us say this is the point A alright.

The change in the A what will be the change in the B right? if I take out this resistance R_a and R_b make it just for our own assumption making it much much simpler if I make this resistance to be 0. This is point A that which C is a capacitance of C_a and then in between point A and B we have a C adjacent or the coupling capacitance and then B to ground we have a C_b.

The change in A will have a change in B and that change we can easily evaluate or estimate using the voltage divider method.

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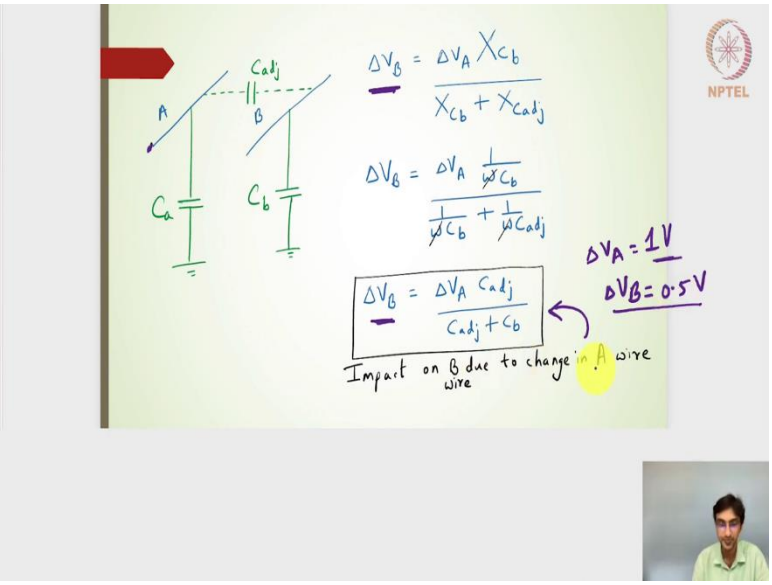

This is what we will have ΔV_B will be nothing, but the voltage divider this is the X is represents the impedance of the capacitance. We will eventually get ΔV_B the change in the wire B due to the change in the wire A.

$$\Delta V_B = \frac{\Delta V_A X_{cb}}{X_{cb} + X_{cadj}}$$

$$\Delta V_B = \frac{\Delta V_A \frac{1}{wC_b}}{\frac{1}{wC_b} + \frac{1}{wC_{adj}}}$$

The change in the wire A is intentional the change in the wire B is unintentional, that is not expected and that is something unwanted, but still because the change in the wire A is there change in the voltage for the wire A is there we will have some kind of a coupling effect on the wire B and that particular change will be nothing but given in this particular expression

$$\Delta V_B = \frac{\Delta V_A C_{adj}}{C_{adj} + C_b}$$

Impact on the B due to the change in A wire is given in this particular expression. If ΔV_B, ΔV_A is 1 volts and then C adjacent and C_b if it turns out to be the same, then if I can rewrite this as if it is 1 volt change because in a digital logic especially in a 65 nanometre technology node the logic at this particular end will be changing from 0 to 1.

The change in ΔV_A = 1V then the change in $\Delta V_B = 0.5$ V This will be the impact on B due to the change in the wire A. Hope this is clear?

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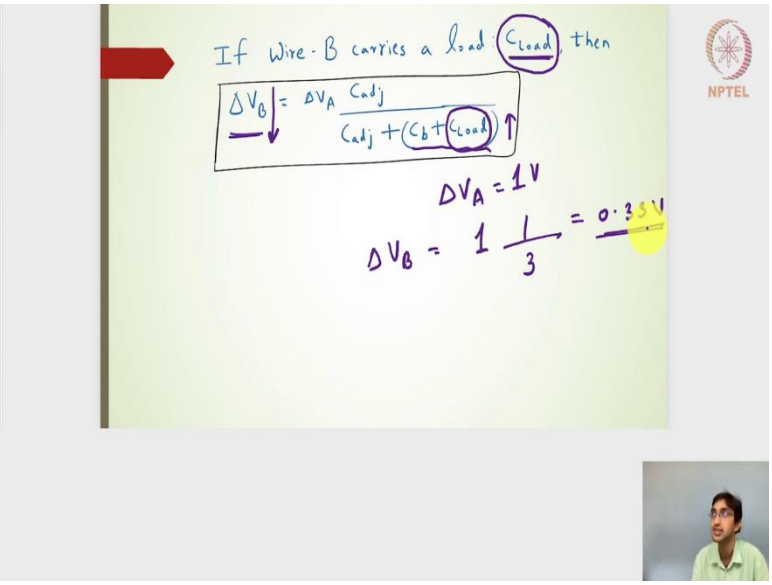

Moving ahead, if the wire B is carrying a load of C_{load} that means, that the wire B which was initially floating, let us say it is driving another load it is driving another circuit or an inverter or any other combinatorial circuit, then we can also represent that particular circuit on the load side with a C_{load} capacitance or a C input capacitance of that particular circuit will be loaded into this particular wire.

Then the overall change in B will be nothing but,

$$\Delta V_B = \Delta V_A \frac{C_{adj}}{C_{adj} + (C_b + C_{load})}$$

Having a load or having the wire B, driving the wire B driving another circuit will be useful in reducing the overall crosstalk effect because this particular parameter it can increase the denominator and then overall my ΔV_B is likely to reduce.

Now if I have $C_{load} = C_b = C_{adj}$ in that sense I will have a $\Delta V_B = 1V$ I then,

$$\Delta V_B = 1\frac{1}{3} = 0.33V$$

This 0.33 volts which is less than that of what we had seen earlier of 0.5 volts. Having a C_{load} or having the wire B connected to some particular circuit connected to some or driving to some particular combinatorial gate circuits that will be very useful.

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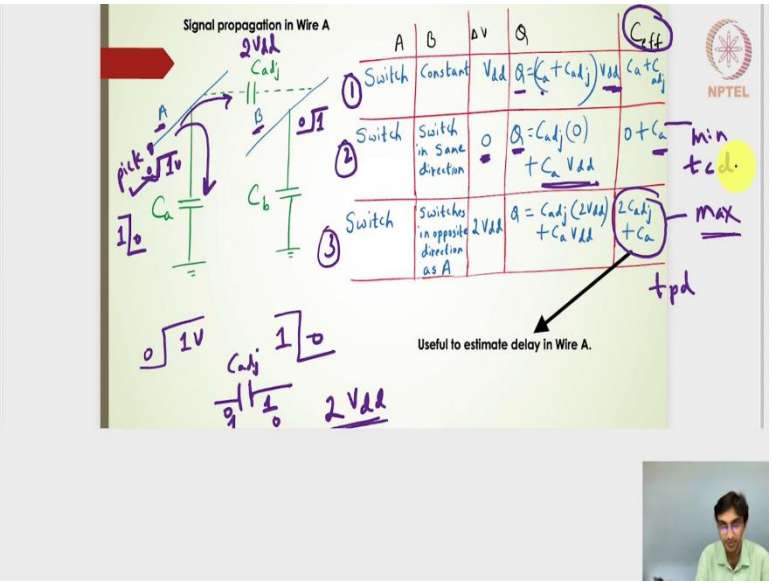

Now, let us take a look at this particular circuit or the representations and here I have the wire A and wire B and its associated capacitances I have neglected the resistance at this particular point of time and we will once again use the resistance or include the resistance to estimate whether it is a performance or the power later on.

We have a wire A and wire B which we can say that it is close by and then we have this C adjacent capacitance and the individual of this wire with respect to its layer below or above whatever it is, it will have its capacitance C_a and then C_b for the wire A and b respectively.

I have drawn a table here just to find out what is the effective capacitance that we have to consider for a change in the voltage for the wire A and the change in the voltage for the wire B, what is that effective capacity? that I have to consider especially, let me pick this wire A, what is that effective capacitance whether it is $C_a + C_{adj}$ that I have to consider.

Because if there is a change in the voltage here from 0 to 1 volts for the wire A and let us say that the B is grounded or connected to the V_{dd} rail through a transistor, let us say there is some particular inverter or a circuit which is driving this wire, its not loading it is driving this wire. Based on that particular input logic it will either be connected to ground or it will be connected to the V_{dd}.

Let us say that this is at a constant voltage or a constant logic and then if I have a change here in the wire A from 0 to 1 or 1 to 0 what is the effective capacitance I need to consider

for the wire A, that it actually charges or it discharges. If I have an effective capacitance, then I can estimate the overall delay for this particular conditions when the wire A is doing the transition and wire B is held constant, that will be one case.

Let us look at this first case A is switching the wire A is switching from 0 to 1 volts B is held constant either to 0 volts or to V_{dd} range or to the logic high. The ΔV the change in the voltage for the wire A will be nothing but V_{dd} so, 0 to V_{dd} or 0 to 1 volts. The charge that this particular driver circuit has to charge that has to charge this capacitance C_a it has to charge this capacitance C_{adj}, C_b is anyways held constant, no need to charge the C_b capacitance.

The overall charge will be nothing but,

$$Q = (C_a + C_{adj})V_{dd}$$

What I am saying is if I have a change step input here from 0 to 1 volts, then I will have to charge the C_a capacitance I have to charge the C_{adj} capacitance. The overall charge will be $C_a + C_{adj}$.

This particular 0 to 1 volts change will be brought by a driver circuit here which will be driving this particular wire. A driver circuit is connected it the output of the driver circuit is connected by an interconnect to another circuit.

If you assume that then a change here 0 to 1 volts will have to charge the capacitance C_a and the C_{adj} and similarly if it is doing the other way from 1 to 0, then the C_a and C_{adj} has to discharge. The overall charge in this particular case will be nothing, but $(C_a + C_{adj})V_{dd}$ it could be either the charging or the discharging.

The C_{eff} capacitance that we have to consider for this particular case of the wire A when it is switching will be nothing but,

$$C_{eff} = (C_a + C_{adj})$$

Hope this is clear the second case wire A and wire B. The wire A is actually switching from either from 0 to 1 or 1 to 0 wire B now it is not held constant. Let me pick up a small eraser, I am going to say that this is not held constant. In fact, it is actually changing in the

same direction in the sense if the wire A is changing from 0 to 1. This if I pick wire B is also changing from 0 to 1.

If wire B is also changing from 0 to 1. Initially the voltage in the C_{adj} when it was 0 and then 0 it was the 0 voltage across the C_{adj} and then when it has moved to 1 volts on the wire A and then moved to the 1 volts on the wire B, the C_{adj} the potential difference between the C_{adj} capacitance will still be 0. Actually there is no charge that has been delivered to the C_{adj} or rather the charge stored in the C_{adj} is actually 0.

The ΔVin this case that has to be provided by the driver circuit, A here driver circuit which is driving the interconnect A will be 0. The total charge Q will be nothing but,

$$Q = C_{adj}(0) + C_a V_{dd}$$

$$C_{eff} = 0 + C_a$$

The C_{adj} does not come into the picture because the wire A and wire B are actually doing the same side, in the same way it is actually doing the transition from 0 to 1 volts or 1 volts to 0 volts.

In both the cases the potential difference across the C_{adj} will be 0 that means, there is no supply or the discharging of the charges that has been stored in the C_{adj}. The third case A is switching, let us say it is switching from 0 to 1 volts, but now B is actually switching in an opposite direction. If A switches from 0 to 1 volts then the B actually switches from 1 to 0 volts.

The overall charge that needs to be delivered to the C_{adj} by this particular driver circuit will be nothing but $2V_{dd}$ because the potential difference here is it has been changed to $2V_{dd}$ times.

Initially the C_{adj} was 1volts here, it was 0 volts here. The potential difference was minus 1 volts and now it has become 1 volts here and 0 volts here. It is basically $2V_{dd}$ or 2 volts the change in the potential difference that means, the total charge that it needs to be accumulated will be,

$$Q = C_{adj}(2V_{dd}) + C_a V_{dd}$$

Anyways this has to be charged because it is rising from 0 to 1 volts, the C has to be charged from for V_{dd}. The effective capacitance in this case,

$$C_{eff} = 2C_{adj} + C_a$$

Notice that we have got three cases in one case it is the minimum C adjacent and in another case it is the maximum. The maximum C_{eff} capacitance will be useful in estimating the propagation delay whether it is falling or rising and the minimum one should be useful in calculating the contamination delay falling or rising because the less capacitance is likely to have a less delay.

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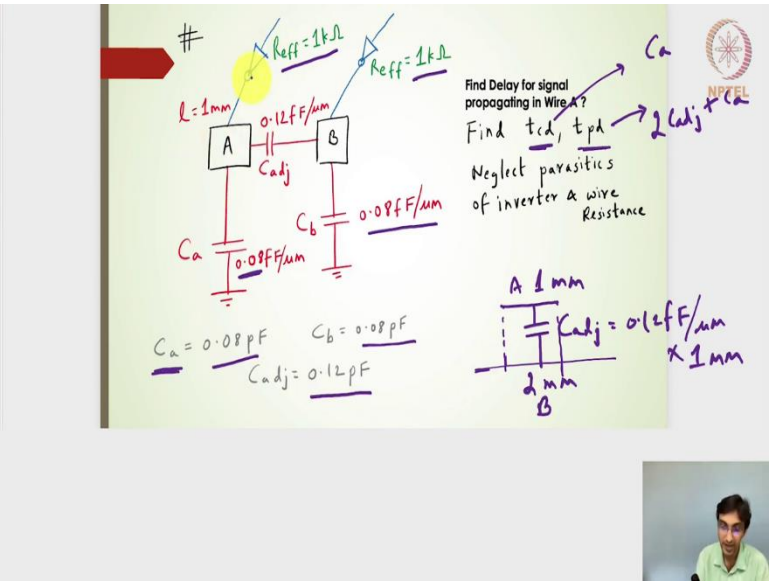

Going forward, let us say that I have a wire A and B and its adjacent capacitance is 0.12fF/μm, that has been characterized. Based on the wire length of the A or and the B wire we can estimate that what should be the C_{adj} capacitance. In fact, it turns out that whichever length is minimum here if A is 1 mm and B is 2 mm then the adjacent capacitance will always be with respect to the 1 mm.

Whatever is kind of aligned. In that sense what I am saying is if suppose A is this wire this is of 1 mm and let us say B is of 2 mm, this is the wire B. The capacitance will be nothing but with respect to this overlapping region and then this particular capacitance

$$C_{adj} = 0.12\text{fF}/\mu\text{m} \text{ x } 1\text{mm}$$

Its basically based on the A and B wire how much ever is the length that has been overlapping between the 2 wires that will be used for calculating the C_{adj} capacitance and of course we have the C_a and C_b which is 0.08fF/μm and then 0.08fF/μm for the C_a and C_b capacitance.

There are 2 driver circuits, inverter is there inverter is driving this interconnect. Its switching resistance is given as 1KΩ and its switching resistance is given as 1KΩ the length of the wire is 1 mm. If it is 1 mm wire and let us say that wire A and B are aligned properly then that means, that the overlapping length is still 1 mm.

Then in that case I should be able to find out what is C_{adj} and C_a and C_b, $C_a = 0.08fF/\mu m \text{ x} 1000m = 0.08pF$, Cb is also same 0.08pF, C_{adj} will be point 12pF. What we need to find is the delay of the circuit.

We need to find out the t_{cd} and t_{pd} propagation delay and contamination delay. For propagation delay the effective capacitance is nothing but $2C_{adj} + C_a$ and for the contamination delay we know that this is nothing but C_a.

If I consider one of the driving circuit driving this particular interconnect. How much time it will take from one end of the wire to reach the other end of the wire with this adjacent capacitance and with this C_a capacitance its own wire capacitance.

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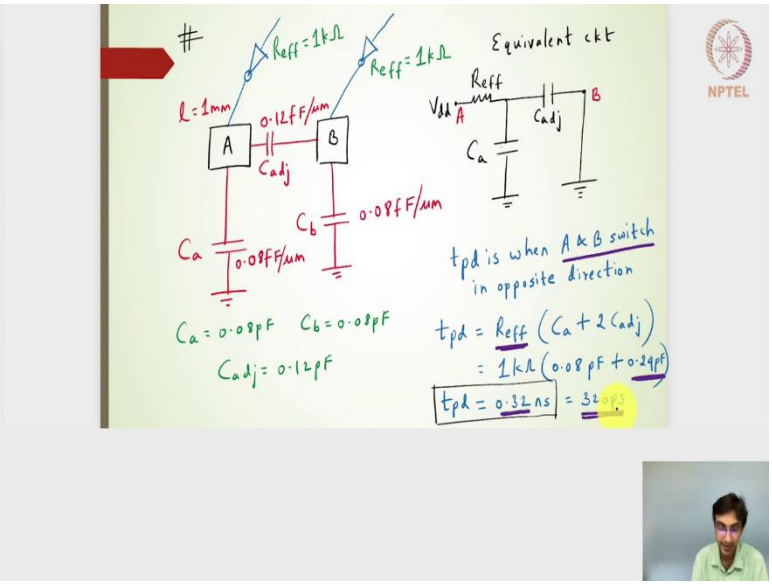

In that sense t_{pd} is when A and B are switching in the opposite direction and in that case t_{pd} will be nothing but,

$$t_{pd} = R_{eff}(C_a + 2C_{adj})$$

$$= 1k\Omega(0.08pF + 0.24pF)$$

$$t_{pd} = 0.32ns = 320ps$$

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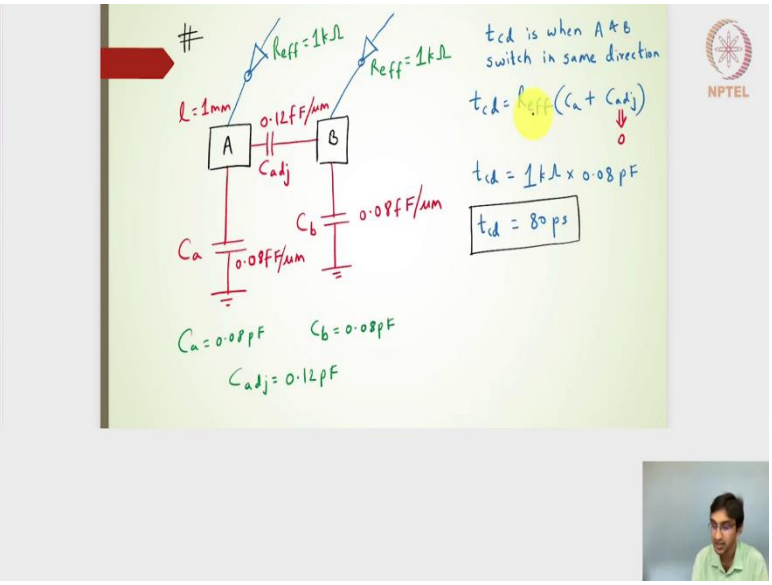

For the contamination delay it is,

$$t_{cd} = R_{eff}(C_a + C_{adj})$$

$$= 1K\Omega + 0.08pF$$

$$t_{cd} = 80ps$$