Design and Analysis of VLSI Subsystems
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Lecture - 52
Multiplexer design and layout

Hello students welcome to this lecture on Multiplexer. We will see the multiplexer representation in two forms, one using the transmission gates and another one using the tristate logic families.

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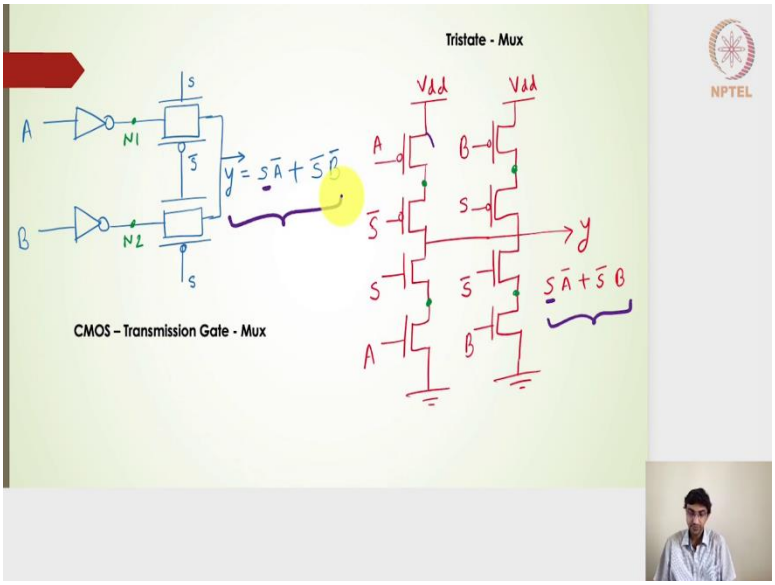

Moving ahead this is the transmission gate configured multiplexer circuit and it is a 2:1 multiplexer and I have represented in a very very simple manner. Let us say that when S = 1, when the select line is 1 here. I will have this transmission gate passing in the input to the output y. If S=high $\overline{S}$ =low and this particular transmission gate will be working.

This particular transmission gate will not be working because this $\overline{S}$ is connected to the NMOS here and an S is connected to the PMOS. When S=1 this will not work, only when S=0 this transmission gate is going to pass the input to the output. What happens is when S=1 we will have whatever is the input here will be passed to the output and the input here is nothing but the inverted, it is basically the inverter output of the signal A. I will get when S=1, I will get the output will be nothing but $\overline{A}$ and then when S=0 the output will be $\overline{B}$.

$$y = S\overline{A} + \overline{S}\overline{B}$$

This is one form of building the multiplexer circuit 2:1 multiplexer using the transmission gates, the another form of building the multiplex is the tristate multiplex. The tristate it has basically the mirror topology and not the conduction complement topology. The mirror topology means whatever we have the circuits in series on the pull down side the same series of the transistors will be there on the pull upside.

Here A is given to the PMOS transistors and to the NMOS transistor which are closer to the rail and the select signal is given to the PMOS and NMOS transistor which are closer to the output node. When A=1 in this particular case or rather when the select is 1 here, when S=1 this will be on and then this will be on because S=0 and this PMOS will be on. The output will be nothing but whatever is the based on the A the output will be nothing but $\overline{A}$, the complement of the A signal.

When S=1, I said this will be on and this will be on, this particular transistors which are there on the next leg or the next branch this particular transistors will be off and thereby y will not be connected to the transistors are connected to the B. The y will be connected only to the transistors of the A transistors on the PMOS and NMOS side and it will give me the complementary output of the A signal.

When S=0, this one will be on and this on, S will be 0, $\overline{S}$ will be 1 and the NMOS transistors here will be on and then S will be on here. The y will be the complimentary of the B signal and these two transistors will be off and thereby y will be disconnected from the A transistors. When S=1, I will have the y output will be nothing but when S=1, I will have an $\overline{A}$ output and when S=0 that means, $\overline{S}$ in to B, we will get this particular expression very very similar,

$$y = S\overline{A} + \overline{S}B$$

In fact, it is same as that of this particular expression, although the schematics or the circuit design is different. One is from the tristate family and another one is the transmission gate family.

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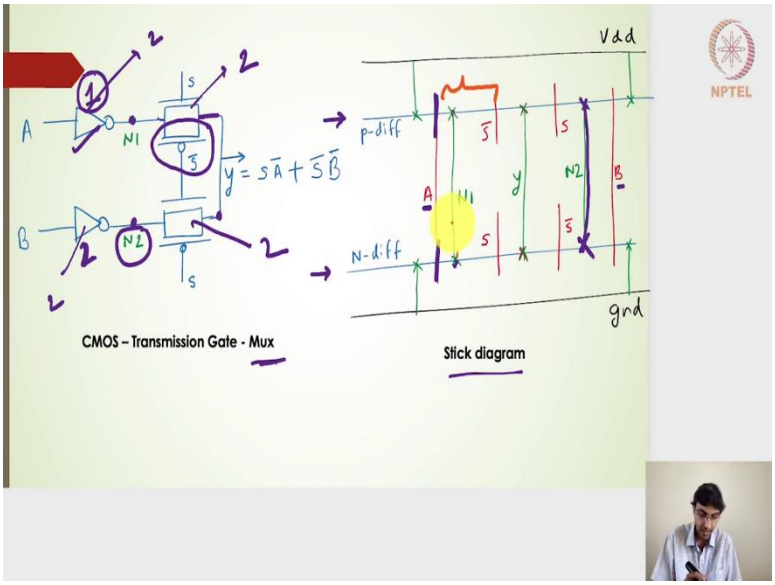

Hope this is clear. What I have done here in this particular slide is I have drawn the stick diagram basically the layout for the CMOS transmission gates configured multiplexer circuit. Let us have a look into this particular stick diagram very closely. In this particular stick diagram, I am going to pick up the transistors A and B, basically the inverters A and B. The inverters A and B here 1 and 2 I am going to pick. I am going to talk about 1 here first. In this particular stick diagram the A is nothing but given to the polysilicon gate.

This is the polysilicon gate and on either side I will have the diffusions, on the either side I will have the one diffusion of the PMOS side. If I consider the PMOS diffusions and NMOS diffusions I will have the polysilicon gate and on either side, I will have the diffusions drain and the source. One is connected to the source of the PMOS transistor is connected to the V_{dd}.

The source of the NMOS transistor is connected to the ground rail alright. Here I want to emphasize that the PMOS the P-diffusion and N-diffusion represents that wherever you will see a polysilicon gate that represents an NMOS transistor on an N-diffusion line. Similarly, on the P-diffusion line wherever we see a polysilicon gate that represents one PMOS transistors on the P-diffusion line.

In this case the A is cutting here, that means, that I need to have the diffusions to make the NMOS and then the PMOS transistors complete. What I have done is on one side of the

diffusion it is connected to the V_{dd}, the another side it is connected to this particular N1 node. Similarly, for the NMOS transistors on the N-diffusion line one diffusion is connected to the ground the other diffusion is connected to the N1 node and this N1 node are connected together because it is an inverter.

The PMOS transistor diffusion and then the NMOS transistor diffusion are connected and that is this particular metal line. This particular realization of this inverter onto the stick diagram is complete, let us go to this second inverter which I have drawn it at the end here. B polysilicon line cutting the P- diffusion and N- diffusion on one side of the diffusion it is ground the other side of the diffusion of the PMOS it is V_{dd}.

The other side is connected to the N2. This is the N2 line which is a metal line which is connected here. These two inverters are done or realized in the stick diagram or in the simpler representation of the layout. Let us go to this particular transmission gate. In this particular transmission gate I have two transistors, NMOS and PMOS. PMOS is S, the PMOS input or the PMOS gate is connected to the S bar and NMOS gate is connected to S input.

What it means is on the P-diffusion if I should have an $\bar{S}$ polysilicon gate on the N-diffusion I should have an S polysilicon gate. So, have an S polysilicon gate and polysilicon gate $\bar{S}$ on the P-diffusion side and S on the N-diffusion side. Once I have that I know the diffusion side is N1 here, this is N1 point and on the other side this is the y point. On the either side of $\bar{S}$ it is N1 point and then the other side is the y point.

Similarly, for the N-diffusion S polysilicon gate one side it is N1 the other side of the diffusion is y and that is what I have represented, S polysilicon gate one side it is N1 the other side is y. This particular point y is actually connected. The diffusions are connected that is why I have this y. This is a y metal line and let us talk of this particular transmission gate, this particular transmission gate if you look closely this $\bar{S}$ is going to the NMOS transistor and S is going to the PMOSs transistor.

I should have an $\bar{S}$ polysilicon gate for the NMOS transistor that means, $\bar{S}$ cutting the N-diffusions and S as the polysilicon gate connecting to the PMOS transistor. S is now the polysilicon gate on the P-diffusion lines. Creating two diffusions on one side it is the N2 N1 and another side it is the y for the both the PMOS transistor as well as the NMOS

transistor. S and $\bar{S}$ on one side it is y signal the other side it is N2 signal, that is what it is represented. This completes the stick diagram representation of the CMOS transmission gate. The CMOS transmission gate derived multiplexer circuit, hope this stick diagram is very very clear.

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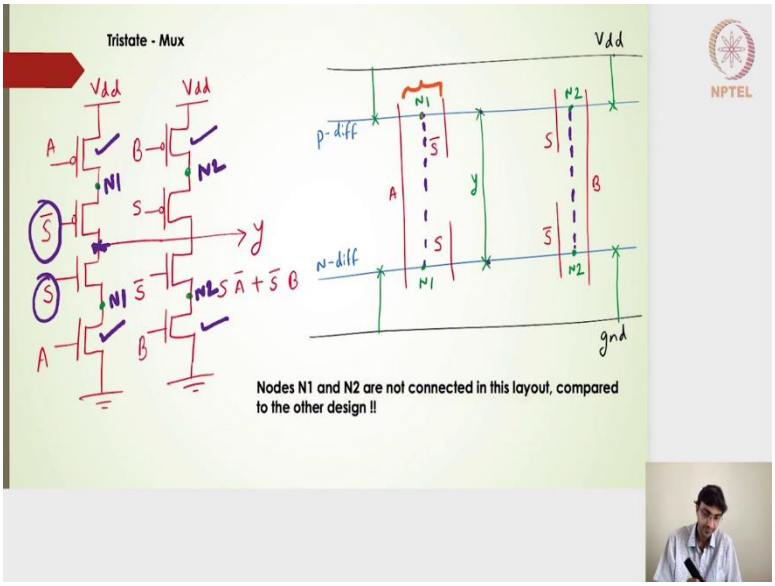

It is very interesting to see the stick diagram of a tristate multiplexer, the tristate circuit diagram is given here and there are you know there are 8 such transistors alright. What it means is basically I should have 8 such polysilicon gates, 4 polysilicon gates on the P-diffusion lines and 4 on the N-diffusion lines so that we will get 4 transistors each on the P-diffusion and then the N-diffusions.

If I go back to the previous slide, I also had 4 polysilicon gates on the N-diffusion and P-diffusion lines creating 8 such transistors and why 8? Because you know this is basically 2 transistors and this is 2 transistors and this is 2 transistors so total 8 transistors. Same thing we will see in the tristate multiplexer also we will have 8 transistors, 4 on the P-diffusion line 4 on the N-diffusion lines.

Let us look into the first branch, the transistors A or rather the transistors which are connected to the A signal. If I pick this particular transistor on the P-diffusion line the polysilicon gate is nothing but A, and on one side it is connected to the V_{dd} the other side this is N1 node. That is what I have written N1 node and if I pick this particular transistor

now, on the NMOS side on the N-diffusion side I have the A polysilicon gate and on one side I will write it as N1 and on the other side it is the ground.

This is completed and similarly I can complete the B transistors here, the B transistors here on the B polysilicon gate on one side of this particular diffusion it is connected to V_{dd}, the other side it is the N on the NMOS side it is connected to the ground. The other side of the diffusion is I can write it as N2 and then N2. Note that N1 and N2 are not connected here, in this tristate multiplexer alright.

If I go back to the previous slide N1 here was actually connected, N1 and N2 are connected in the sense the output of the inverter, the output of the inverters which is the output of the inverters this one in the stick diagram. On both the diffusions of the P-diffusions and N-diffusions has to be a single point in the schematic that means, there is a wire that is connecting the PMOS diffusion and NMOS diffusions.

N1 was actually connected between the PMOS and NMOS diffusions, similarly N2 was connected between the PMOS and NMOS diffusions. If I look closely now into the tristate multiplexer design and it is a stick diagram, the N1 is an unmerged a diffusion rather it is a merged uncontacted diffusion, here I mean the diffusions are merged. The diffusion of this particular transistor and this particular transistor are actually merged, but there is no metal line.

Whereas, in the previous case of the transmission gates design multiplexer you can see that the transistors A here on the P-diffusion side and on the $\bar{S}$. I am talking about this particular transistor and then I am talking about the inverters of PMOS transistors. This particular line, let me draw this. This particular line is a merged diffusion because there are two transistors I and the diffusions are merged, even then the diffusions are merged there is a contact here.

The metal line is going around that is why it is called as a metal contacted merged diffusions whereas, here we do not have any metal line that is passing on from N1 to N2. It is an uncontacted it is an non-metal contact, but it is a merged diffusions. It is merging with that of the $\bar{S}$ signal here, so $\bar{S}$ signal that is having a merged diffusion with that of the A transistor and S bar transistor. I have an S bar polysilicon gate on one side it is N1, the other side it is the output y.

Similarly for the S signal, S transistor on the NMOS side I have a polysilicon S on one side it is N1 the other side it is y. Now, remember that the y are connected here means it is indicated by a point here on the PMOS transistor and then the NMOS transistor. That means, that the y has to be connected, there is a metal line that is going around and connecting this particular point and then this particular point.

To complete the other part we have anyways completed the B transistors. We have to complete the S and the $\bar{S}$. I have an S on the PMOS side. S and on one side the diffusion is N2 the other side it is y and similarly $\bar{S}$ polysilicon gate, on one side it is N2 the other side it is y. This complete a stick diagram and if I look closely into this particular stick diagram with respect to the previous one, the only difference here is this particular contact line is missing.

Otherwise, the tristate derived mux is also having a similar stick diagram as that of the transmission gate derived multiplexers, the only thing which is missing is the dotted lines which is the metal lines, that is what I have written nodes N1 and N2 are not connected in this layout compared to the other designs.

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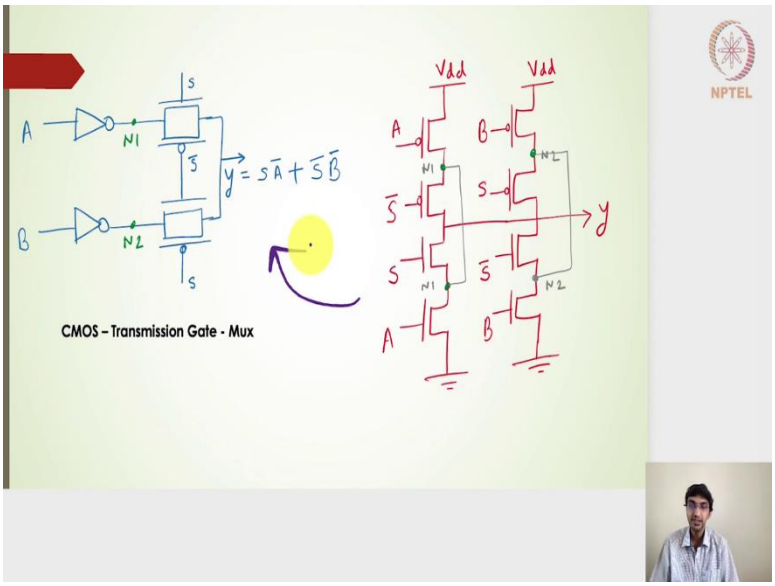

The transmission gate multiplexer and then the tristate multiplexer the schematic I have designed, we notice that the stick diagram is different by only 1 by only one metal contact. The stick diagram if I actually connects the schematic with this N1 and an N2 connection

this behaves very very similar to that of the CMOS transmission gate designed multiplexers.

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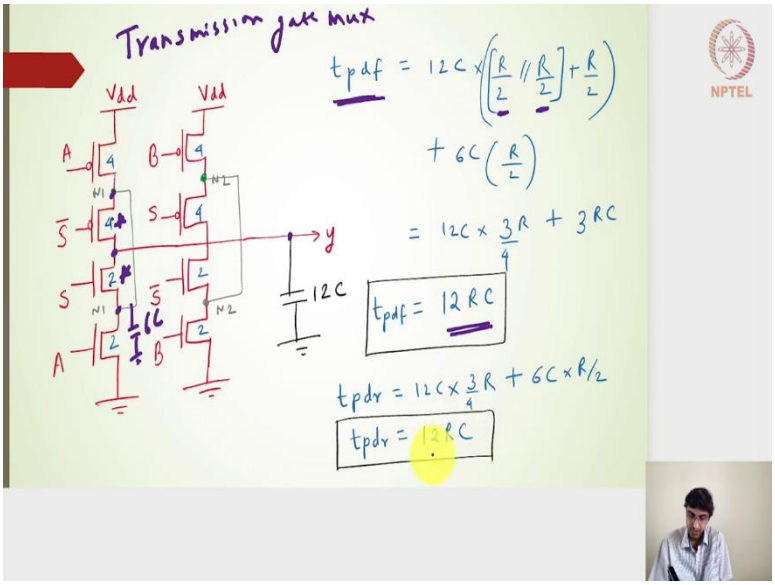

Now, what is the advantage of this? this is a tristate design, but now I am connecting this N1 and N2 nodes so that means that this now behaves like a transmission gate multiplexer, because it is behaving also I have drawn this like a tristate logic family, but because of this connections between N1 and N2, N2 connected to the N2 here and N1 connected to the N1 here.

The stick diagram of this represents the transmission gate multiplexer and this is now a transmission gate multiplexer and in a transmission gate multiplexer I wanted to find out what is the delay. If I size it properly 4, 4, 2, 2 so that I will get the switching resistance of R and then R here on this branch on the pull down side and 4 and 4 will give me the switching resistance of R on the pull upside.

The t_{pdf} will be nothing but as I have calculated here. The capacitance seen at the output node will be nothing but 4+2+4+2=12C. The capacitance here will be nothing but 4 which is a merged capacitance from these two transistors and then one more 2C merged capacitance from these two transistors 2C, 6C will be the overall capacitance. If I want to find out the propagation delay falling, it will be nothing but 12C and then now we will

have this resistance and this resistance in parallel and then it will have a in series resistance of $\frac{R}{2}$.

I will have an $\frac{R}{2}$ and $\frac{R}{2}$ in parallel because this node and this metal node are the same now and this side it is nothing but y. I will have a y line and the switching resistance of this and then this will be in parallel with that of in series that of 2 the $\frac{R}{2}$. That is why I have parallel $\frac{R}{2}\frac{R}{2}+\frac{R}{2}$ and then the 6C x $\frac{R}{2}$ that is the switching resistance so overall I will get 12 RC.

$$t_{pdf} = 12C\left(\left[\frac{R}{2} \,||\, \frac{R}{2}\right] + \frac{R}{2}\right) + 6C\left(\frac{R}{2}\right)$$

$$= 12C\,x\frac{3}{4}R + 3RC$$

$$t_{pdf} = 12RC$$

The tpd rising the propagation delay for the rising will also be very very similar,

$$t_{pdr} = 12C\,x\frac{3}{4}R + 6Cx\frac{R}{2} = 12RC$$

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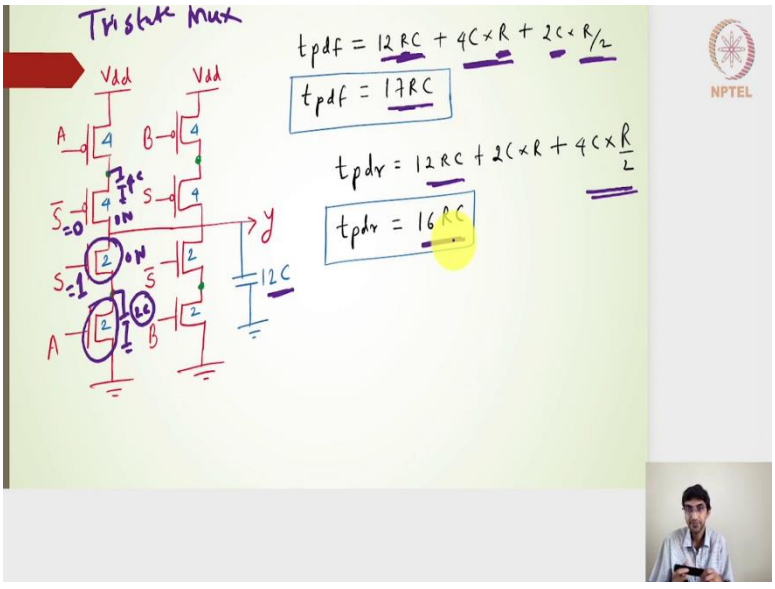

This is the delay for the transmission gate multiplexers where the N1 are connected on both the PMOS and NMOS transistors and N2 are connected on the PMOS and the NMOS transistors. For a tristate based multiplexers what should be the delay? Tristate multiplexers means this particular nodes are not connected alright. In that case I will see a total capacitance of 12C, there will be a capacitance of 4C here and 2C here. I can similarly draw it here and here, but let us say that under this particular branch we are interested in. For that propagation delay falling I will have this 12C x R. This transistor and then this transistor will give me a resistance of R and then this 2C x R/2. This 2C x R/2 is this one and then this is a 12RC which is output node capacitance multiplied by R.

Remember that for even for the falling one this S=1 that means, this transistor is on, this $\bar{S}$ = 0 and then this transistor will also be on. That means, this 4C capacitance will also be considered for the falling output and as for the Elmore delay method 4C x R should be accommodated. The totally 17 RC which is greater than the 12 RC.

$$t_{pdf} = 12RC + 4C \times R + 2C \times \frac{R}{2}$$

$$t_{pdf} = 17RC$$

Similarly, tpdr that means, the propagation delay for the rising one will be nothing but,

$$t_{pdr} = 12RC + 2C \times R + 4C \times \frac{R}{2} = 16RC$$

I will have a 16 RC and then 17 RC again 16 RC is much is also greater than that of the 12 RC which we have seen for the transmission gate derived multiplexers.

This is a very small analysis on the multiplexer designs. We have two different multiplexer designs, one is the tristate based and another one is the transmission gates. The tristate based multiplexers the layout of both of them will be very very similar, the advantages with the tristate multiplexer is the metal line is not there, additional two metal lines does not come into the picture.

Which is good in the sense that additional metal lines will cost us little bit more, but whereas, the delay in terms of the tristate multiplexer it is more than that of the transmission gate because the metal line is connecting and then it makes the switching

resistance less. Because the equivalent switching resistance for the two transistors which are in parallel, it reduces the switching resistance and thereby the delay will also naturally be smaller.