Design and Analysis of VLSI Subsystems
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Lecture - 51
Applying Eulers path for stick diagram representations

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Hello students, welcome to this lecture. This is the second part of the Stick Diagram Representation and in this particular lecture, we will talk more about a particular way of designing or ordering the polygates so that we can complete the stick diagram very efficiently.

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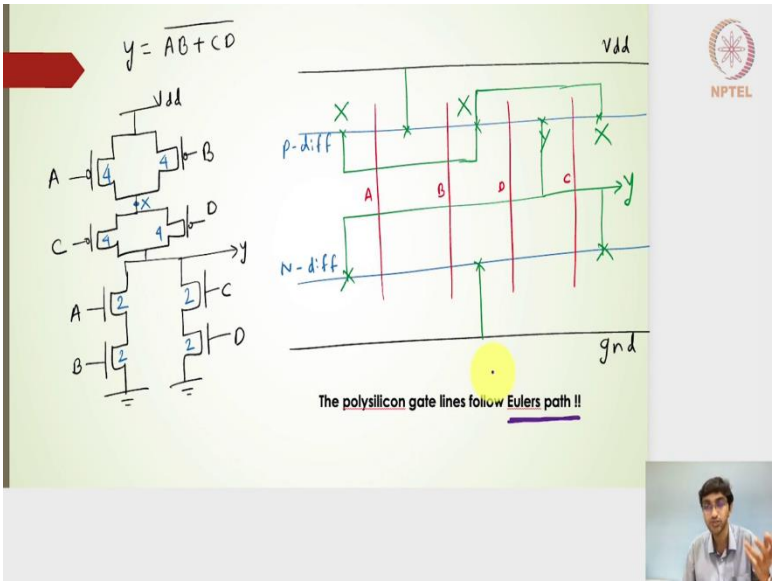

This is what we had seen in the last lecture. We had a combinational circuit of $\overline{AB + CD}$ and then the inverted in the form of that or the complement form of that. The schematic is given on the left hand side where we have the inputs A, B, C, D connected to the pull up circuit and then the pull down circuit. We have the PMOS transistors and then the NMOS transistors completing this particular combinational circuit.

What we had seen in the last class was the ordering of the polysilicon gates where the order should be A, B, D, C and not A, B, C, D. It has to be in an order of A, B, D, C so that we can use the merge diffusion and then contacted merge diffusions or an uncontacted merge diffusions. Remember that if you have the merged diffusions then the overall layout or the overall stick diagram can be very very compactly designed.

What we will do in this particular lecture is try to follow a particular method called as Eulers path. The Eulers path will help us in designing the polysilicon gates A, B, D, C or rather I will say that it will help in ordering our polysilicon gates. For this particular circuit if we were to design the polysilicon gates in the layout instead of A, B, C, D it will be the order will be A, B, D, C and that has been arrived or that has been deduced from the Eulers path.

Although, we have not seen the Eulers path. We just took one such example instead of A, B, C, D if you use A, B, D, C then we can get a compact one. We will see how to use the

Eulers path for designing the stick diagrams and then estimate what should be the overall footprint.

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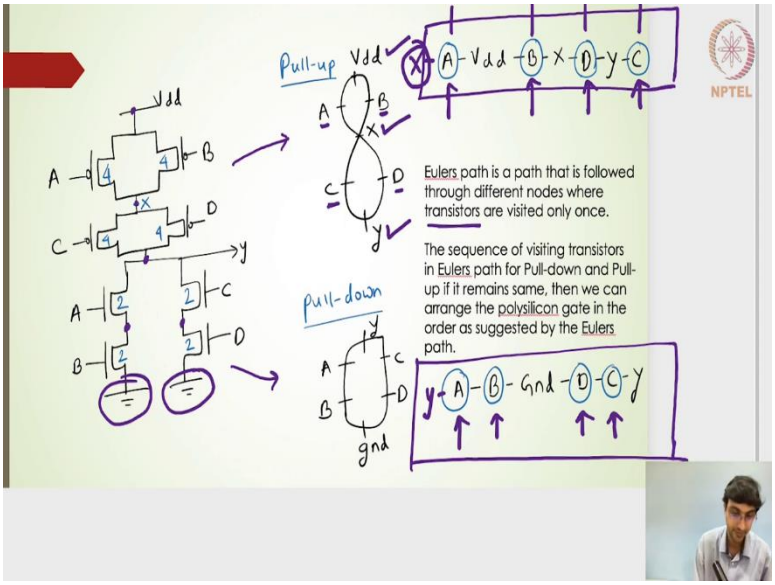

The Eulers path especially for this particular circuit. Let us try to define this, I have actually put 2 Eulers path one for the pull up circuit and then one for the pull down circuit. The Eulers path recognises all the nodes in the circuit design.

In this particular pull up path we can say that V_{dd} is one node, the x is another node and then of course, the y is another node, there are three nodes in the pull up side. Then in the pull down side we have the y output node is one node and then there is one the merged diffusion which is uncontacted one and then there is a ground one this and this ground are same. I will have y output node and then this one node and then the ground node and then we will have one more node. The Eulers path for the pull up and pull down circuit should consist of all the nodes that are available in the schematic so that we need to represent that in the Eulers path. In the pull up side I have written the nodes of V_{dd}. I have written the x node and then I have written the y node and in this particular path if you are trying to visit from one node to the another node, we will also try to label or annotate the polysilicon gates or rather the input to this particular PMOS transistor which is nothing but the polysilicon gates. While I am traversing from one node to another node let me also write or label the polysilicon gates here which is $\overline{AB + CD}$. In this particular Eulers path on the pull up side we will see that it forms a shape.

If I am starting from V_{dd} to x node. I will traverse the B node right and then from x to y I will traverse either the C or the D node and then traverse back to the x node with the left out node whether if it was the C node which I have traversed earlier, then I will use the D node path, and then it will traverse back to the V_{dd} through the remaining polysilicon gate.

Just to reiterate, I will travel from node V_{dd} to x node you know traversing the B polysilicon gate and then from x node to y node, I will traverse using the C polysilicon gate and then from y to x node using the D gate and then from there to the V_{dd} traversing the A polysilicon gate.

That is one particular path, but this particular path it is actually says that it is revisiting the node and traversing the polysilicon gates only once. I can also have multiple combinations, I can have one combination starting from whatever I have written here.

Starting from the polysilicon gate A that means, that it starts from the x node passes the polysilicon gate A and then goes to the V_{dd} node and then comes back to the x node through the B polysilicon gate and then goes to the y node through the D node, D polysilicon gate and then from y to x back traversing through the C polysilicon gate.

The nodes could be multiple visits to the nodes, but the polysilicon gates here should be visited only once. The nodes could be visited multiple times, but the polysilicon gates has to be visited only once and similarly on the pull down side we will have one particular path starting from y to A to B and then to ground and then traversing back to D and C back to y.

Here also I have the polysilicon gates A, B, D, C and here also I have the polysilicon gates traversing in the order of A, B, D, C. If I define the Euler paths where the polysilicon gates are visited only once for both pull up and pull down side. If the order of the polysilicon gates on the pull up and pull down side matches then we are bound to get a compact footprint, that is what I have written here

Eulers path is a path that is followed through the different nodes and multiple visits through the nodes, but where the transistors are visited only once. The sequence of visiting the transistors in the Eulers path for both pull down and pull up, if it remains the same then we can arrange a polysilicon gate in the order as suggested by the Eulers path.

In this particular schematic what we had seen is the pull up and pull down circuit we have got the same order of polysilicon gates that is A, B, D, C on the pull up side and A, B, D, C on the pull down side and then this order if it matches then we can get a compact circuit.

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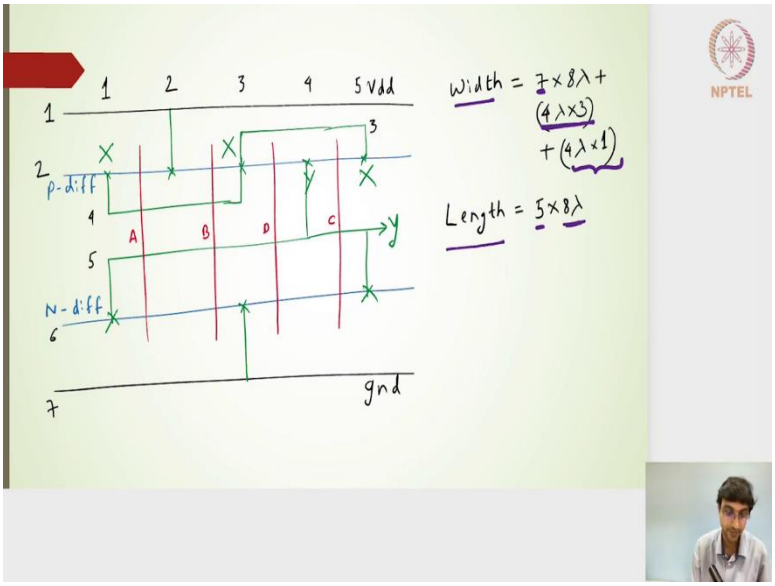

Moving ahead, this is now the stick diagram and this is something we had already seen. So, I have a V_{dd} rail, I have a ground rail, I have a P diffusion I have an N diffusion and I have the polysilicon gates A, B, D, C that is the order which is suggested by the Eulers path and this gives us the compact design and then the width of this and then the length of this is stated here. Let us now have a look at the overall width of this particular stick diagram.

For estimating the width of this particular stick diagram, we need to number the metal tracks. The number of horizontal metal tracks will be 1, 2 second is for the P diffusion line and then we have the 3rd line here and then the 4th line here and then the 5th line which is nothing but connects to the output node.

The 6th one is the N diffusion line and then the 7th one is the ground rail. I have total 7 metal rails x 8λ. But, if you look at the sizes of this gates of this transistors, if I go back if I notice the sizes it is actually different than that of the scaling of one. If I have the size of 4 and 4 here on the PMOS side and 2 and 2 on the NMOS side, my P diffusion line is not any more 4λ it is it has to be 12λ.

On the N diffusion side, the N diffusion line is not anymore 4λ it is now 8λ. Moving ahead. I now have 4λ x 3 = 12λ has to be accommodated in this particular in a footprint for the P diffusion line and on the N diffusion side I have to accommodate additional 4λ x 1.

$$\text{width} = (7 \text{ x } 8\lambda) + (4\lambda \text{ x } 3) + (4\lambda \text{x} 1)$$

The overall length of this particular footprint if I want to track the number of metal lines it is nothing but this particular metal line is one, the second one is this one, the third one is this one, fourth one is this particular line and then the fifth one is this particular line which is aligned here.

$$\text{Length} = 5 \text{ x } 8\lambda = 40\lambda$$

Multiplication of this width and length should be able to give me the overall footprint in terms of λ square. Of course we can always identify what should be the absolute the footprint by considering λ with regards to the technology node.

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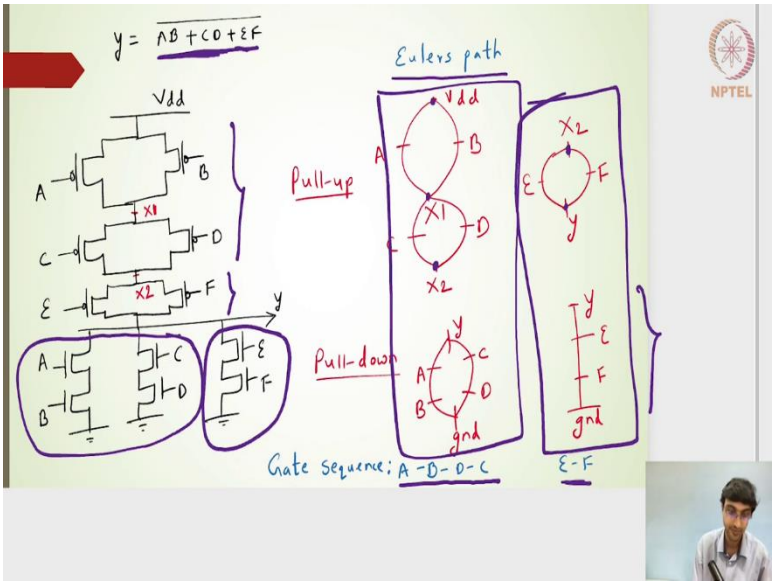

Moving ahead this is one more example where we have the combinational circuit of $\overline{AB + CD + EF}$. Last time we had seen $\overline{AB + CD}$. Here I think there is one more two additional inputs E and F.

This is the circuit the schematic diagram in the transistor level. I have AB in series and then that is in parallel with that of the CD transistors which will be in parallel with that of

the EF transistors which are in series and because its a conduction compliment I will have the AB on the pull up side I will have A and B in in series with that of CD and then in series with that of EF transistors. I have not written down the sizes of these transistors that we will have a look at it later.

If I want to use the Eulers path, I will identify all the nodes in the pull up side and in the pull down side and then try to traverse through the nodes visiting the polysilicon gate only once, I will try to do that. I have identified the nodes V_{dd}, I have identified X_1 node, I have identified X_2 node and, then I am trying to form a path. Here the path is again you can have an A V_{dd} B X_1 and then D X_2 and then C X_1.

I cannot have X_2 going to y without traversing the polysilicon gate only once and that is why I have separated it out now. Now, I have actually separated it out the X_2 and then y where it is traversing from X_2 to y and then y to X_2 through the polysilicon gate C and F. I cannot have actually A B and then D and then go to E F and then cover back C, that will be difficult. In that sense what we have done is we have separated it out and then on the pull down side we will have again because on the pull up side we have A B C D as one particular path and then E F as another path.

We will also cover the paths of A B C D on the pull down side in one path and then E and F on the another path. On the pull down side we now have y connected to the ground via the A and B polysilicon gates and then coming back to y via the D and C polysilicon gates and that will be for this particular path, and then we will have for this particular path we will have the X_2 go to the y via the E and F polysilicon gates. Then on the pull down side we will have the y connected to the ground via the E and F polysilicon gates.

The gate sequence which is actually matching with the two Eulers path now for the pull up and pull down side. If I consider this particular path, I will now have a gate sequence of A, B, D, C which is matching for both pull up and pull down side and here it is matching with that of E and F.

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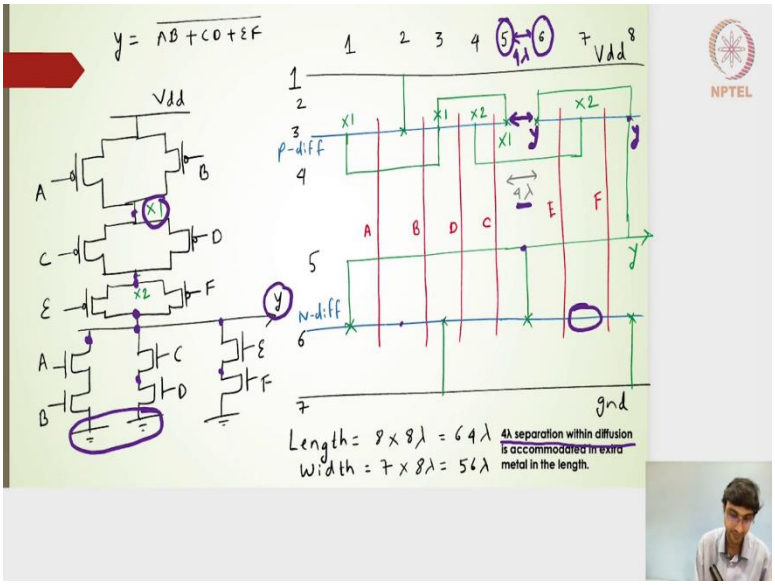

I will not now draw the stick diagrams where the order of the polysilicon gates is A, B, D, C and then E and F. The A, B, D, C path will remain the same it is very similar to what we had seen in the previous case. E and F it is very interesting. I have now the nodes X_1 and also I have the node X_2 here. X_1 is here and then I have written the X_2 node here. Then I have to draw the E and F polysilicon gates. Notice, that there is a separation indicates that the transistor E and F has one merged diffusion that is this X_2 node.

On the other side it has a merged diffusion node which is a y output node. This is the y_1 for the F transistor and then somewhere there is A and then this is a y node for the E transistor on the other side it is the X_2 node. Now, this y and then this X_1 this y and X_1 are not connected and therefore I should not have these diffusions to be connected. I cannot have the merged diffusion here that means, that there should be a separate diffusion.

If there is a separate diffusion, this distance between the diffusion should be a minimum of 4λ. It should have a 4λ separation on the pull up, on the pull down side I have the A, B, D, C and then I have the E and F polysilicon gates. The A, B, D, C it is very similar to the previous case and then the y output node will come to the x diffusion here and then A and B will have a merge diffusion and then you have the D and B, the merge diffusion gets connected to the ground that is what I have here.

D and C will have the uncontacted merge diffusion and after C is the output y. That gets connected here which becomes the merged contacted diffusion between the C and E

transistor. I will have the merged contacted diffusion which goes to the output node y and then E and F will have this particular portion is an uncontacted merge diffusion. Finally, the diffusion of the F transistor will get connected to the ground.

Notice that there is a separation of 4λ that is very much required otherwise the X_1 and y point will be the same. If I now want to find out what is the number of horizontal tracks and then the number of the vertical tracks, here I will have the vertical tracks as 1, 2, 3 and 4, 5, 6, 7, 8 and a horizontal tracks including the P diffusion and N diffusion lines will be 1, 2, 3, 4, 5, 6 and 7.

The overall length will be,

$$\text{Length} = 8 \text{ x } 8\lambda = 64\lambda$$

$$\text{Width} = 7 \text{ x } 8\lambda = 56\ \lambda$$

Of course, 4λ separation within the diffusion is accommodated in the extra metal in the length. What I meant was the 5th and the 6th line anyways has a separation of 4λ which is anyways taken care for the separation of the diffusion. I need not have to accommodate this extra 4λ.

But, mentioning that there is not a straight line is very important because then if its corrected although there is a separation of 4λ between the metal lines, what it indicates is that diffusions are connected. So, you have to ensure that in the stick diagram as well as in the layout there is this separation right those lines, P diffusion lines are not there.

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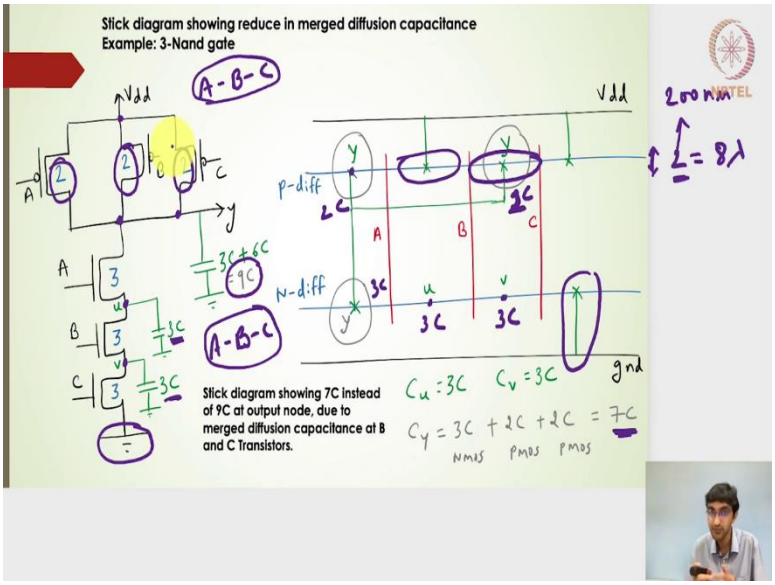

The last one, here is a stick diagram just a 3-input NAND gate stick diagram. The schematic is given here and then I have drawn this the stick diagram, here the stick diagram is very very simple, here the V_{dd} line and then the ground line and then P diffusion and then the N diffusion line.

Let me try to complete this particular stick diagram. If I consider the A transistor B and C transistor, A, B, C and then in this order. The Eulers path will go to A to V_{dd} to B to output to C to V_{dd}. I will have on the pull up side I will have the order of polysilicon as A, B, C and then on the pull down side the Eulers path will give me the order of A, B, C this y to ground I will get an order of A, B, C. In that sense I will have the orders matching and then I can have a very compact stick diagram or the footprint design.

That is what I have drawn here the polysilicon gates A, B, C. On one side of the polysilicon gate it is the connected to the V_{dd} and both B transistor and A transistors are connected to the V_{dd} that means, that the A polysilicon and B polysilicon the merged diffusion have connected it to the V_{dd}.

On the other side of A it is connected to the y output node and D is also connected to the y output node, on the other side it is connected to the y output node. On the other side of the B you know this B and C we can consider it to be a merged contacted diffusion and then it gets connected to the y output node.

The other side of the v will go to the V_{dd}, this completes the connections of the diffusions. On the pull up side on the pull down side I have the A, B and C the merged uncontacted diffusion here. A and B wherever it meets it is this particular point which is u point and B and C wherever it meets or the merged diffusion is there that is the v point.

The last diffusion on the C transistor is anyways connected to the ground, that is implied here and the first diffusion of the A transistor is connected to the output node. The first diffusion of the A transistor is connected to the y output alright. This particular stick diagram I have drawn this not to estimate the overall footprint, but just to estimate what should be the overall capacitance.

In terms of schematic, if I want to estimate the delay I will actually draw the parasitic capacitance, the inter node diffusion capacitance and then try to evaluate the delay in terms of R and C values. Here what I have done is I have taken the capacitance two from the A transistors on the PMOS side another 2C capacitance from the B transistor and another 2C capacitance from the C transistor and then the 3C capacitance from this side indicating a total of 9C capacitance and this is what we have been doing the inter node merge diffusion capacitance on the NMOS side we had taken or considered 3C and then 3C here, but if I really look into the stick diagram right especially on the pull up side there is a slight difference.

If I consider the u point here on the pull down side I will see a merged diffusion and if the width is 3, I will get a capacitance of 3C and v point also if it is a merged diffusion I will get a capacitance of 3C. On the pull up side this B and C transistors are actually having a merged diffusion capacitance and a contacted the merged diffusion capacitance, the diffusion is actually single.

This particular point is going to give me a capacitance of 3C or rather a capacitance of 2C because the width here is 2 that means, I will have 8λ scaling. Whatever is that it is the scaling of 2 implies that it is 200nm not 100nm. 100nm will give me a capacitance of 1C, 200nm will give me a capacitance of 2C for one diffusion.

Since B and C are actually merged I will get only one 2C capacitance A will give me one 2C capacitance. The total capacitance coming from the PMOS side is actually 2C and then 2C and then on the NMOS side it is actually 3C. The total capacitance turns out to be 7C here rather than what we have been using is the 9C capacitance.

$$C_y = 3C + 2C + 2C = 7C$$

This is actually very very useful in that sense that the overall capacitance has come down and in fact, it actually comes down in a stick diagram or in the layout design. Overall performance or that delay is actually less than what we have been calculating using the linear delay model or in the Elmore delay model because in the Elmore and linear delay model up till now we have not been considering the merged diffusion capacitance coming from the pull up circuit side.

We have been always using a very linear combination of this particular capacitance associated with this transistor, capacitance associated with this transistor, capacitance associated with this transistor, whenever the transistors were in parcel. We used only the merged diffusion capacitance whenever the transistors were in a series. But in fact, from the stick diagram we can easily see that if we make it very very compact design make use of lot of merged diffusion capacitance the overall capacitance seen in the output node also decreases. Instead of 9C, it is actually 7C and 7C will naturally have a much better performance than that of the 9C capacitance.