Design and Analysis of VLSI Subsystems
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Lecture - 50
Stick Diagram for different gates

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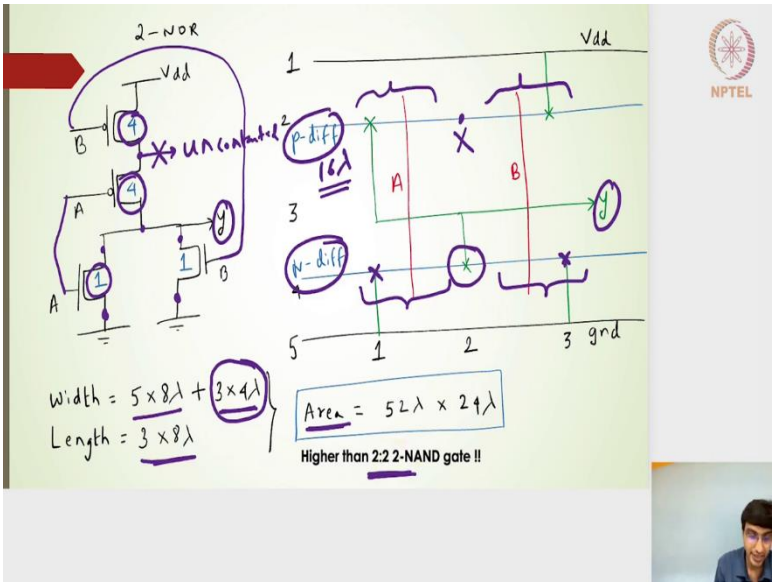

Hello students, welcome to this lecture on the Stick Diagram. In this particular lecture we will have a look into the 2 input NOR gate and then one more additional combinational logic gates and then we will try to represent or draw the stick diagram for this gate. Two input NOR gate again the schematic is given here, let me put pick up a pointer. This is the 2 PMOS transistor in series and then 2 NMOS transistor in parallel. I have given the width of the PMOS and then the NMOS transistor 4:4 and 4 and then 1 and 1 on the NMOS side.

This is what I need to draw in the stick diagram. I now have the polysilicon gate, this A and A are the same and then this B and then this B are the same. What we will do is we will have the P diffusion lines and then the N diffusion lines. We will also have the V_{dd} rail and then the ground rail the polysilicon gate A and B will cut across the P diffusion and N diffusion lines forming the P transistors and then the N transistors for the input A and B respectively on the P diffusion and N diffusion sides.

I will now have this particular line which is A polysilicon line, a polysilicon gate which is cutting across the P diffusion forming the P transistor here and then cutting across the N

diffusion here forming the N transistor here. Similarly B polysilicon gate which is cutting across forms this one and then the transistor on the P diffusion side and on the N diffusion side, that is about the polysilicon gate that is cutting across.

Let us now go over the connections here. What we have is let me have this particular diffusion node as an X node and the other side is nothing, but y. If I consider the B polysilicon gate and its transistor on one side of the diffusion it is connecting to the V_{dd} on the other side it is the X node, which is kind of a common or a merged diffusion with that of the A transistor.

If I have A polysilicon and then B polysilicon this particular node which is an uncontacted. This is an uncontacted because there is no metal line this is an uncontacted merge diffusion. This X is an uncontacted merge diffusion. On the other side of the B transistor it is connecting to the V_{dd}, on the other side of the A transistor it is connecting to the output node y. Here remember that in the stick diagram this overlapping lines of the metal lines which is overlapping with that of the polysilicon line will be on a different layer.

The stick diagram if I have the same colour if I have the same let us say the metal line it should not overlap. If I have the metal line which is kind of overlapping that means that those two metal lines are wired together, that means there is a short circuit. If they are different coloured or in the sense they are of the different nature such as the P diffusion lines which is overlapping with that of the polysilicon gate.

Because the P diffusion lines will be on one layer and then the polysilicon will be on another layer and then the metal line will be on another layer. There will not be any kind of an intersection between the metal lines and then the other natured lines, but if you see the metal lines kind of overlapping or merging or intersecting then there is a problem. In a stick diagram we have to ensure that there are no two lines of the same nature which are cutting across alright. Hope that is clear, moving forward.

This is my X point and then Y point on the pull down side we have the two transistors which are in parallel, the A transistor on one side it is connected to the ground and then the B transistor on one side it is connected to the ground, this is the ground 1, this particular diffusion side is this particular one. This is the X here connecting to the ground and on the B side also this particular point is my line here which is cutting and connecting to the ground.

On this particular diffusion and then this particular diffusions are the same on the pull down side which is gets connected to the y. It is basically a merged contacted diffusion. This is the point merged contacted diffusions. Now to track the number of what is the footprint or the area we will have to track or count the number of the horizontal metal tracks or the vertical metal tracks.

Counting the horizontal tracks is this 1 and then the diffusion is the 2nd the 3rd is this particular metal track Y output node and then 4th one is this particular N diffusion line and then the 5th one is this ground rail. I have 5 metal tracks horizontal, metal tracks on the vertical side we will have this one particular metal line and then this particular metal line can be on the same alignment. I will indicate it by a 1st vertical track, the 2nd one is being this and then the 3rd one is being this.

I will have 3 vertical tracks and then forming the length of the footprint and then the width of the footprint is nothing but,

$$\text{Width} = 5\text{x}8\lambda + 3\text{x}4\lambda$$

$$\text{Length} = 3\text{x}8\lambda$$

Just to ensure that this is the 4 scaling on the 2 input NOR gate and this is only 1 scaling. This 1 scaling will be accommodated in this particular 8λ. That means, that the N diffusion does not have to change the width of the N diffusion does not have to change it is still the 4λ because the scaling is 1. The width of the P diffusion is not 4λ anymore it is actually 16λ + 4λ for the spacing. What we have done is we have taken 4λ on the width side 4λ and then the spacing of 4λ and the 12λ is getting added here. Multiplied by 3 x 8λ on the length side will give me the overall area,

$$\text{Area} = 52\lambda \text{ x } 24\lambda$$

Where λ is nothing but 25 nm for a 65 nm technology, this particular area turns out to be higher than 2:2, 2 input NAND gate.

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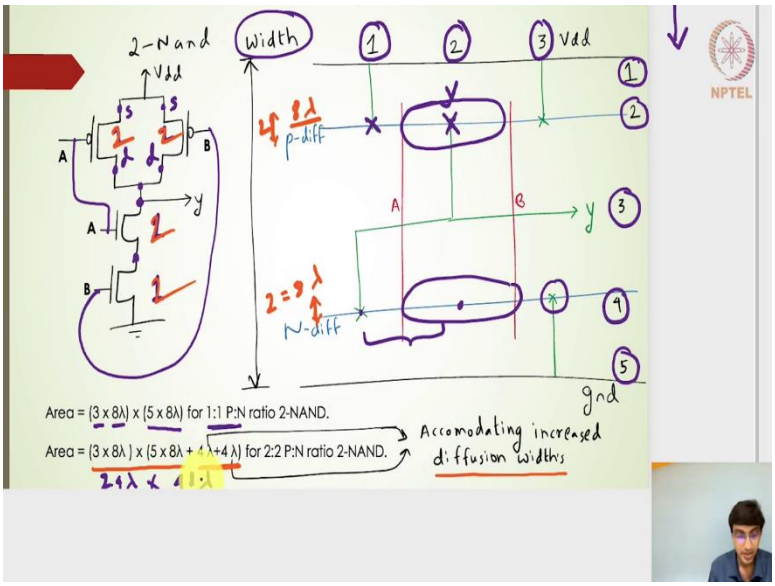

If I go back to the 2 input NAND gate this is what we had. We had this is 24λ x 48λ and here we have a 52λ x 24λ. 48λ x 24λ in the NAND gate and then for the NOR gate it is for 52λ x 24λ, naturally this area is higher the footprint.

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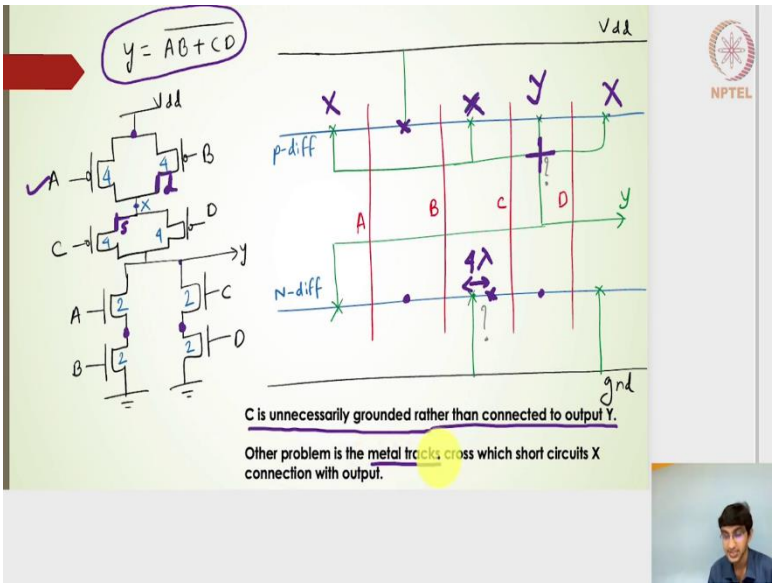

Moving ahead. Let us take a look at this particular combinatorial circuit $Y = \overline{AB + CD}$ and this is the schematic for the $\overline{AB + CD}$. AB in series on the pull down side and then in parallel with that of CD transistor in series then that is connected to the output node Y because it is a conduction complement topology, we will have A and B in series will

become parallel on the pull up side and then CD in series will become parallel on the pull up side.

I have represented a diffusion intend node of X node and on the other side it is the Y node. On the stick diagram side I have the V_{dd} rail and then the ground rail and then we have the P diffusion lines and then we have an N diffusion lines. Let us start with the transistor A on the P diffusion side on the PMOS transistor A on one side it is connected to the V_{dd} on the other side it is actually connected to the X node.

On one side it is connected to the V_{dd} on the other side it is connected to the X node, B transistor on the PMOS side it is connected to the V_{dd}. So, a common contacted merge diffusion is connecting to the V_{dd} and then the other side it is connected to the X node, this is the X node again. C transistor PMOS side one side it is the X node, so C transistor on one side it is the X node, it is kind of getting merged with that of the B transistor this line and then the C transistors this particular diffusion.

In fact, I can say that the source of the C and then the drain of the B is kind of getting merged together. This is the C the C polysilicon gate on the one side it gets merged with that of the B transistors diffusion and on the other side of the C transistor I have a Y node. This we are going to say that this is the Y node and then we will complete the D PMOS transistor. The D PMOS transistor on one side it is connecting to the X node on the other side it is the Y which is the merged one and that is the Y node.

But here the problem is I have this metal line which is going across and connecting all the X nodes and the Y metal line is also coming across it. There is this kind of a cross section which is not expected, what it really happens is we will have the short circuit between the Y metal wire and then the X metal wire and what it also indicates is that D transistor on the footprint, the D transistor both this diffusions are connected which is not indeed the case.

Because, the D transistor on the schematic the X node is not connected to the Y node. The Y node is isolated from the X node of course, it is connected via the transistor, but what we are saying is actually we are connecting this X node and Y node with a metal wire that is been indicated in the footprint or that is been indicated in the stick diagram which is incorrect.

On the pull down side we have the A transistor and then the B transistor. A transistor A polysilicon, gate B polysilicon gate the merged diffusion is this one side it is connected to the ground. This is the B transistors the other diffusion is connected to the ground, the A transistor is connected to the Y node. The A transistor gets connected to the Y node and thereby the A transistor is getting connected to the diffusion of the A transistor is getting connected to the Y node.

The C transistor on one side it is connected to the Y node the other side it is the merged uncontacted diffusion. On this particular seats A polysilicon line on one side it should get connected to the D transistor diffusion. That is what it is doing the A polysilicon and C polysilicon, but on the other side it is kind of forced to get connected to the B transistors diffusion which is connecting to the ground.

What we need is some kind of a separation between this diffusion. That this particular node gets the C node is getting connected to the Y node. In the D transistor I have this particular polysilicon gate on one side it is having a merged diffusion with that of the C transistor and on the other side it is connected to the ground. We need some kind of a separation here. What it this separation indicates is any kind of a diffusion to diffusion, the separation always has to be minimum of 4λ. There are two things here which we notice here is one is the metal wire getting intersected which is a very wrong design and the other thing is we need a 4λ of separation.

If we do not have the 4λ of separation, then the C is unnecessary grounded rather than connected to the output node Y, the other problem we saw was the metal tracks intersecting or crossing each other which ensures that which makes the short circuit connection.

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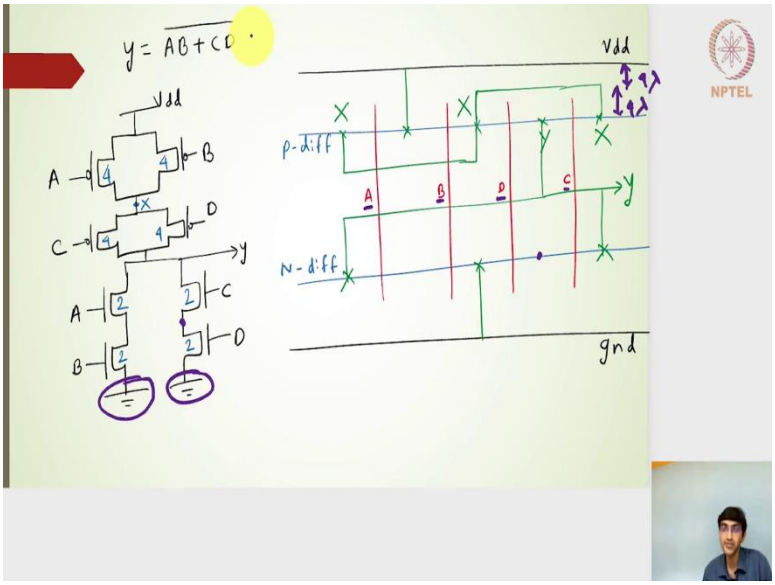

What do we do? one way is to ensure that the metal tracks are in a different layer in the sense are designed differently. So, instead of taking it from here which will intersect the Y metal line instead of that you take it on to the other side. Of course, my area will increase because this metal spacing will have a 4λ spacing and then we will have additional 4λ spacing, but we cannot do anything else.

But even if I do this on the pull down side if I have a C gate and then a D gate here this one the C will be forced to ground which we should not have and that is why I have changed now, I have changed the order of the polysilicon. The A, B and instead of C I have a D and a C now. If I do that I will have A, B, D and C, instead of A, B, C and D, I will have A, B, D and C. The X node will still remain the same position, but instead of the C transistor I am considering the D transistor first and then going towards the C transistor.

For A and B transistor it is very much similar for the D polysilicon I have one side it is X node the other side it is Y. It is also very similar X and Y and then C will have X and Y. Y is the merged contacted diffusion and X it will get connected to the other X nodes. On the pull down side where we had this problem of the C transistor which was forced to connect to the ground that will not be there.

Now, A and B transistor remains the same, the D transistor one side it is connected to the ground because this ground and then this ground are the same. I will have a merged contacted diffusion which is getting connected to the ground. On the other side of the D is

this particular point which is an un contacted merged diffusion and the other side of the C gets connected to the Y output node.

This is what we have for the $\overline{AB + CD}$, in this particular recording what we learnt was we started with the 2 input NOR gates and then the sizing of the of the PMOS transistors and of course, NMOS transistors was incorporated into our stick diagram to find out the footprint. The area of the 2 input NOR gate was naturally higher than that of the area of the 2 input NAND gate. We started analyzing the stick diagram for a another combinational circuit which is $\overline{AB + CD}$ and in $\overline{AB + CD}$ we notice that the ordering of the polysilicon gate is also essential.

Because if I have an order of A, B, C, D on the pulled down side the C polysilicon gate was forced to the ground, if I need to overcome that then I need to have a separation of 4λ, but separation of 4λ is likely to increase the spacing. Instead of that if I can actually reorder the polysilicon gate order.

In the sense instead of A, B, C, D if I have it aligned as A, B, D and C, then I could have a merged diffusion, I can make use of the merged contacted diffusions and then can reduce the size and make the design very very compact. The order of the polysilicon gates is also very very essential in designing the stick diagram and to make the overall footprint very very compact.