Design and Analysis of VLSI Subsystems
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Lecture - 46
Other Logic Family

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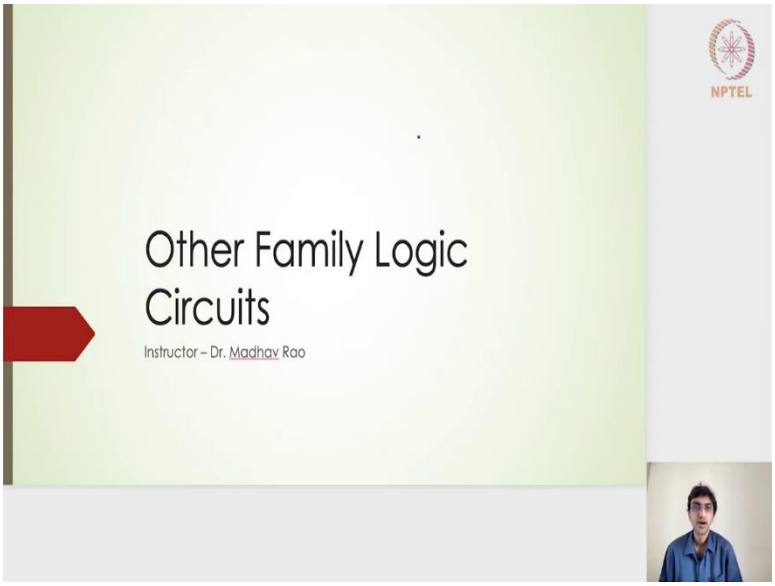

Hello students welcome to this lecture on different kinds of the Logic Circuits. Up till now what we have seen is a regular CMOS family or the regular CMOS designs and then we had seen the pseudo NMOS CMOS logic. In this particular lecture, we will look into two different logic families, one is the ganged the CMOS logic family and another one is the dynamic logic families.

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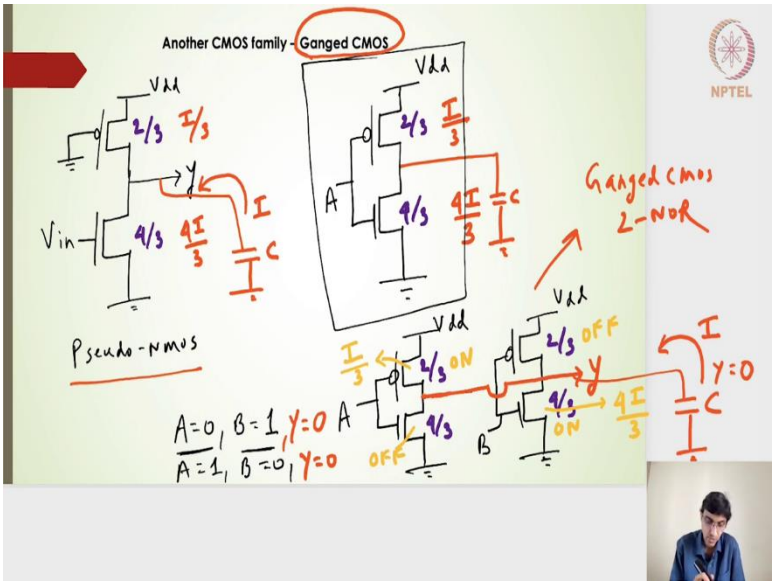

Let us begin this lecture, just with an understanding of the pseudo NMOS circuit and then I think we will dive into the ganged CMOS logic family. Let me quickly draw the pseudo NMOS inverter.

The pseudo NMOS inverter as we know that the PMOS should always be on, that has to be there. It is always connected to the ground and the NMOS is connected to the input, the gate of the NMOS transistor will be connected to the V_{in} and then based on this particular V_{in} value we will get the output.

I will also draw the real V_{dd} and then of course, this is the ground and then this is my output. This is how the pseudo NMOS inverter schematic looks like and what we need is to get a current while it is actually the output is going down, to get a current of I we are having a size of $\frac{2}{3}$ and then $\frac{4}{3}$.

The reason for doing this is, because $\frac{2}{3}$ because this PMOS is always on. This $\frac{2}{3}$ width is going to give me a current of $\frac{I}{3}$ here and that will always be a current of $\frac{I}{3}$ here, even when the input is 1 here, that I will get the NMOS to be on and the output is going to be continue to discharge with a current of $\frac{4I}{3}$.

The NMOS has a current of $\frac{4I}{3}$ and the capacitor will be discharging with a current of I. The $\frac{4I}{3} - \frac{I}{3}4I$ will give me a current of I from the capacitor side. Let me draw the capacitor also, that it becomes easier for 1C.

We need a size of $\frac{2}{3}$ and $\frac{4}{3}$ so that the capacitor discharges with the current of I and then this $\frac{I}{3}$ is the PMOS current which will be driving the capacitor to charge and $\frac{4I}{3}$ is the NMOS current and thereby the capacitor has $\frac{4I}{3} - \frac{I}{3} = I$. This is one kind of the logic family.

Now let us use the same size and draw the regular inverter. If I use the same size and draw the regular inverter, note that the regular inverter, the input is connected to both PMOS and NMOS. I will use this and this is my input now. I am going to write this input as A input and the size of this particular regular inverter is same as that of the pseudo NMOS 1 which I have drawn $\frac{4}{3}$.

Now because the PMOS is not continuously on, it depends on whether A = 0, if A = 1 the PMOS will be off and NMOS will be on and when A = 1 the NMOS will be on and PMOS will be off or A = 0 PMOS will be on and NMOS will be off.

My driving current here will be $\frac{I}{3}$ on the pull up side and then it will be in fact $\frac{4I}{3}$ on the pull down side. The reason is simple, even if I have a capacitor here connected or whatever the parasitic capacitance, this capacitance will have to be driven by this $\frac{4I}{3}$ current, because the PMOS will be off when A = 1 the NMOS will be on and then PMOS will be off.

There is actually no channel for the capacitor to get charged continuously. This is off and thereby this NMOS will be on and then capacitor will get discharged to 4I by 3. Now, with this particular understanding of $\frac{2I}{3}$ and $\frac{4I}{3}$. Let me draw one more circuit, basically the circuit will be nothing but two sets of inverters.

Let me draw it here, although in a small way. I have one inverter and this is my one input and I am connecting one more inverter of course, this is the V_{dd} rail, the same rail goes there and of course, this is the ground rail the same ground rail and I will have one more input this input is called as B input. There are two inverters and now I am going to connect the outputs of these two inverters.

So, I am going to connect the output of these two inverters together and call this as the final output. Now I am going to size this up similar to the pseudo, NMOS similar to

whatever the inverter I have drawn here that is $\frac{2}{3}$, $\frac{2}{3}$ on the PMOS side and then $\frac{4}{3}$ on the NMOS side.

The sizes are actually derived from the pseudo NMOS inverter and let us say that and I am going to pick one such combination when let us say A = 0 and B = 1.

There are two inputs to this particular circuit, whatever that circuit is it is no longer an inverter because there are two inputs. It should be a NAND gate or a AND gate or a OR gate or a NOR gate or whatever XOR gates and so on. If I pick A = 0, and B = 1 as one such combination. A = 0, that means A = 0 says that this one is on, this particular PMOS is on, this particular NMOS is off. I am actually writing it out and B = 1 represents that this NMOS is on and this PMOS is off.

Now I have two of the transistors out of 4 transistors which are on and in a way that it says that the PMOS transistor is on, on this A side and on the B side the NMOS transistor is on. The outputs are connected here by this kind of a red wire here. What it means is I will have a current of $\frac{I}{3}$. I am going to write this the current of $\frac{I}{3}$, the PMOS of $\frac{2}{3}$ width is going to give me a current of $\frac{I}{3}$ and here B = 1 will give me a current of $\frac{4}{3}$, because the width is $\frac{4}{3}$. This one will give me a current of $\frac{4I}{3}$. When A = 0 and B = 1, I have now both the pull up and as well as the pull down circuit to be on with the currents of $\frac{I}{3}$ and $\frac{4I}{3}$. Thereby the capacitors which are now connected at the output whatever the capacitors will be it will basically be the parasitic capacitors of all these 4 transistors, will be seen at the output node.

This particular capacitor will be discharging at a current of I. Hope you know this is clear to everyone. I have a now a current of I that will be discharging, this ganging up of regular inverters, ganging off of this particular inverter and then this particular inverter.

Ganging in the sense, combining these two regular inverters and then forming a particular circuit is called as the gang the CMOS family and then the other version is we are using the size that of the pseudo NMOS because I finally want the current of I from the capacitor side.

What it also implies is $\frac{2}{3}$ and then $\frac{4}{3}$ here, when A = 0 and B = 1 is likely to give me an final output of y = 0. Because the NMOS current drive or the current strength is better than that of the PMOS and thereby I will get finally this capacitor will discharge to 0, here my output will be 0.

Similarly, if I take another combination of A = 1 and B = 0, I will have on the B side I will have the PMOS transistor to be on, and on the a side I will have the NMOS transistor to be on.

The A side NMOS transistor has a better current strength than that of the B side PMOS transistor and thereby my output voltage will eventually be discharged to 0 and I can say that y = 0 here also. If A = 1and B = 1, I will have both the NMOS transistors to be on and both the PMOS transistors to be off and the capacitor will be completely discharged to 0, the output will be 0.

I have now for 3 input combinations I will have output as 0 and finally, when A = 0 and B = 0 both the NMOS transistors will be off and PMOS transistors will be on and thereby the output will be pulled to V_{dd} level on the logic high. Out of the 4 combinations, one combination when A = 0 and B = 0 is giving the output of 1 all the other three combinations give the output of 0 which says that this is a NOR gate.

It is a NOR representation using the ganging up of two regular inverters with the sizes coming from the pseudo inverters. This particular inverter what I have drawn here the two inverters connected or tied together represents the ganged CMOS NOR gate, rather I will say that two input NOR gate, hope this is clear.

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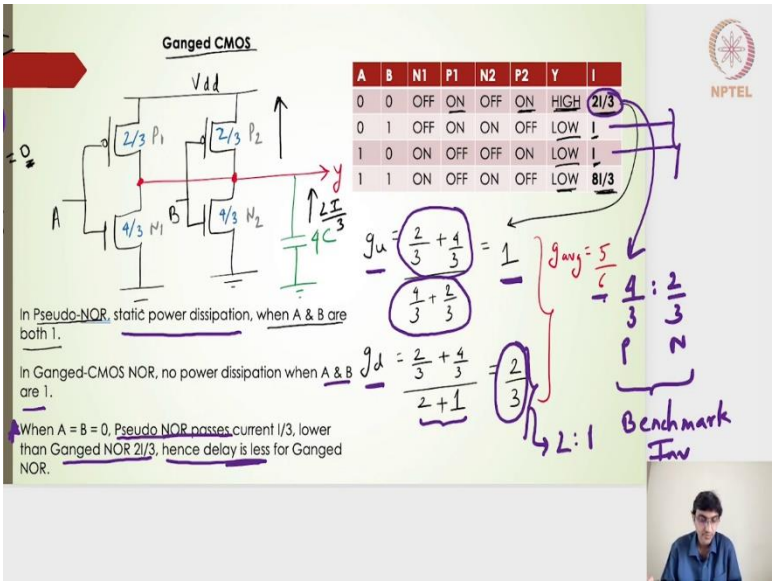

Let me quickly go to the next slide. This is an overview of what I have stated in the previous one. The size is $\frac{2}{3}$ and $\frac{4}{3}$ here, $\frac{2}{3}$ and $\frac{4}{3}$ here and A and B and I have drawn a truth table here, just to summarize all the effect. If A = 0, B = 0 we will have both P1 and P2 to be on. That is what I have written P1 here and P2 here to be on and both the NMOS transistors are off and Y will be the logic high. The output current or whatever the capacitance here or whatever I have written here it will be charging.

The charging current or the rising current to the V_{dd} level will be nothing but $\frac{I}{3}$ coming from the P1 transistors and then $\frac{I}{3}$ coming from the P2 transistor. The capacitor will be charging with a current of $\frac{2I}{3}$. That is what I have written here, let us take an example of 1, the another extreme. When A and B are 1 that means, that the NMOS transistors are on and PMOS transistors are off and thereby the capacitor is going to discharge with a current of $\frac{4I}{3}$ on one branch and a $\frac{4I}{3}$ on the other branch. Total current is $\frac{8I}{3}$, the logic will be anyways be low, here the logic was high.

For the other two cases 0 1 and 1 0 we noticed that one of the PMOS will be on, the other NMOS will be on. Thereby we will get a total capacitor current of I and I, because it will be nothing but $\frac{4I}{3} - \frac{I}{3}$. It will be nothing but a current of I on the capacitor side and the output will be low and that is why it is a 2 input NOR gate.

Now, let us see what is the benefit of the ganged CMOS over the other set of logic families. Let me take the pseudo NMOS here, the pseudo NOR gate and if I want to understand the pseudo NOR gate, let me try to draw that. The pseudo NOR gate again I will have a PMOS which is always continuously on, so it is connected to the ground and it is a NOR gate so I needed two inputs. I am going to draw two of the transistors on the NMOS side with an input of A and the input of B and this is my output. The size will be nothing but $\frac{4}{3}$ here and $\frac{4}{3}$ here and the size here will be $\frac{2}{3}$.

This I am going to call it as the pseudo two input NOR gate, what I am saying is when A and B are 1 here. I will get the current of $\frac{4I}{3}$ and then $\frac{4I}{3}$ here when both are 1 and in this particular ganged CMOS I will get a current of $\frac{4I}{3}$ and $\frac{4I}{3}$, but the point to be noted here is when A and B are 1 in this ganged CMOS the PMOS transistors are off alright.

The PMOS transistor are off, that means that the transient current will be $\frac{4I}{3}$ and $\frac{4I}{3}$, but after y = 0 there will not be any other current, there will not be any DC current or a steady state current that will be flowing to the ground. Once the y reaches the value of 0 it will be the current will be 0 in the ganged CMOS, because both the PMOS transistors are off. Here in the pseudo NMOS NOR gate when A and B are 1, I will get a current here, y is likely to reach to a value of 0, but even after reaching 0 there is a continuous current of $\frac{I}{3}$ which will be charging the capacitor.

There is a current that will be flowing because this PMOS is on and then thereby the capacitor is going to charge. The moment it charges it has a Δq charge it has to be discharged back by this NMOS transistor so that the output stays at 0. What it means is, what it implies is there is always a current that will be flowing from the V_{dd} to the ground always, even after y reaches a steady state output, there will be a nonzero current.

I am going to write it as a non-zero current that will be flowing from V_{dd} to the ground and thereby I will get some static power dissipation always in the pseudo NMOS NOR gates. The gangs CMOS has this particular advantage that there is no static power dissipation similar to that of our regular inverter. Even on our regular inverter there is no static power dissipation because if the NMOS is on then the PMOS side will be off especially for the two input NOR gates, hope you have understood that. The other

advantage in the gang CMOS NOR gate, no power dissipation when A and B are 1, that is what I have explained now.

The other one is this particular point when A = B, A = 0 and B = 0, A = 0, B = 0, I will have both these PMOS transistors to be on, NMOS to be off. Now the pseudo NOR passes, if I consider the pseudo NOR when A and B are 0 the pseudo NOR passes a current of $\frac{I}{3}$. It only passes a current of $\frac{I}{3}$, lower than the ganged NOR which passes a current of $\frac{2I}{3}$. That is what I have explained here. It passes a current of $\frac{2I}{3}$, when I compare that with that of the pseudo NMOS it passes a current of $\frac{I}{3}$ here.

For the rising output when the output wants to go to 0 the gang CMOS structure is likely to have a higher current of $\frac{2I}{3}$ and thereby the delay or the performance will be better. The delay will be less and then the performance will be better. Hence the delay is less that is what I have stated here. Those are the two advantages, one is the static power dissipation, will not be there in the gang CMOS and another advantage is for the rising output it is much faster.

Let us take a look at the logical efforts here, the logical efforts for the inputs, again because it is tied to both PMOS and NMOS side, I will get the capacitance from the PMOS as well as from the NMOS. $\frac{2}{3}+\frac{4}{3}$ will be the total capacitance and then especially for the rising output is sees a current of $\frac{2I}{3}$. That means, my benchmark inverter should be of size $\frac{4}{3}$ and $\frac{2}{3}.\frac{4}{3}$ on the PMOS side and $\frac{2}{3}$ on the NMOS side that I will get a current of $\frac{2I}{3}$ on the PMOS side and $\frac{2I}{3}$ on the NMOS side, this will be the benchmark inverter, I am going to write it as the benchmark.

The logical effort will be nothing but on the input A side or B side is,

$$g_u = \frac{\frac{2}{3}+\frac{4}{3}}{\frac{4}{3}+\frac{2}{3}} = 1$$

It is very very beneficial compared to that of the regular inverter and then the logical effort for the going down 1 we will take the worst case where one of them is on and the other

one is off. What I mean is, when A = 1 or B = 0 or A = 0 and B = 1, I will have a current of I and I here. My benchmark inverter in this particular case will be nothing but because it is giving a current of I will have a 2:1 inverter.

$$g_d = \frac{\frac{2}{3} + \frac{4}{3}}{2+1} = \frac{2}{3}$$

I have now the logical effort for going down is $\frac{2}{3}$ and logical effort for going up is actually 1. My average is nothing but $\frac{5}{6}$ much better than that of the regular CMOS structure to input NOR gates. Hope this is clear.

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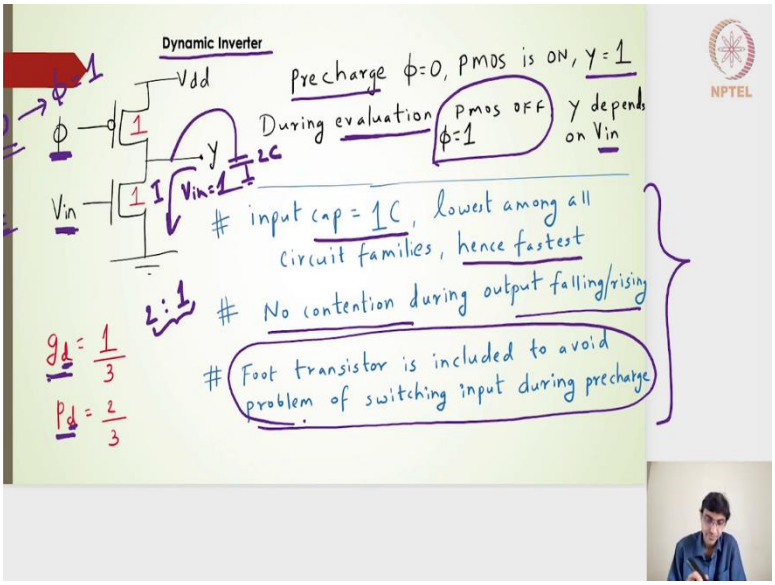

That is one set of logic family, the gang CMOS and it is kindly very very applicable to that of the NOR gates and it is implemented only for the NOR gates circuits. Now, another circuit, another very useful circuit is the dynamic logic and I have drawn here the dynamic inverter. Again, let us talk about this particular inverter circuit how it works. I have a PMOS circuit with a width of 1 and then an NMOS circuit with a width of 1, input is applied only to the NMOS side and then a clock is provided to the PMOS side.

If the structure is very similar to that of the pseudo NMOS family, but the pseudo NMOS family had always the PMOS to be on. That means, that the input or the gate of the PMOS was connected to the ground, here it is connected to the clock signal. What it means is whenever the clock is low the PMOS ensures is on and if the input is 0, the NMOS will be

off and y will be charged or we can say that it will be pre charged to V_{dd}, it will be pre-charged to logic level high.

When $\phi = 1$, that means when the PMOS is off and then whatever is the input whether it is 0 or 1 the y will either stay at 1 if the input is 0 or if the input is 1 then the y will completely get discharged to 0. When $\phi = 0$ actually that is called as the charging mode or it is called as the pre charging mode and then when $\phi = 1$, that means, the PMOS is off that is called as the evaluation phase. When the PMOS is on or when the $\phi = 0$ it is called as a pre-charge mode and then when the PMOS is off that means, the $\phi = 1$.

$\phi = 1$, PMOS being off that is called as the evaluation phase, y actually depends on the input. During the evaluation phase y depends on the input based on the input whether it is 0 or 1, the y will be the complementary logic and during the pre charged phase y will always be 1. The input capacitance is always 1 here because the input is connected to the NMOS transistor and then NMOS transistor width is nothing but 1, the input capacitance is always 1C.

There are some advantages I have written here. Let us try to understand this, before going into this particular understanding let me try to summarize this, there is an pre-charged mode and then there is an evaluation mode. In the pre-charge mode $\phi = 0$ and that is when the output will be connected to the V_{dd} or it will be charged to V_{dd}. In the evaluation phase $\phi = 1$, that means the PMOS will be off and then the based on the input whether it is 0 or 1, the y will be retained to 1 or it will be discharged to 0. There are some hiccups I will come to that in this particular circuit, what should be the logical effort here?

The logical effort in terms of the V_{in} whether it is 0 or 1, if it is 0 it is retained to 1 logic because in the previous phase $\phi = 0$ and then the y is charged to V_{dd} or the logic level high. The moment in the evaluation phase that is when $\phi = 0$ or $\phi = 1$ in the evaluation phase and when it sees input to be 0, the y will stay at 1. Only when the input is 0 y will get discharge to 0 only when $V_{in} = 1$. In this particular case logic, we have to ensure that the input or whatever the evaluation that is the output is being evaluated based on the inputs.

That happens only in the evaluation phase and not in the pre-charge mode and in the evaluation phase we are trying to find out what is the delay alright that means, during our delay evaluation what we need to find out is the logical effort and then the normalized parasitic. My definition of the normalized parasitic as well as the logical effort will not be

applicable for the rising output. The rising output we will anyways have the pre-charge mode which is anyways covered and then when V_{in} = 0 it will stay at 1. The logical effort and then the normalized parasitic is applicable only for when V_{in} = 1 in this case.

My output will actually get drop to 0. My logical effort is always in the dynamic inverter it will always be going down signal and parasitic for the going down signal because for the going up signal the logical effort and parasitic is not at all applicable. Now, for the logical effort for the going down signal, it has a current of I here. My benchmark inverter for the going down signal is nothing but 2:1 inverter.

My logical effort will be nothing but the input capacitance seen in this particular gate side and remember that the PMOS and NMOS are not tied together, the PMOS sees a clock of phi and the NMOS sees the input side it is nothing but the input V_{in}. My logical efforts is a capacitance of the input capacitance of 1 here and that will come in the numerator side divided by the benchmark inverters 2:1. It sees an input capacitance of 3, the logical effort is nothing but,

$$g_d = \frac{1}{3}$$

Similarly, for the parasitic, the benchmark inverter is again 2:1 at the output side here, I will see a total capacitance of 1 and 1.

There is a capacitance of 2C here and the benchmark inverter is going to give a capacitance of 3. The parasitic will be,

$$P_d = \frac{2}{3}$$

Further going down, there is no values defined for the going up signal that means, that there is no values stated for the logical effort for the going up and then the parasitic for going up.

Let me quickly go through this particular 3 statements, the input capacitance is 1C here that is correct and it turns out to be the lowest among all the circuit families and hence the fastest. If I compare the regular inverter, it has a 2:1. The input capacitance is actually 3C,

pseudo NMOS family are inverter if I look into it is $\frac{2}{3}$ and $\frac{4}{3}$ and then if I choose that $\frac{4}{3}$ on the input side it is actually the capacitance is $\frac{4}{3} > 1C$.

In this case it turns out to be the overall input capacitance is low and thereby it becomes the fastest and no contention during the output falling and rising, assuming that the input is not 1 during the pre-charge mode, that is during when $\phi = 0$ I am going to eliminate this and then say that $\phi = 0$ here. That means, that the PMOS is on and if input is not 1, the reason is if input is 1, I will have NMOS and PMOS both to be on and thereby there will be a current here, the V_{dd} will supply the current to the ground.

Assuming that in the pre-charged mode when $\phi = 0V$ input is not equal to 1, we will ensure that the V_{in} states at 0 when it goes through the evaluation phase, that is when $\phi = 1$ that is when the input is applied, I will have no contention during the output falling or rising. The foot transistor is included to avoid the problem of switching the input during the pre-charge mode.

What I said was when $\phi = 0$, I do not want the input to be 1. In that case if input does not stay to be 0 and if it switches to 1, then I can do something to avoid the contention. That is what we will see in this third statement in the next slide, hope this is clear.

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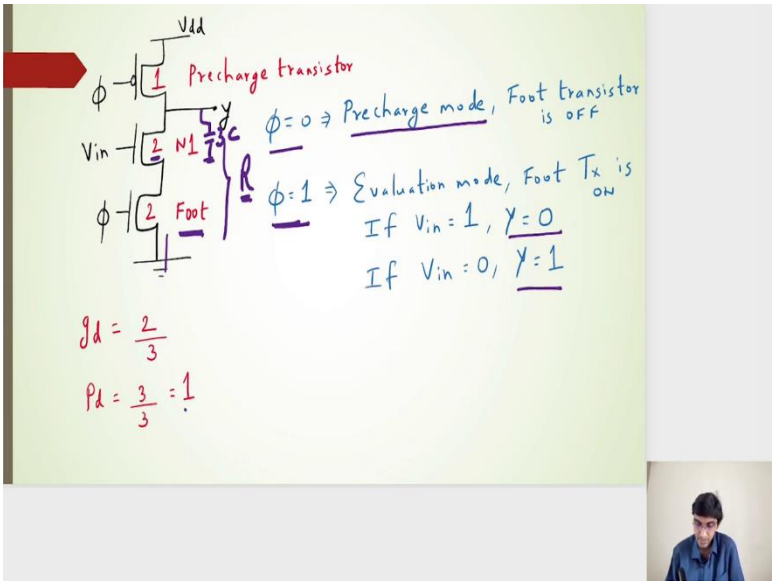

The foot transistor, we have added one more transistor and if I add one more transistor on the pull downside to get a switching resistance of R which is same as that of 2:1 the regular

inverter. I will have to make the width of 2 here and then 2 here. In the previous case the width was 1 and 1 here, but now it has become 2, because there are 2 stack transistors. The input here is ϕ here to the foot transistor, foot transistor which is closer to the ground drain that is called as a foot transistor and these two transistors work similarly the way we had seen previously.

There is an additional foot transistor that is it and then the input of to this particular foot transistor is nothing but the clock which is provided to this PMOS transistor. Again everything remains the same when phi is equal to 0 this is called as a pre-charge mode and now when $\phi = 0$ this foot transistor will be off, this PMOS will be on and then the output will be charged to V_{dd} or logic level high.

When $\phi = 1$ evaluation mode comes in, the foot transistor will be on this will be off. The pre-charge is done in it we are now into the evaluation phase and based on the input it will either stay at V_{dd} or it will be discharged to 0.

If $V_{in} = 0$ there is no complete discharged path to the ground and thereby y will be connected will be retained to logic level high, whenever the $V_{in} = 1$ the y will have a discharge path coming from the N1 transistor as well as the foot transistor and to the ground. That is what I have written y = 0 and y = 1. The logical effort for the going down signal now will be slightly higher because the width is 2 here. The input capacitance seen at the input side will be 2 and my benchmark inverter is anyways 2:1 inverter, I will have a input capacitance of 3.

The logical effort for going down signal is,

$$g_d = \frac{2}{3}$$

The parasitic now will also increase because now I see if the parasitic capacitance at the output node is nothing but,

$$P_d = \frac{3}{3} = 1$$