Design and Analysis of VLSI Subsystems
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Lecture - 45
Psudeo NMOS gates

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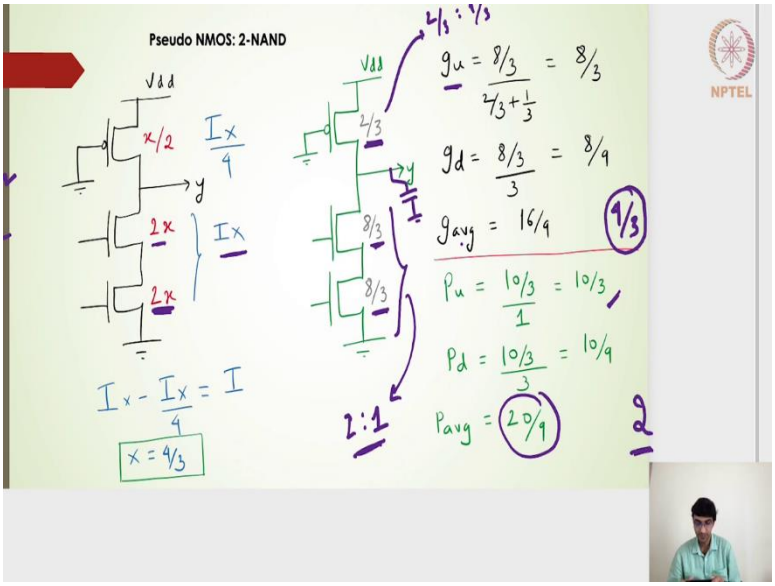

Hello students, welcome to this lecture on the pseudo NMOS family of the circuits. In this particular lecture we will have a look at the 2-input NAND gates and then the 2-input NOR gates and designed using the pseudo NMOS circuit family. In this particular slide I have just shown the 2-input NAND gate.

As I had said the pseudo NMOS circuit with always have an operating or a working PMOS. The gate of the PMOS is always connected to the ground, that forms the pull-up circuit and all the logic is actually done or taken care by this the pull down circuit. For a pseudo NMOS and especially designing the 2-input NAND gate. We need two of the NMOS transistors on the pull down side and then on the pull up side we will have only one transistor, which is always connected to the ground, that means that the PMOS transistor is always on. What we need is to size this transistor up, such that we can design the most primitive 2-input NAND gate using the pseudo NMOS circuit families. In the pseudo NMOS inverter of the circuit we had a size of this was always on and this was connected to the V_{in} and we had the V_{dd} here and then this is the ground. On the PMOS side we had

$\frac{2}{3}$ and on the NMOS side we had $\frac{4}{3}$. What we need is at most primitive 2-input NAND gate and if I see on the pull up side, on the 1 PMOS transistor I am going to follow this same $\frac{2}{3}$ will come on to the PMOS side or rather I know if it is X here, $\frac{4}{3}$ represents X then this will be $\frac{x}{2}$. On the pull down side what we need is if there are two transistors on the pull down side I have to make sure that the sum of the sizes will give me an equivalent transistor of $\frac{4}{3}$ or a value of X.

If I size the two transistors individually as 2x and 2x, then the equivalent transistor will be nothing but of the size X. The reason is, it will give the current of X into I, if I have two transistors 2x and 2x the total current here will be nothing but I into X and $\frac{x}{2}$ will give me a current of $\frac{Ix}{4}$. That is the reason why we have this $\frac{2}{3}$ here which is nothing but $\frac{x}{2}$ and then $\frac{8}{3}$ which is nothing but 2x and then $\frac{8}{3}$, 2x.

It is basically derived from the pseudo NMOS inverter where we had a size of $\frac{2}{2}$, $\frac{2}{3}$ is to $\frac{4}{3}$, that $\frac{4}{3}$ component has been increased to $\frac{8}{3}$ and $\frac{8}{3}$ and if it just resembles to our 2-input NAND gate with a size of 2 and 2 on the pull down side and the inverter size was actually one on the pull down side.

One became 2 and 2 here also the $\frac{4}{3}$, became $\frac{8}{3}$ and $\frac{8}{3}$ in the two transistors and $\frac{2}{3}$ remains the same as instead of the pseudo NMOS inverters pull up PMOS transistor size. If now I have $\frac{2}{3}$ and $\frac{8}{3}$ and $\frac{8}{3}$, I know the benchmark inverter for this falling down output will be 2:1 because this gives me a current of $\frac{4}{3}$ I and then this charging current of $\frac{5}{3}$.

The capacitors output current on the discharging current will be I. My 2:1 benchmark inverter will give me a capacitor output current as I for $\frac{2}{3}$ on the pull upside. The benchmark inverter here will be nothing but $\frac{2}{3}:\frac{1}{3}$ as a inverter because this current when the V_{in} or both the transistors will be off then only we will have the rising output. The rising output current will always be $\frac{I}{3}$. $\frac{2}{3}:\frac{1}{3}$ benchmark inverter will give me the rising current of $\frac{I}{3}$.

In that sense what should be the logical effort, now the logical effort will be nothing but the input capacitance,

$$g_u = \frac{8/3}{\frac{2}{3}+\frac{1}{3}} = \frac{8}{3}$$

For the going down signal the logical effort will be nothing but,

$$g_d = \frac{8/3}{2+1} = \frac{8}{9}$$

$$g_{avg} = \frac{16}{9}$$

If I want to compare with that of the regular CMOS 2-input NAND gate, the g average or the g value was nothing but $\frac{4}{3}$.

The normalized parasitic for going up will be nothing but whatever is the capacitance seen in this particular output node, which will be nothing but,

$$P_u = \frac{\frac{8}{3}+\frac{2}{3}}{\frac{2}{3}+\frac{1}{3}} = \frac{10}{3}$$

Parasitic for going down output signal will be nothing but again,

$$P_d = \frac{\frac{8}{3}+\frac{2}{3}}{2+1} = \frac{10/3}{3} = \frac{10}{9}$$

$$P_{avg} = \frac{20}{9}$$

The P average turns out to be $\frac{20}{9} > 2$. 2 is for the regular CMOS structure 2-input NAND gates had a parasitic of 2 and a logical effort of $\frac{4}{3}$. Here both the logical effort as well as the parasitic in terms of the average turns out to be greater than that of the 2 and $\frac{4}{3}$.

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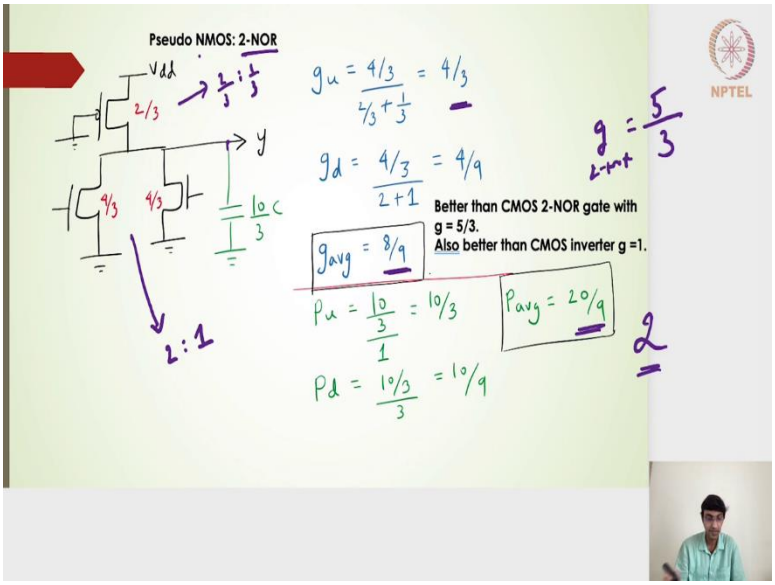

Moving ahead let us see the 2-input NOR gate structure, the two input NOR gate again in a pseudo NMOS circuit family we will have the pull up side with or represented by the PMOS, which is always on. I will have a PMOS here which is always on, that means that the gate is connected to the ground and then the size of that will be $\frac{2}{3}$. Because it is a NOR gate on the pull down side I will have lot of parallel transistors and each of the inputs will be connected to the individual parallel transistors.

It is a 2-input NOR gate, I will have two of the transistors and the size of this will be nothing but similar to that the size of the inverters pull down circuit, which turns out to be $\frac{4}{3}$. I have taken the size of $\frac{4}{3}$ and $\frac{4}{3}$. Under worst case condition I will have one of the branches to be on to be operating. I will get the current of driving from the NMOS will be $\frac{4I}{3}$ current driving from the PMOS will be $\frac{I}{3}$.

The output capacitor discharging current will be nothing but i. In this case to find out the logical effort the benchmark inverter for the pull up side will be nothing but $\frac{2}{3}:\frac{1}{3}$ and for the pull down circuit it will be nothing but 2:1 inverter. In that case the logical effort for going up signal will be nothing but the input capacitance here will be,

$$g_u = \frac{4/3}{\frac{2}{3}+\frac{1}{3}} = \frac{4}{3}$$

Logical effort for going down signal is nothing but again,

$$g_d = \frac{4/3}{2+1} = \frac{4}{9}$$

$$g_{avg} = \frac{8}{9}$$

The average logical effort will be nothing but $\frac{8}{9}$, which turns out to be much much better than that of the $\frac{5}{3}$ which we have seen in a regular CMOS structure, for 2-input NOR gate and in terms of the logical effort this is actually better than that of the inverters.

The normalized parasitic if I find out what is the parasitic seen at this output node which is nothing but,

$$P_u = \frac{\frac{4}{3}+\frac{4}{3}+\frac{2}{3}}{\frac{2}{3}+\frac{1}{3}} = \frac{10/3}{1} = 10/3$$

For the going down parasitic will be,

$$P_d = \frac{10/3}{3} = \frac{10}{9}$$

$$P_{avg} = \frac{20}{9}$$

The average turns out to be $\frac{20}{9} > 2$, which we had seen for the regular CMOS structured two 2-input NOR gate, but the logical effort here is the normal 2-input NOR gate is a the logical effort of $\frac{5}{3}$ using the regular CMOS structure here it is actually $\frac{8}{9}$ and that is a worst difference here.

That is one of the major advantages of using the pseudo NMOS family structure especially for the NOR gates and the NOR gates are usually are implemented in the memory design and where you will see that the pseudo NMOS is there and the reason is because the logical effort is very much lower than that of the $\frac{5}{3}$.

It gives a better performance and in terms of the memory design you will see mostly the NOR gate implementation and there we will it is been observed that we will have the pseudo NMOS structure 2-input NOR gate or whatever k input NOR gates.

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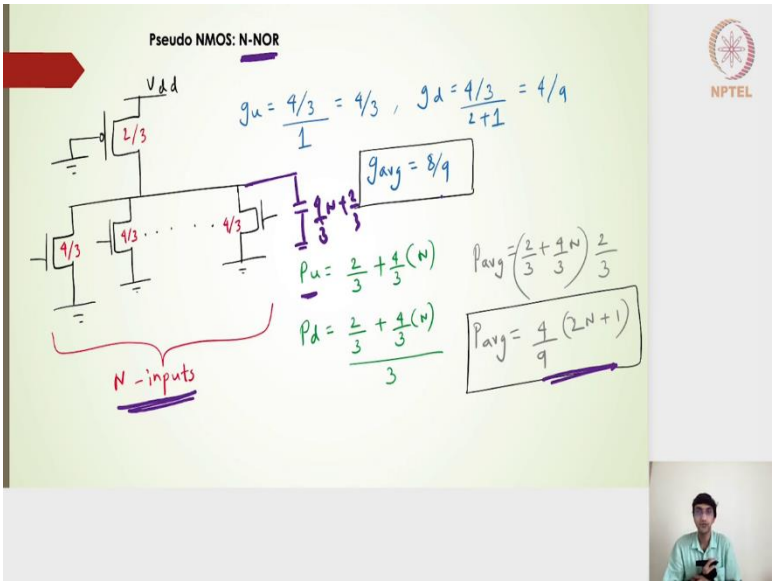

Going ahead, what should be the logical effort for an N input NOR gate, it will be the same $\frac{2}{3}$ on the PMOS side and then $\frac{4}{3}$ on all the parallel transistors which are on located on the pull down side.

For an N inputs the parasitic here seen in the output node will be nothing but $\frac{4}{3}N + \frac{2}{3}$. Here the logical effort remains the same $\frac{4}{3}$ for the going up and then for going down $\frac{4}{9}$ and the average is $\frac{8}{9}$, which is much much lower than that of $\frac{5}{3}$.

The parasitic for going up will now change because of this N input,

$$P_u = \frac{2}{3} + \frac{4}{3}(N)$$

Normalized parasitic for going down signal turns out to be nothing but,

$$P_d = \frac{\frac{2}{3} + \frac{4}{3}(N)}{3}$$

The average parasitic is nothing but,

$$P_{avg} = \left(\frac{2}{3} + \frac{4}{3}N\right) 2/3 \; = \; 4/9\,(2N + 1)$$

For an N input NOR gate the parasitic is a function of the N whereas, the logical effort is independent of the number of the inputs it turns out to be $\frac{8}{9}$, which is very very lower than that of the $\frac{5}{3}$ value.

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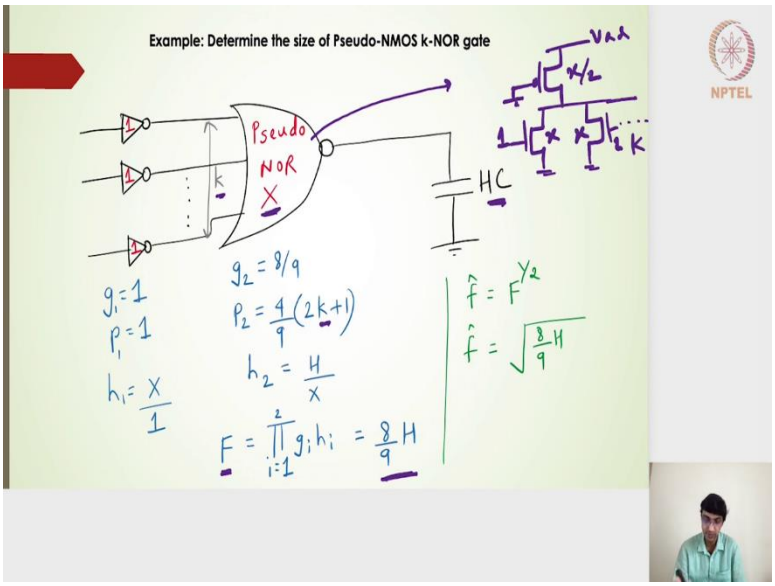

Let us take an example of designing this circuit using the pseudo NMOS NOR gates. Let us say that the size of the pseudo NMOS NOR gate is X we have k inputs. In the previous slide we had seen an expression of the parasitic which varies with respect to the number of inputs N here it is nothing but k inputs.

We will replace that n term with that of the k variable and each of these inputs is coming from an inverter which the gate size of 1, that means that the input capacitance to this particular regular inverter is 1. Remember that this inverter are the normal inverters and not the pseudo NMOS inverters.

The logical effort of this particular inverter is

$$g_1 = 1$$

The logical effort of this particular NOR gate is

$$g_2 = \frac{8}{9}$$

That is what we had seen previously the pseudo NMOS NOR gates.

The parasitic for inverter is,

$$P_1 = 1$$

For the pseudo NMOS NOR gate is nothing but,

$$P_2 = \frac{4}{9}(2K + 1)$$

I have replaced the term k here it is of in place of the n variable. This one says the load capacitance of HC. The electrical effort for this particular second stage pseudo NMOS NOR gate will be nothing but,

$$h_2 = \frac{H}{X}$$

Then the electrical effort for the first stage will be nothing but,

$$h_1 = \frac{X}{1}$$

Because there are two stages given to us and if I want to find out the minimum delay, we need to say that this individual stage sees the same effort. I am going to calculate the path effort here, the path effort is nothing but the product of all the individual stage efforts and then if I do the square root of that particular F value the path effort value then I should be able to assign the best stage efforts to the individual stages.

The product of all the stage efforts will be nothing but,

$$F = \prod_{i=1}^{2} g_i h_i = \frac{8}{9}H$$

$$\hat{f} = F^{\frac{1}{2}}$$

$$\hat{f} = \sqrt{\frac{8}{9}H}$$

I should be able to find out what should be the x size in terms of H. Then I should be able to find out what is the delay expression in terms of the H value as well.

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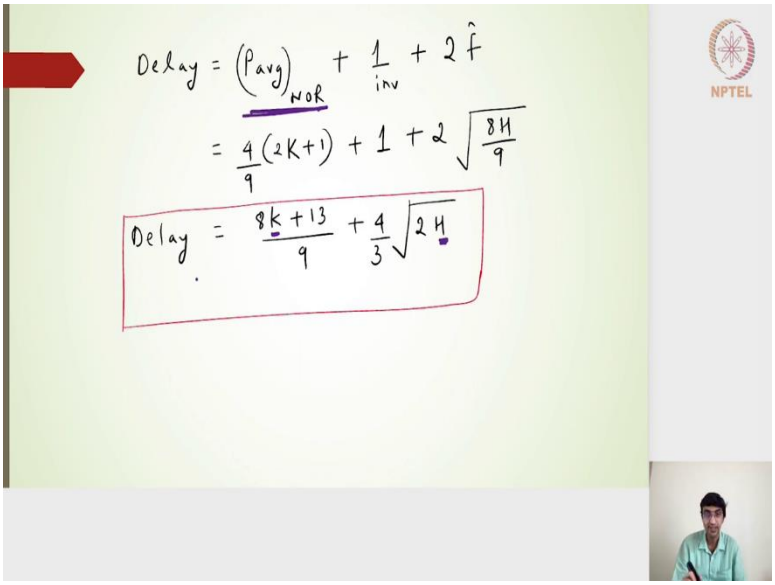

The delay is nothing but the P_{avg} because we have using the pseudo NMOS, where the normalized P value for going up and going down will be different. We take the average value for the pseudo NMOS NOR gate and then the inverter is anyways,

$$\text{Delay} = \left(P_{avg}\right)_{NOR} + 1_{inv} + 2\hat{f}$$

$$= \frac{4}{9}(2K + 1) + 1 + 2\sqrt{\frac{8H}{9}}$$

$$\text{delay} = \frac{8k + 13}{9} + \frac{4}{3}\sqrt{2H}$$

If I know the value of K and if I know the value of H, I should be able to find out what is the delay and this delay will be the normalized delay. If I want to find out the absolute delay it should be multiplied by 3RC and if RC=1ps. We should be able to estimate the delay in terms of the picoseconds. Hope this is clear.

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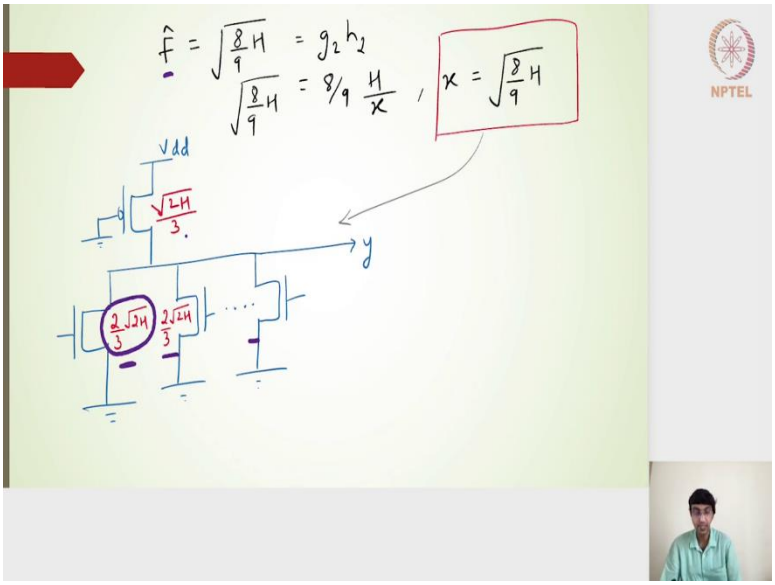

Finally, if I want to find out what should be the size? the individual stage efforts is,

$$\hat{f} = \sqrt{\frac{8H}{9}} = g_2 h_2$$

$$\sqrt{\frac{8H}{9}} = \frac{8}{9}\frac{H}{x}$$

$$x = \sqrt{\frac{8H}{9}}$$

This will be $\frac{\sqrt{2H}}{3}$, this is the x value $\frac{2}{3}\sqrt{2H}$, $\frac{2}{3}\sqrt{2H}$ and then so on. This x value will be this particular value of the size of the NMOS transistor, that is what we wanted to see. I am going to the previous set of slides. This is the x value we want. What the pseudo NMOS NOR gate represents is on the pull down side and then on the pull up side I have k inputs this is the PMOS V_{dd}. This is my x value. If this is my x value because this is the input capacitance seen by the input nodes here.

This is the 1 input this is the 2nd input and then so on, k inputs this is anyways grounded. If I have the value of x here, $\frac{x}{2}$ will be my width on the PMOS side, that is what we had

seen for the primitive word pseudo NMOS 2-input NOR gates. If this size turns out to be x this particular width on the PMOS side will be $\frac{x}{2}$.

Going back to the present slide where we found the $x = \sqrt{\frac{8}{9}}$. That is what I have written here $\sqrt{\frac{8H}{9}}$, which will be nothing but $\frac{2}{3}\sqrt{2H}$.

Individual sizes on the NMOS or the pull down side will be nothing but $\frac{2}{3}\sqrt{2H}$.. The PMOS transistor size will be nothing but which is always on in the pseudo NMOS circuit families will be $\frac{\sqrt{2H}}{3}$. We have identified the sizes of the pseudo NMOS circuit for the 2-input for the k-input NOR gates, that we will get the best delay.