Design and Analysis of VLSI Subsystems
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Lecture - 44
Introduction to Pseudo NMOS

Hello students. Welcome to this lecture on Pseudo NMOS circuits. Pseudo NMOS circuits represents another family of the circuits are again derived from the CMOS family wherein the operation is completely done by the NMOS and the PMOS transistor in the pull up circuit will exist and it will be operational continuously.

Let us have a look at it and we will see some of the disadvantage with respect to this particular family of the circuits.

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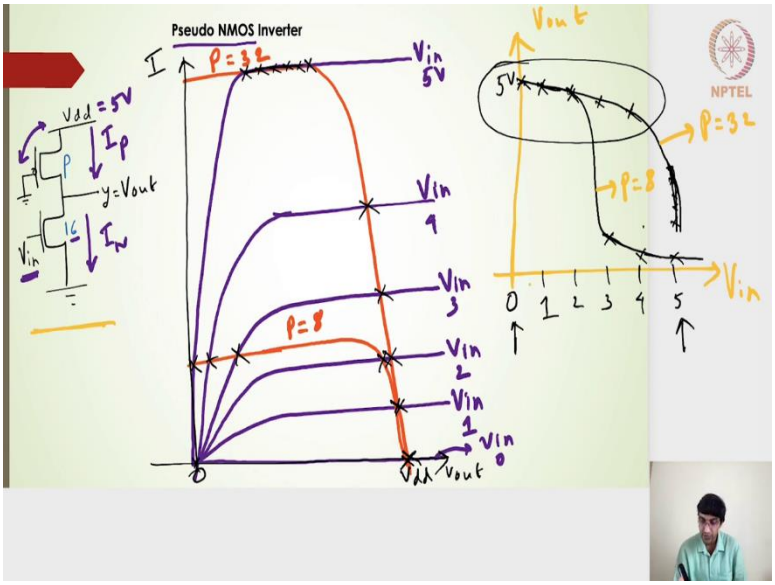

I have an empty almost an empty slide, this is a representation of the pseudo NMOS circuit. This particular part if you look closely, into this particular part this P is the size of the PMOS circuit and 16 is one such size of the NMOS circuit. Although, I know at this particular point of time let us ignore this P variable and the 16 as the width of the NMOS and P as the width of the PMOS circuit. But more importantly I think this is the input or the gate of the PMOS is connected to the ground which implies that the $V_{gs} = -V_{dd}$. That

means, that I will have a constant flow of the current in the PMOS side. I will always have the PMOS circuit operational and on the NMOS side the input is given to the NMOS side.

If the input is 0 the NMOS will not be operating I mean my output will be anyways be pulled to V_{dd}. If the input is high, if the input is similar to V_{dd} of whatever 5 volts or 1 volts whatever we considered the V_{dd} value. If it is same as that then the NMOS will be on and now we will have the NMOS current and I will have continuously a PMOS current.

If we make this NMOS width higher than that of the PMOS width then I will have this NMOS current to be higher than that of the PMOS current. Thereby the output will be dominated by the NMOS, that means that the output will be pulled down. Finally, we should be able to have a logic of 0 if the NMOS width is higher than that of the PMOS width, rather I will say instead of the width I will say that if the NMOS driving strength is better than that of the PMOS driving strength then the output will be pulled down to low logic, whenever the input is high. This forms a primitive circuit of the inverter circuit drawn from the pseudo NMOS family and that is why it is called as a pseudo NMOS inverter.

Let me draw a quickly the IV characteristics of this particular inverter. We had seen earlier the IV characteristics of the PMOS and NMOS circuit in the regular inverter, but this one is a pseudo NMOS where the PMOS is continuously on. Let me draw the IV characteristic. This will be my current and then this will be my output voltage this is nothing but y is nothing but my output and then this is what I am going to draw and let me pick one colour for the PMOS current.

Let me pick a red colour for the PMOS current and if I want to draw the IV characteristics of the PMOS let us say that the PMOS is equal to 32 means this P variable is equal to 32 because I have written the size of 16 here. If I want to match the betas of the PMOS and NMOS it is better to have the PMOS size as 32.

I am going to write this one like this which represents that this is a PMOS current versus the voltage characteristics for a size of 32. Now I am going to draw the NMOS IV characteristics for varying values of the input because the input is connected to the gate of the NMOS that is it and it is not connected to anywhere else it is not connected to the gate of the PMOS it is connected only to the gate of the NMOS. For different values of V_{in} I will have the IV profile. Let me begin with V_{in} and then the NMOS size of 16 here. Let us

say that the $V_{in} = 5V$. If I want to draw the profile of the V_{in} of 5 it will match with that of the PMOS with a width of 32. Because the magnitude level of the saturation current of the NMOS here for 16 size, when the input voltage is 5 volts and when P = 32 here that is a 32 size, my $V_{gs} = -5$ volts, assuming $V_{dd} = 5$ volts. Then I will get the saturation current to be the same, I should be having something like this.

The IV characteristics something like this for a V_{in}. Let me consider this $V_{dd} = 5V$, hope this is clear and for $V_{in,4}$ I will have something going like this. So, $V_{in,4}$ and similarly V_{in} of 3, 2 and 1, I should draw. I am going to draw $V_{in,3}$, $V_{in,2}$ and then $V_{in,1}$ and finally I will have $V_{in,0}$ which will be nothing but this x axis line alright.

$_{5V}$

This is my IV characteristics for the size of 16 and considering the PMOS width has 32. If I want to find out the intersection point, then I should be able to find out to estimate the transfer characteristics. Let us try to identify the intersection points for this particular 2 transistors which are in series, but of course having a different input.

For the PMOS all my intersection points will be on this particular red line the PMOS current line. For a different input starting from this particular line where I will have Vinput of 0 my intersection point will be nothing but here when $V_{in,0}$.

When $V_{in,1}$ my intersection point is here and then when $V_{in,2}$ my intersection point is here, $V_{in,3}$ the intersection point is here, $V_{in,4}$ the intersection point is here and when the $V_{in,5}$ I will have this series of the intersection points. This will be my series of the intersection points because the both the saturation currents will give me a range of the intersection points. If I want to draw the transfer characteristics of this let me pick up another colour, this will be my transfer characteristics V_{out} versus V_{in}.

For all these points $V_{in,0}$, I need to draw something 0 I will say 1, I will say 2, I will say 3, 4 and then finally, 5. $V_{in,0}$ I will get somewhere very close to the 5 volts. Let me find out this one seems to be better I think. This one is my particular point on the Voutput line which will be nothing but 5 volts. When $V_{in,1}$ I will have again a closer point here, when V_{in2} I will have another closer point here. $V_{in,3}$ another closer point, all these points are actually close to the my V_{dd} point here. V_4 is also somewhere here, V_4 is also on the other side closer to the V_{dd}, this will be here and then V_5 actually comes somewhere here.

I will say this particular line of V_{out}will be my transition line. My transfer characteristics here turns out to be something like this. Of course, this will be my transfer characteristics which turns out to be actually bad transfer characteristics.

What to do now? this transfer characteristics turns out to be bad in the sense that most part of the input it is staying close to 5 volts and it does not really behave like an inverter. When I pick 0 it will anyways give 5 volts, but when I pick the logic high here at the input side it will still going to give me somewhere above 2.5, it lies on that particular transition region. Now, what if I pick a value of P = 8? P = 32, P = 16 will be exactly half of this particular current characteristics and P = 8 will give me one fourth of that. I am going to draw P is equal to 8th line which will be nothing but somewhere here P = 8.

This will be my P is equal to 8th line and now I am going to get the intersection points somewhere here 1 of course, close to here 2, 3 of course, I will have three points here and then the remaining three points somewhere here and here. Now, if you look into P =8 I have three intersection points on one side close to the Vdd and the other three intersection points on the other side which is close to the 0, which is close to the 0 in the sense this is my 0 and this is my V_{dd}.

If I look into the P = 32 line the intersection points were almost loaded or dominated or were line close to the V_{dd} line whereas, P = 8. Now, I am getting the points actually closer or rather the three intersection points on one side of the V_{dd} and the other three points exactly away from the V_{dd} and closer to the 0.

Now, if I actually draw the transfer characteristics, I will get actually three points here 1, 2 and 3 will remain the same and starting from $V_{in,3}$ it will be somewhere. This particular point on the V_{out} line will be somewhere here, 4 again it will be here and then 5 will be somewhere here. Now I will get something like this. If I look into this particular profile which is P = 32 and P = 8 and if I want to choose it for an inverter characteristic I will actually choose P = 8 instead of P = 32, hope this is clear.

Once again, I want to just summarize this particular slide what we did was we looked at this particular circuit starting from this particular stage where the PMOS is continuously on and then the NMOS is connected to the V_{in}. The output is actually dependent on the input that is been passed to the NMOS and that is why it is this particular circuit is called

as a pseudo NMOS family of circuit because the output is a pseudo dependent on the NMOS evaluation or the NMOS output. Whether the NMOS is going to pull it down or high, that is the reason why it is called as a pseudo NMOS circuit or also called as a semi NMOS circuit, whereas the PMOS is continuously ON.

For finding out that the solution points what should be the current for a different input voltage applied to the NMOS circuit, we do the IV characteristics for both PMOS and NMOS. For PMOS only this particular variable when P = 32 we do that and then identified the intersection points. The intersection points were not giving me asymmetrical points and it was heavily loaded towards the 5 volts side and then when the P = 8 was plotted, we saw that the intersection points were now not symmetrically. But we got three points which are close to the 5 volts and then the three points or remaining three points, these three points were close to the 0 volts. If I draw that particular transfer characteristics P = 8 is more preferable than that of the P = 32.

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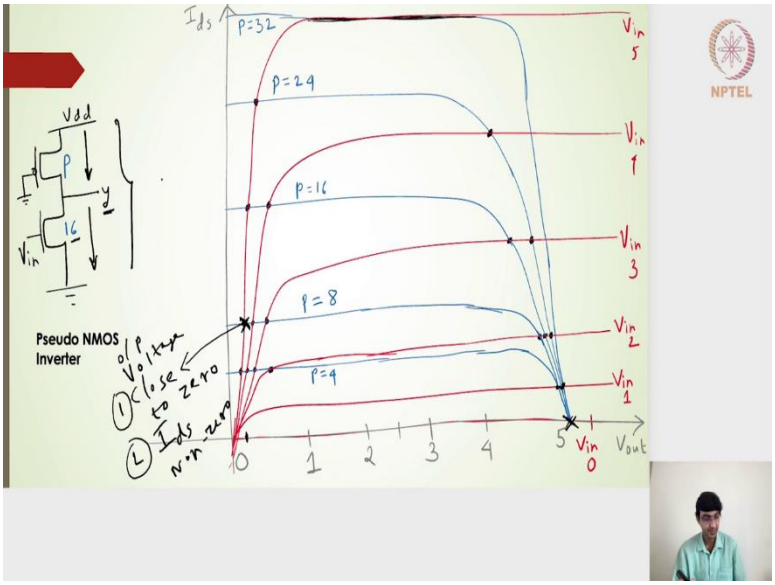

Moving ahead, this is what we have the transfer characteristics which we draw in the previous slide, P = 32 line and then the intersection points and then I have drawn P = 24, P =16, P = 8, P = 4 here and this P = 8.

When it is 16 here the width of the NMOS is 16, P = 8 gives me close to the symmetrically opposite points. If I plot at this intersection points on the transfer characteristics, I have also got P = 4, but the problem with P = 4 is now I have this four points close to 0 and then

one point or rather two points close to 5 volts. What we really need is three points on one side and three points on the other side. P = 8 it turns out to be a better one for drawing the inverter characteristics. The reason I am saying that P = 8 is a better one is the transfer characteristics of the P = 8 turns out to be a close match with that of the unskewed CMOS inverter.

If I have a CMOS wherein the PMOS and NMOS gates are connected and then if I supply the input voltages and then we will get the output voltage. The transfer characteristics of that particular CMOS inverter turns out to be a matching with P = 8 here, when 16 is the NMOS gate size. P = 8 where is the three intersection points are on one side and the three intersection points on the other side, it turns out to be a close match with that of the CMOS inverters transfer characteristics, hope this is clear.

Another point here is if I get into $V_{in,0}$, $V_{in,0}$ the intersection point is on the x axis is on the V_{out} axis what it means is the intersection point is actually here for an input of 0. If I pick P = 8 the intersection point is actually on this x axis or the V_{out}axis what it means is the current is actually 0, when $V_{in} = 0$.

Whereas, if I pick for this P is equal to 8th line and if I supply $V_{in,5}$, this is the line. The intersection point is somewhere here what it means is the current is actually a non zero current it is not a 0 current it is actually a non zero current. This is what the disadvantage of the pseudo NMOS circuit does. Even if the logic is 0 the output logic it is close to 0, although this particular point I will say that it is not 0 it is close to 0. For picking P = 8 and supplying the $V_{in,5}$ I will get this particular point the output voltage is close to 0 that is one observation.

The second observation is I will say that the output voltage close to 0. The second observation is the current here I_{ds} current or whatever that current is, this particular point it is a non zero current. I will have a non zero current that will be flowing from the NMOS side. I will have a non zero current that will be flowing from the NMOS side, which will be going to the ground.

What it means is with respect to the CMOS inverter when the input was 0 volts the current was 0, when the input was 5 volts the current was actually 0. There was no power dissipation when I am actually putting the input of 0 or 5 volts here in a normal inverter.

But whereas, in a pseudo NMOS circuit and then the gate represented by the pseudo NMOS circuit family.

Whenever there is the input is 0 there is no current, but when the input is a logic 1 or in this case 5 volts, I will get a non zero current continuously passing from the V_{dd} to the ground. There is a constant current that will be flowing from V_{dd} to ground when the $V_{in,1}$.

That means, I will get a constant power dissipation from V_{dd} to 0. Even when the logic is at steady state, even when the $V_{in,5}$ or the logic 1 and the output is actually close to 0 volts which will be held at steady state. But the current will still be flowing from V_{dd} to ground, that means I will get a continuous power dissipation, this is the disadvantage of the pseudo NMOS circuit family.

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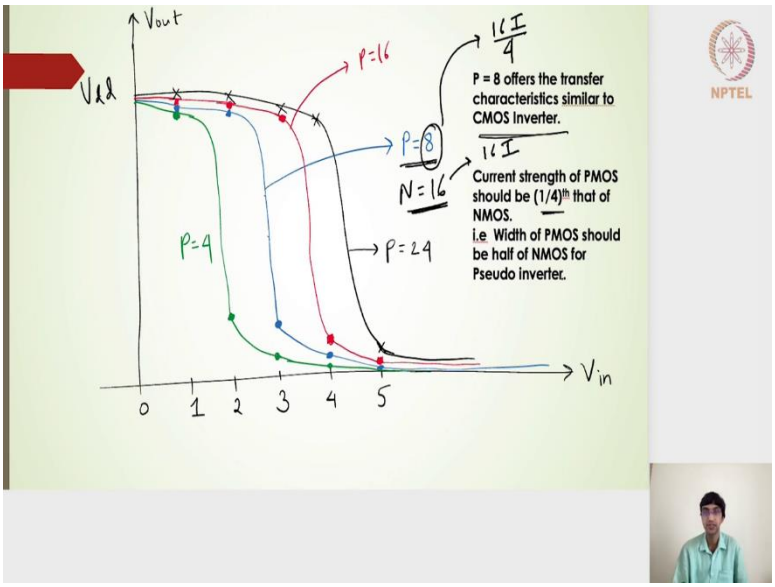

If I draw this particular transfer characteristic, this is what I get the transfer characteristic, I have not drawn the 32. But P = 24 is what this gives me only one intersection point on the other side all other four points are on close to the V_{dd} side. This is the V_{dd} and you can see that the output actually becomes close to 0 and not exactly 0.

P is equal to 8th line, this is our preferable line because I will have 1, 2 and 3 intersection points and then the other three intersection points on the other side. This represents close to our standard inverter circuit P = 4 is on the other side. This could be termed as a low

skew inverter and P = 16 can be termed as a high skew inverter. But P = 16 and P = 4 represents the low skew and then the high skew of the normal inverter.

In a pseudo NMOS there is nothing like the low skew or high skew, but the transfer characteristic implies that way P = 8 offers the transfer characteristic similar to the unskewed CMOS inverter. What we really need is a current strength of the PMOS should be one fourth that of the NMOS. The current strength of the PMOS if it is P = 8 and for that the NMOS we took the width as 16 what it means is I will get a current strength here as, let us say it is 16I.

The current strength of this particular PMOS P = 8 represents, when P = 32, I will get 16I. It is basically $\frac{16I}{4}$. P = 8 gives me a current strength of $\frac{16I}{4}$. P is equal to 16 will give me a current strength of $\frac{16I}{2}$, P = 8 will give me a current strength of $\frac{16I}{2}$x2 $= \frac{16I}{4}$.

The current strength of the PMOS should be one fourth that of the NMOS that is the width of the PMOS should be half that of the NMOS width in this pseudo inverter. That I will get the transfer characteristic similar to that of the unskewed CMOS inverter.

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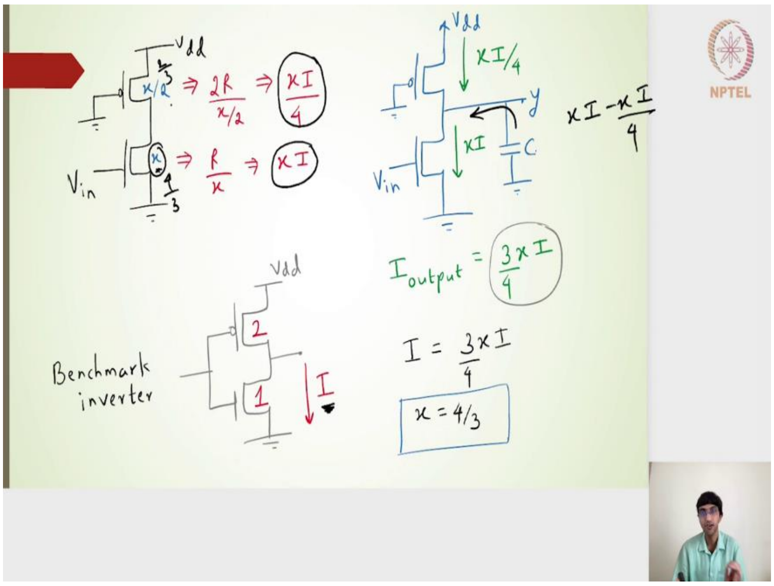

Hope this is clear moving ahead. What I need is, let us say the size of the NMOS is x here. The size of the PMOS in a pseudo NMOS inverter should be $\frac{x}{2}$, that is what we had interpreted from the last slide.

The size is x for the NMOS, the PMOS should be $\frac{x}{2}$. So, that my current strength is xI the current and the driving current is xI here for an x size of NMOS and the current drive for the PMOS will be nothing but $\frac{xI}{4}$. I have denoted the switching resistance here x by 2 will give me a switching resistance of,

$$\frac{2R}{x/2} = \frac{4R}{x} = \frac{xI}{4}$$

Similarly, here it is nothing but,

$$\frac{R}{x} => xI$$

If I actually show this particular current strength $\frac{xI}{4}$ and xI here. The capacitor discharging current turns out to be or the output current in this particular case will be nothing but $\frac{\mathrm{xI}}{4}$ and then this particular current is equal to xI. It will be the capacitor discharging current will be nothing but,

$$\mathrm{I_{output}} = \mathrm{xI} - \frac{\mathrm{xI}}{4}$$

$$\mathrm{I_{output}} = \frac{3}{4}\mathrm{xI}$$

$$\mathrm{I} = \frac{3}{4}\mathrm{xI}$$

This will be my output current which is nothing but a capacitor discharging current. My I value, this is my output discharging current, but now let us say that if this is what I want to match with that of the 2:1 benchmark inverter. 2:1 benchmark inverter when the input is high this PMOS is off and then I will get the complete discharging current on this NMOS transistor. If I want to match this current I, current should be nothing but this particular output current what should be my x. In that case if,

$$\mathrm{I} = \frac{3}{4}\mathrm{xI}$$

$$\mathrm{x} = \frac{4}{3}$$

That means I need a size of $\frac{4}{3}$ here and $\frac{2}{3}$ here. While it is discharging I will get a falling current output of I, this becomes our primitive circuit, primitive in the sense there is no smallest transistors on the NMOS side and the smallest transistors on the PMOS side which will give me a falling current of I.

That becomes the most primitive circuit for the pseudo NMOS inverter circuit. To find out the most primitive circuit I have represented this in the form of an x and I try to equate this the output current with that of the output current of the benchmark inverter and it turned out that I should have a size of $\frac{4}{3}$ on the NMOS side and then a $\frac{2}{3}$ on the PMOS side. So, that I will get the falling current of I, hope this is clear.

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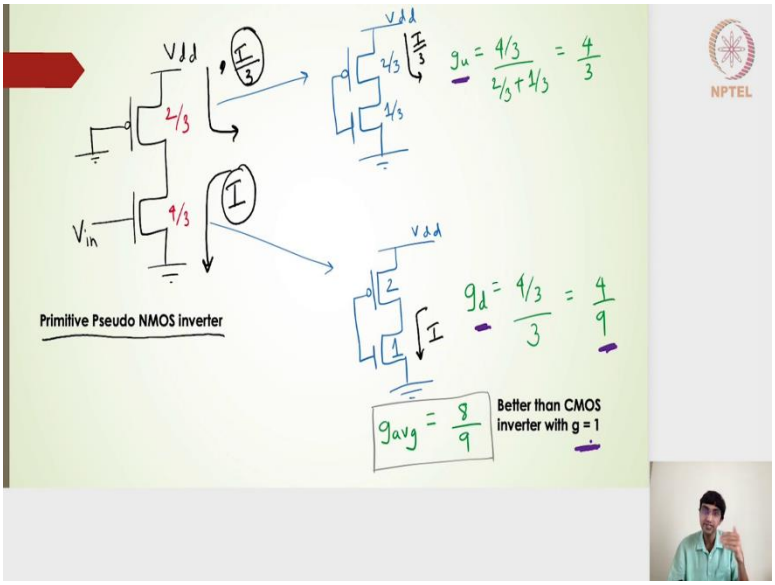

Finally, we have $\frac{2}{3}$ and then $\frac{4}{3}$, this becomes our primitive pseudo NMOS inverter. Now, how do I evaluate the logical efforts and then the parasitic? the logical efforts for the rising output and then the for the falling output will be different benchmark inverters and then the reason is very simple for the falling output current is actually I. The discharging current will be I from the capacitor side for the rising one, the charging current or the rising current turns out to be $\frac{I}{3}$. This forms, this current are different. I current here for the falling output for the rising output the current is $\frac{I}{3}$ because it is the size is $\frac{2}{3}$ and $V_{in} = 0$, that means that completely the discharging is done by this PMOS or the charging is done completely by

this PMOS transistor. If the size is $\frac{2}{3}$ the current will be $\frac{I}{3}$, if the size is $\frac{2}{3}$ the switching resistance = $\frac{2R}{2}x3 = 3R$.

The current will be nothing but $\frac{I}{3}$. If I want a current of $\frac{I}{3}$, my benchmark inverter will now be $\frac{2}{3}$ and $\frac{1}{3}$. Instead of 2:1 it will now be $\frac{2}{3}$ and $\frac{1}{3}$ because 2:1 inverter will give me a current of I. $\frac{2}{3}$ and $\frac{1}{3}$ will give me a current of $\frac{I}{3}$.

Here also I will get the current of $\frac{I}{3}$. For the falling output here $\frac{4}{3}$ and $\frac{2}{3}$ pseudo NMOS the falling current is I. The benchmark inverter will be 2 by 2:1 because the falling current will be nothing but I. Now if I have that the benchmark inverters ready I should be able to find out what is the logical efforts.

The logical effort for the rising output for the going up output g_u will be nothing but the input capacitance, the input capacitance is nothing but,

$$g_u = \frac{4/3}{\frac{2}{3}+\frac{1}{3}} = \frac{4}{3}$$

The logical effort for the going down output signal will be nothing but,

$$g_d = \frac{4/3}{3} = \frac{4}{9}$$

Note that $\frac{4}{9}$ is comparatively very very lower than that of 1 and if I consider the average of g_d and g_u $\frac{4}{3}$ and $\frac{4}{9}$, I will get $\frac{8}{9}$. This in fact is better than the CMOS inverter of g = 1 and that is the advantage of the pseudo NMOS family. Some of the circuits has really has a low parasitic and a low logical effort, it can help in improving the performance of the circuit output.

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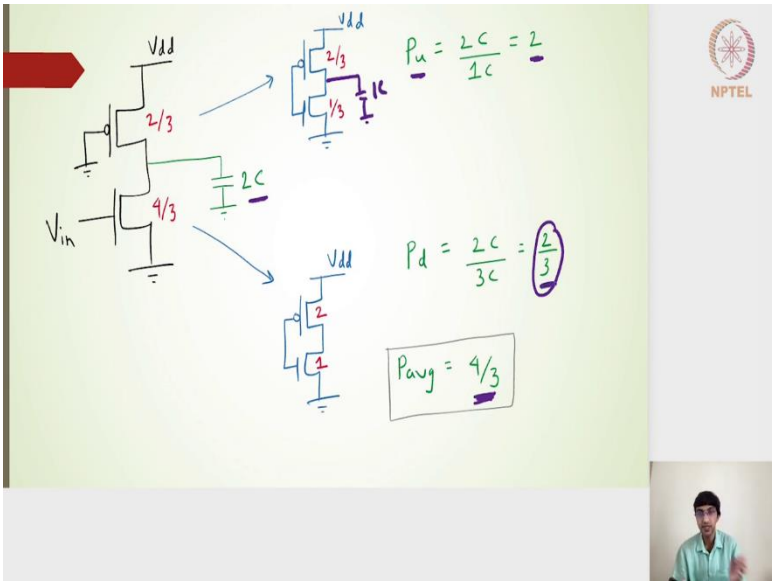

Let us go to the next one. Let us try to find out the parasitic for the going up output and then the going down output. For the going up output we know the benchmark inverter should be $\frac{2}{3}$ and $\frac{1}{3}$ inverter and for going down it should be 2:1.

The parasitic here will be nothing but the parasitic or the capacitance in the output node for the pseudo NMOS inverter, here will be nothing but, $\frac{2}{3}+\frac{4}{3}=\frac{6}{3}=2\text{C}$. The 2C comes here on the numerator side and 1C will be the output node capacitance coming from the benchmark inverter, that will be 1C here.

Finally, the normalized parasitic for going up signal is,

$$\text{P}_\text{u}=\frac{2\text{C}}{1\text{C}}=2$$

For the going down signal it will be nothing but,

$$\text{P}_\text{d}=\frac{2\text{C}}{3\text{C}}=\frac{2}{3}$$

$$\text{P}_\text{avg}=\frac{4}{3}$$

The average is $\frac{4}{3}$ which is actually higher than that of our regular inverter, but the going down parasitic turns out to be less than that of the value of 1, the CMOS regular inverter has a parasitic of 1.