**Design and Analysis of VLSI Subsystems**
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**Lecture - 43**
**Skewed gates and best P/N ratio**

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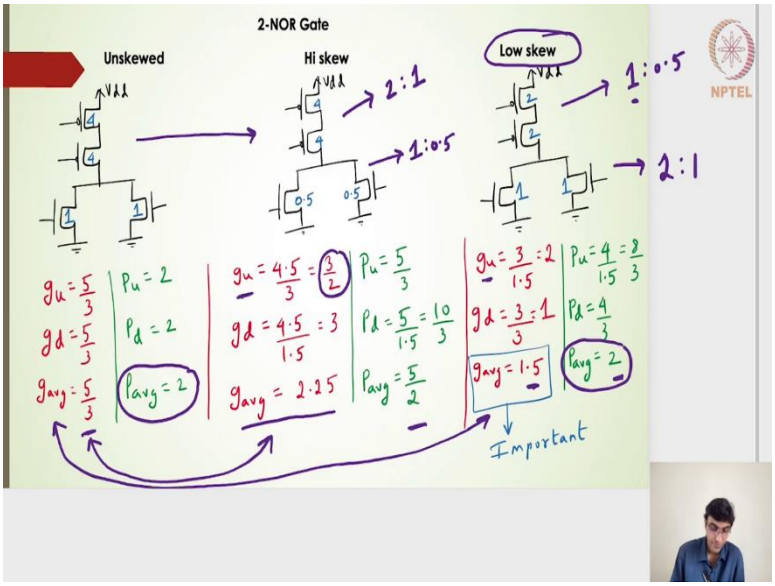


Hello students, welcome to this particular lecture, continuing on to the Skewed gates. This particular example on this particular slide talks about 2-input NOR gate. We have the unskewed gate and then the high skew gate and then low skew gate. We would like to go through how to evaluate the logical efforts and then the normalized parasitic for this different skewed 2-input NOR gates. Unskewed gate it is quite common $\frac{5}{3}$. Then the normalized parasitic is anyways 2, the logical effort is $\frac{5}{3}$, that is what I have written here. For the high skew gate, let me pick up a pointer. Now, the widths of the transistors are 4 and then on the NMOS side it is 0.5 on the PMOS side it is 4.

My benchmark inverter will change for the pull up circuit and then the pull down circuit. The benchmark inverter for the pull up circuit will be 2:1, the reason is its equivalent of the two transistors on the PMOS side will give me an effective transistor width, the equivalent transistor width of 2. That is the reason why I need a 2:1 inverter as the benchmark inverter for the pull up side of the circuit.

For the pull down side 0.5 is the width of the transistors and that is why my benchmark inverter will be 1:0.5. With this particular benchmark inverter, can we now calculate what is the logical efforts and what is the normalized parasitic. For the going up output the logical effort is nothing but,

$$g_u = \frac{4 + 0.5}{2 + 1} = \frac{4.5}{3} = \frac{3}{2}$$

The normalized parasitic for going up will be the almost,

$$P_u = \frac{0.5 + 0.5 + 4}{2 + 1} = \frac{5}{3}$$

For the logical effort, for the output going down it will be,

$$g_d = \frac{4 + 0.5}{1 + 0.5} = \frac{4.5}{1.5} = 3$$

The parasitic for the going down output will be nothing but,

$$P_d = \frac{4 + 0.5 + 0.5}{1 + 0.5} = \frac{5}{1.5} = \frac{10}{3}$$

Its average of $g_u$ and $g_d$ will give me the logical effort average 2.25. The normalized parasitic average here is $\frac{5}{3}$ and then $\frac{10}{3}$ and that is the average which will give me $\frac{5}{2}$. Hope this is clear.

If I look into this $\frac{5}{3}$ which is almost 1.66 in this particular value and then compare with that of 2.25 this is quite large. The $g_{avg}$ is quite large although this $\frac{3}{2} < 1.66$ for an unskewed inverter. If we can characterize the NOR gates in such a way that the output is always going up more frequently then I think we can have this the high skew NOR gate for the going up output.

For the low skew 2-input NOR gate it turns out to be very very interesting. The size of the low skew 2-input NOR gate. It is a low skew, that means that the NMOS should be more dominant. The NMOS is of size 1 here in the high skew, we wanted the PMOS should be more dominant. We had the same size as that of the unskew 4 and 4 and then made the NMOS size lower.

That is why it became high skew 2-input NOR gate. In the low skew version, if it is this 1 and 1 is taken from the unskewed 2-input NOR gate of 1 and 1 size. 1 and 1 is what we have and to make it low skew. In this particular circuit what we have done is on the PMOS side the strength has been reduced, the width has been reduced and the NMOS side the width is taken as same as that of the unskewed and thereby it becomes a low skew.

Low skew in the sense the NMOS transistor is more dominant now. If I have this particular size, my benchmark inverter for the going up output and then the going down output will be different. The benchmark inverter for the going up output will be nothing but 1:0.5 and for the going down will be nothing but 2:1 inverter because this size is 1 here, that is why my inverters NMOS size should be 1 and thereby my PMOS benchmark inverter will be 2 here.

In this particular case, the equivalent transistor for the two of these transistors in series will turn out to be the size of 1 and that is why we have the benchmark inverter size as 1 on the PMOS side and thereby the NMOS side benchmark inverter size will be 0.5, hope this is clear.

Now, if I have this particular benchmark inverter size as the logical efforts for going up will be nothing but,

$$g_u = \frac{2+1}{1+0.5} = \frac{3}{1.5} = 2$$

The parasitic for going up will be nothing but whatever is the output capacitance seen in this particular output node which will be,

$$P_u = \frac{2+1+1}{1.5} = \frac{8}{3}$$

The logical effort for the going down output which will be nothing but,

$$g_d = \frac{2+1}{2+1} = \frac{3}{3} = 1$$

The parasitic will be the output capacitance seen at the output node which will be,

$$P_d = \frac{2+1+1}{2+1} = \frac{4}{3}$$

The average of $g_u$ and $g_d$ turns out to be 1.5 and then the $P_{avg}$turns out to be 2.

Now if I start comparing between the unskewed 2-input NOR gate and a low skew 2-input NOR gate turns out that a low skew on an average also it is $1.5 < 1.66$ which is $\frac{5}{3}$. Parasitic average turns out to be the same P average is 2 here. The parasitic remains the same logical effort, there is an advantage for the low skew 2-input NOR gate. Because a logical effort is less than that of the logical effort of an unskewed 2-input NOR gate. This becomes kind of an very important circuit and then most of the memory designs we will have to use the 2-input NOR gates or whatever multiple inputs NOR gate. In that case, it is always prefer to have a low skew 2-input NOR gate, because this logical effort is less and thereby my overall delay will be less. Hope this is clear to everyone moving forward.

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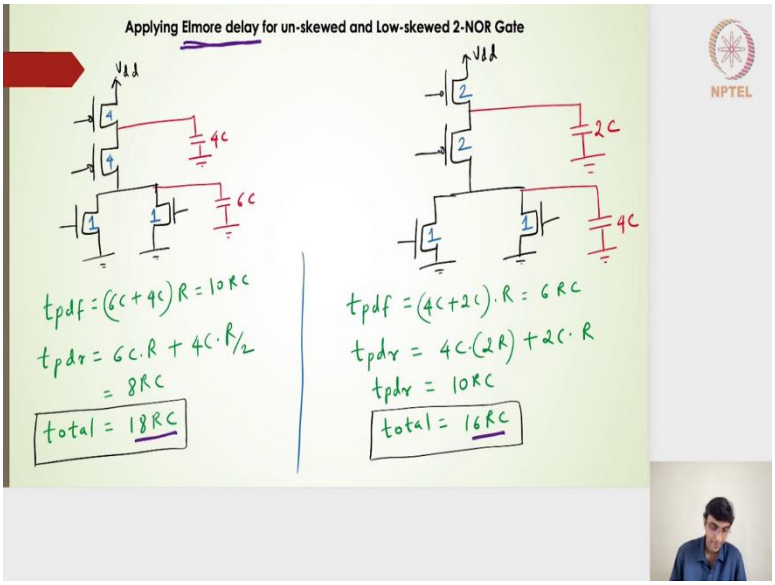


Now, what we had seen is for a 2-input NAND gate and for a 2-input NOR gate we realize that the logical effort for a 2-input NOR gate turns out to be best for a low skew 2-input NOR gate.

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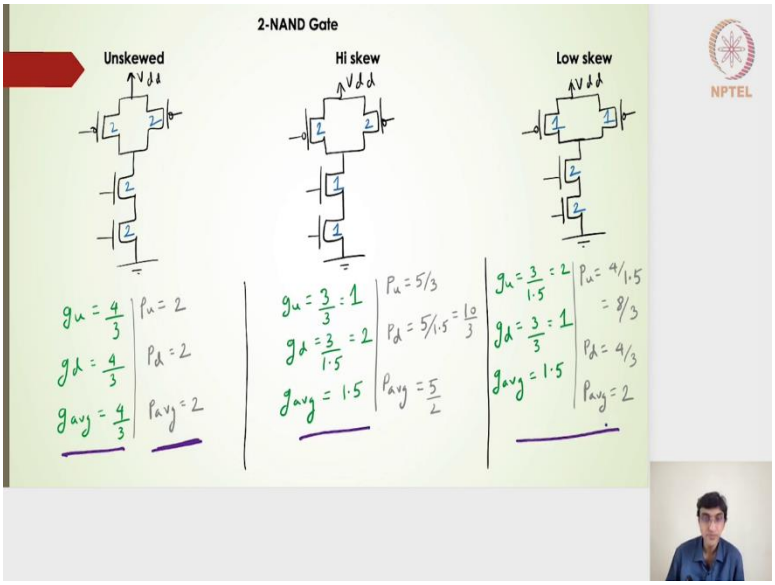


Whereas for a NAND gate, we notice that the logical effort and then the parasitic average turns out to be best for the unskewed one compared to the other gates. What it really means is somewhere the skewing will help me to reduce the overall delay, can we now find out the optimized width for the standalone gates which will give us the lowest delay. Moving in that particular direction, let us say that I have this unskewed 2-input NOR gate and here is a low skew 2-input NOR gate and then try to find out the overall delay.

This time we will try to apply the Elmore delay because that turns out to be more accurate than that of the linear delay model. If I use the Elmore delay method I need to use the inter node diffusion capacitance and that is why it has been reflected here. For an unskewed 2-input NOR gate I have the sizes of 4 and 4 and 1 and 1, at the output side I will see the capacitance of 6C.

In this particular inter node diffusion capacitance it is having a 4C. If I want to find out the overall delay I need to find out the propagation delay falling and then the rising and then total it up and then find out the average. Although, average is nothing but totally/2, but that is something I have just ignored it because it will be nothing but a linearly scaled by 0.5 times.

I am just calculating the overall total delay which is nothing but the propagation delay falling and then rising. The propagation delay falling will be nothing but 6C capacitance in this particular node and it is a falling output, one of them should be on, it will see a

switching resistance of R. So, 6C x R and then this 4C is also there, but the shared resistance turns out to be the R value.

$$t_{pdf} = (6C + 4C)R = 10RC$$

Propagation delay rising will be nothing but, both of these should be on and individual one of the transistors has a switching resistance of $\frac{R}{2}$, overall switching resistance will be R.

$$t_{pdr} = 6C\,R + 4C\frac{R}{2} = 8RC$$

$$\text{Total} = 18RC$$

The total RC turns out to be 18RC and if I try to find out for the low skew 2-input NOR gate and the inter node diffusion capacitance is 2C, the output node total capacitance is 4C because my sizes are 2, 2, 1, 1 and if I want to find out the propagation delay falling at this one of this transistor should be ON.

$$t_{pdf} = (4C + 2C)R = 6RC$$

On the rising side it will be nothing but,

$$t_{pdr} = 4C(2R) + 2C\,R = 10RC$$

$$\text{Total} = 16RC$$

The total delay will be nothing but $16RC < 18RC$, that is what we had actually calculated or we had noticed. In the previous slide, when we calculate the logical effort, although it will be used for the next stage what it says is overall that particular stage has somewhere the delay is less.

If I want to find out the best sizes, that my overall delay or the total delay in the sense the propagation delay falling and then the propagation delay rising sum of it should be less if that is the case I need to identify what is the best size.

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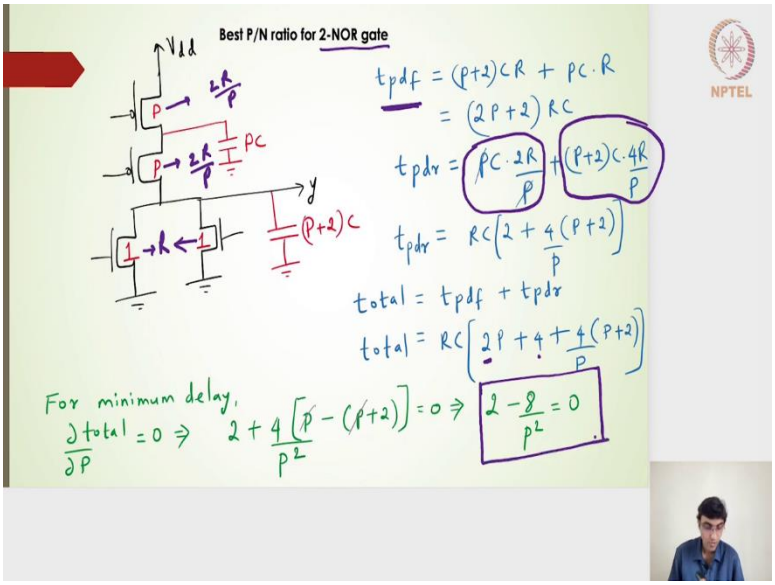


Moving ahead. If I want to find out the best size or in fact, I will go ahead and say that it is the best size ratio the best $\frac{P}{N}$ ratio. If I want to find out then I will have to use the Elmore delay method, find out the total delay that is nothing but the propagation delay falling and rising we will get a total delay expression in terms of a variable.

Then if I do a derivative of that and equate it to 0, I should be able to find out the best optimal sizes. In this particular case what I have done is, for a 2-input NOR gate I have taken a variable P on the PMOS side. P represents the width of the PMOS transistor in this particular case and there are two PMOS transistors for the 2-input NOR gate.

For the NMOS side, I have taken a size of 1. My overall capacitance and then the resistance now have to represent it in the form of the variable P. My overall diffusion capacitance is PC here because it will have the shared diffusion capacitance which will give me the capacitance of PC.

The output node capacitance reflected at the output side will be nothing but $P + 1 + 1 = (P + 2)C$, the switching resistance for this particular transistor will be $\frac{2R}{P}$. The switching resistance of this particular transistors will be again $\frac{2R}{P}$. The switching resistance of this transistor is nothing but R, and either one of them and now I should be ready to evaluate the expression of the propagation delay falling and then rising.

The propagation delay falling in this case will be nothing but,

$$t_{pdf} = (P + 2)CR + PC\,R = (2P + 2)RC$$

Propagation delay rising in this particular case will be nothing but,

$$t_{pdr} = PC\frac{2R}{P} + (P + 2)C\frac{4R}{P} = RC[2 + \frac{4}{P}(P + 2]$$

I will get this $t_{pdr}$ and $t_{pdf}$ and if I do the summation I will get the total delay in terms of the variable P, this is my overall expression for the total delay.

$$\text{total} = t_{pdf} + t_{pdr}$$

$$\text{total} = RC\,[2P + 4 + \frac{4}{P}(P + 2)]$$

We need the best $\frac{P}{N}$ ratio, we need the best P here because the other N side I have taken the width as 1. If I do a derivative with respect to P and then equated to 0, I should be able to find out the P value.

$$\frac{\partial \text{total}}{\partial P} = 0 => 2 + \frac{4}{P^2}[P - (P + 2)] = 0 => 2 - \frac{8}{P^2} = 0$$

If I take the derivative of this total expression. Finally, I will have this particular equation what it means is the P should be of the value plus or negative 2 we cannot have a negative value in the widths.

$$P^2 = 4 => P = 2$$

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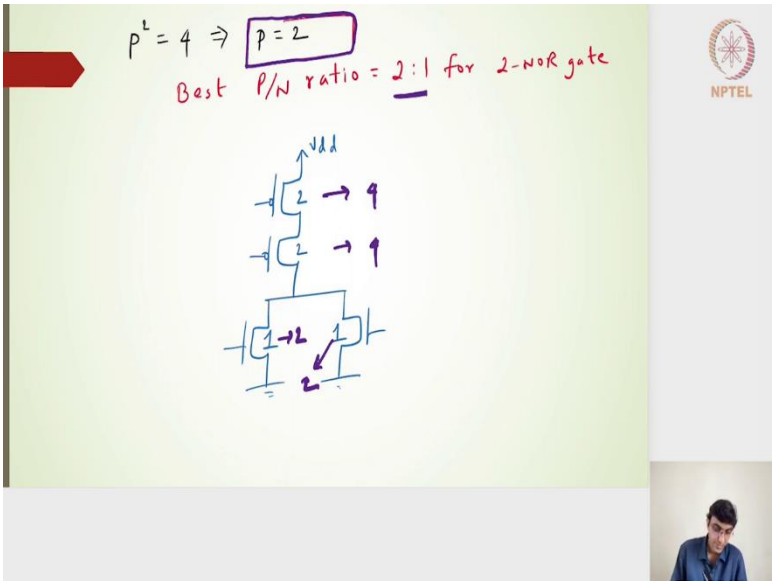


We will take the positive value, this will be my final expression which says that P by N ratio should be of 2:1 ratio for the 2-input NOR gate. What it really means is if I take the size of 2 and then 1 here it will give me the best delay. I can also take the size of 4 here.

I can take the size of 2 here and then the size of 2 here, it will also give me this similar total delay. This is also be 4:2 or 2:1 or 8:4, everything should give me the best delay, the best total delay in terms of the standalone circuit.

If I want to find out the best $\frac{P}{N}$ ratio for the 2-input NOR gate or for any other matter 2-input NAND gate or then inverter I need to find out the total delay expression then take the derivative with respect to one of the P variables and then equate it to 0 and then we should be able to get that best $\frac{P}{N}$ ratio,for the 2-input NOR gate turns out to be 2:1 ratio.

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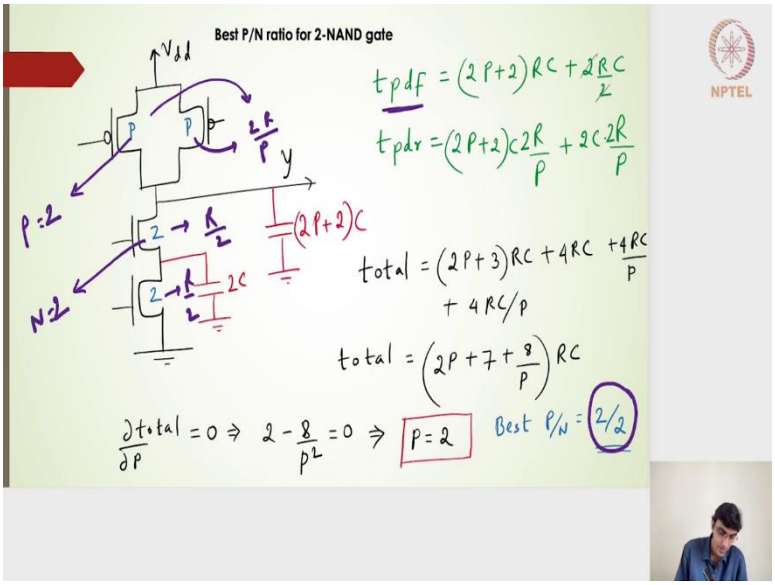


Similarly, can we find out for the 2-input NAND gate, what is the best ratio? For the 2-input NAND gate I have taken on the NMOS side the size of 2 and on the PMOS side I have taken the variable P here. Which means that the P should be the PMOS width on the N- NMOS side it is nothing but the variable 2.

If I have the total capacitance seen at the output node will be nothing but P + P + 2 which will be 2P + 2 capacitance. In this particular inter node diffusion capacitance, it will be 2C. The total propagation delay falling in this particular case will be nothing but (2P+2). This particular capacitance value multiplied by switching resistance of $\frac{R}{2}$ this will have a switching resistance of $\frac{R}{2}$ this should have a switching resistance of $\frac{2R}{P}$. Of course, this 1 should also have the switching resistance of $\frac{2R}{P}$. If I have this switching resistance then I should be able to find out what is the propagation delay falling and it turns out to be,

$$t_{pdf} = (2P + 2)RC + 2\frac{R}{2}C$$

Propagation delay rising will be nothing but,

$$t_{pdr} = (2P + 2)C\frac{2R}{P} + 2C\frac{2R}{P}$$

The total expression turns out to be this which is something about,

$$\text{total} = (2P + 3)RC + 4RC + 4\frac{RC}{P} + 4\frac{RC}{P}$$

$$\text{total} = \left(2P + 7 + \frac{8}{p}\right) RC$$

If I take the derivative of this particular expression with respect to P it will be,

$$\frac{\partial \text{total}}{\partial P} = 0 \Rightarrow 2 - \frac{8}{P^2} = 0 \Rightarrow P = 2$$

The best $\frac{P}{N}$ ratio even for the 2-input NAND gate is actually 2:2, because the best p turned out to be the value 2 and N we have considered it to be 2. The best $\frac{P}{N}$ ratio turns out to be 2:2 or 1:1.

If you remember for the 2-input NAND gate, the unskewed inverter, the unskewed 2-input NAND gate, the unskewed configuration had the PMOS width of 2 and NMOS width of 2 which was giving the best logical effort and then the best parasitic equation across the different high skews and low skews. Hope this is clear how do we evaluate the best $\frac{P}{N}$ ratio.

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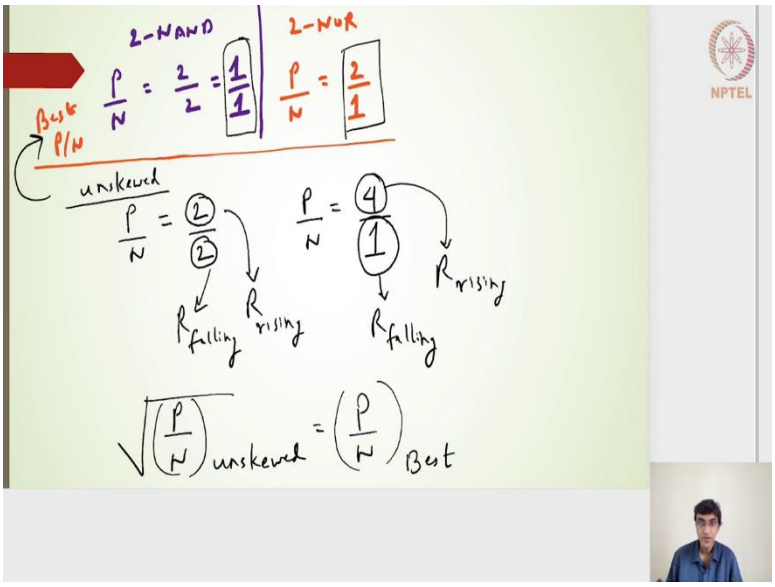


What we had up till now, what we had done for the 2-input NAND gate the best $\frac{P}{N}$ ratio someone will write it as best $\frac{P}{N} = \frac{2}{2}$. For the 2-input NOR gate the best $\frac{P}{N} = \frac{2}{1}$, this is the best. I am going to write it somewhere that this is the best $\frac{P}{N}$ ratios. Now, if I want to do an

unskewed one, for the 2-input NAND gate, $\frac{P}{N} = \frac{2}{2}$. which is actually nothing but here I can say that it is 1:1, I will come to that and this is 2:2 for an unskewed one.

The size of 2 is required on the NMOS side to get the falling resistance at the benchmark inverter and the size of the PMOS side 2 is there for the 2-input NAND gate because you know either of the branch will be on, and then I will see have the rising resistance equal to that of the 2:1 benchmark inverter.

If once I have this unskewed form which is considered from making the equal rise time or the equal falling time. Here if I have the size of 2 and 2 I will have the same falling resistance and then the rising resistance. I am going to write it as the rising resistance and then the falling resistance turns out to be R and it matches with that of the 2:1 inverter.

Similarly, here 4:1, I have taken the size as such that again the rising resistance and then the falling resistance matches with that of 2:1and it should be equal to that of the R. In that case if I have an unskewed version I should be able to get to the best $\frac{P}{N}$ ratio. I can do that if I have an unskewed version and if I take the square root of the unskewed version of the $\frac{P}{N}$ ratio.

Then, this 1 should be able to give me the $\frac{P}{N}$ ratio. In fact, I am going to write it as the best $\frac{P}{N}$ ratio. Let us try to validate this if I actually have an unskewed version of the $\frac{P}{N}$ ratio which is nothing but $2/2$ for the 2-input NAND gate and $4/1$ for the 2-input NOR gate. If I take the $\sqrt{\frac{2}{2}}$ it will give me the square root of this output of the $\sqrt{\frac{P}{N}}$, for an unskewed version will give me 1:1 which is what I have written here the 1:1.

Similarly for the 2-input NOR gate the unskewed 2-input NOR gate gives me 4:1. If I take the square root of that here 4:1 which will give me 2:1 and that is what we get here 2:1, hope this is clear.

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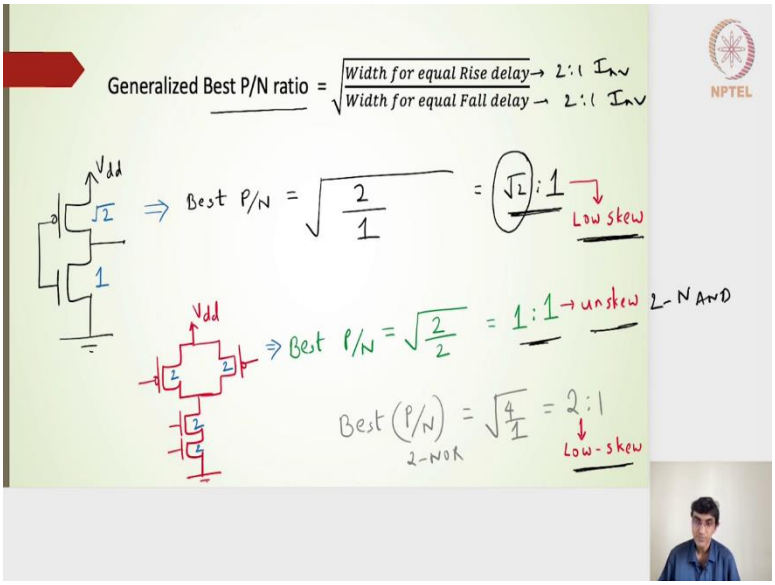


To generalize the best $\frac{P}{N}$ ratio it is actually the width for the equal rise delay or the fall delay with respect to the 2:1 inverter.

$$\text{Generalize Best}\frac{P}{N}\text{ ratio} = \sqrt{\frac{\text{Width for equal rise delay}}{\text{Width for equal fall delay}}}$$

In another sense if I have an unskewed version of the gates whatever it would be a 2-input NOR gate or a N input NOR gate or a 2-input NAND gate or any other combinational gate, if I can form the unskewed gate. Unskewed gate formation is very very simple, I need to make sure that the falling resistance and then the rising resistance matches with that of the 2:1 inverter.

If I can get that the square root of the width of those particular inputs, where the inputs connected to the PMOS and the inputs connected to the NMOS, if I can identify what is the square root of that width and the output of the square root should give me the best $\frac{P}{N}$ ratio.

The best $P/N$ ratio for actually 2:1 inverter which is an unskewed inverter turns out to be the $\sqrt{2}:1$ which is again a low skew inverter because the low skew because this size it become less than that of 2 and thereby the PMOS is going to or rather the NMOS is going to be more dominant.

Again for a 2-input NAND gate I have taken an expression 2:2. The best P/N ratio is nothing but the square root of 2:2 which is 1:1 which is again an unskewed for a 2-input NAND gate. The best P/N ratio for a 2-input NOR gate is nothing but 2:1, which is again a low skew. For inverter and then for the a NOR gate turns out to be the low skew a version which is better in terms of the overall delay. Whereas, for the 2-input NAND gate unskewed version is better in terms of the overall delay.