Design and Analysis of VLSI Subsystems
Dr. Madhav Rao
Department of Electronics and Communication Engineering
Indian Institute of Information Technology, Bangalore

Lecture - 42
Introduction to Skewed gates

Hello, student's. In this particular lecture, we will take a look at the Skewed Gates. Previously we had seen the asymmetric gates and how do we evaluate the logical effort for the asymmetric gates. Today in this particular lecture we will look into this skewed part of the gates. Please note that skewing is not equivalent to the asymmetric gates.

Asymmetric gates means the input capacitance seen by the several inputs are different. If I have two inputs to the particular gate and if their widths are designed in such a way that their input capacitance for the several of the inputs if they are different and it is called as an asymmetric gate. Whereas, the skewed gates even though the inputs might see the same capacitance based on the designs, whatever we have the skewing happens with respect to the pull up circuit and pull down circuit.

In that sense for an inverter and if I say that it is a high skew, that means that the PMOS is more dominant with respect to the NMOS, what it indirectly means that the PMOS has a better width, the better current driving strength than that of the NMOS. Similarly, a low skewed inverter will resemble the inverter having or dominated by the NMOS transistors and not by the PMOS transistors.

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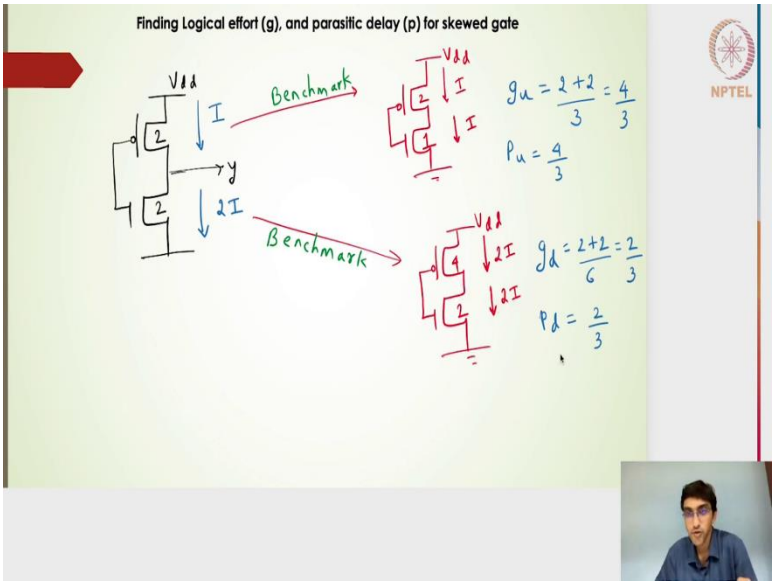

Here is our usual inverter a primitive circuit, this is the size of the PMOS transistor is 2 here and then the size of the NMOS transistor is 2 here and it is not 2:1. What it really means is it is a skewed inverter and if I have a skewed inverter how do I find out the logical efforts and how do I find out the normalized parasitic that is seen at the output node.

What we had been saying is while we set up a benchmark inverter like for any gate, if I want to find out the logical effort or the normalized parasitic delay we set aside a benchmark inverter and we used to say that the benchmark inverters current should be the same as that of this particular gates the current.

In this particular case, because it is a skewed inverter the current strength of the PMOS will be different than that of the current strength of the NMOS. Now, one can always say that both of them are in series, so what is that current strength because all the series transistors we are eventually likely to pass the same current here. But what I really meant was if I have a capacitance here at the output node this particular capacitance charging current will be different than that of the capacitance discharging current because the driving strength or the width here which has been designed for the particular transistors are different.

In that sense although the widths are same here in this particular case the betas of the PMOS and then the NMOS are different and that is why the current strength value will be different. In that sense what we are saying is the output current in this particular node while

it is charging through the PMOS that particular current will be different than when the capacitor is actually discharging through the NMOS.

Now the question is, if I want to evaluate the logical effort or the normalize parasitic delay factor, now what should be the benchmark inverter. The benchmark inverter should be designed in such a way that we should have a benchmark inverter, in such a way that its rising current should be the rising current whatever this particular gate will give and then its falling current will be whatever this particular gate will give.

For example, if I want to find a benchmark inverter so that I can evaluate the logical effort, the benchmark inverter for the falling current should give me a current of 2I and the reason is because this NMOS here it is size to 2, that means the current strength will be 2 or rather the falling resistance is $R/2$ and I will get a current strength of 2I or the falling resistance to be $R/2$ only if I have a benchmark inverter with an NMOS size of 2 and the benchmark inverter should always have the equal β. What I mean is the benchmark inverter should always mean a ratio of 2:1 or 4:2 or 8:4 and so on. In that sense if I making this 2 size here, that I will get the falling current as 2I, so as to match with that of this gates NMOS transistor size of 2, my PMOS size of the benchmark inverter will be twice that of the size of the NMOS transistor here, it should be 4 here. I will now have the benchmark inverter of 4:2.

Similarly, if I want to find out the benchmark inverter for the rising current. The rising current of the charging current is nothing but I here because you know the size of 2 in the PMOS side will give me a current of 1I. I need the same charging of the rising current in my benchmark inverter. I need to have a size of 2:1, which will give me the rising current of I here in the benchmark inverter, hope this is clear.

What we now have is 2 benchmark inverters, one for the rising output and another for the falling output. One for the rising output this is the benchmark inverter and then one for the falling output. If I have 2 benchmark inverters, I cannot get one logical effort.

In that sense I will have two logical efforts defined now. The logical efforts for the output going up and then the logical effort for the output going down, it is represented as g_u and g_d and g_u will be nothing but, if I consider the input capacitance of this particular gate will be nothing but,

$$g_u = \frac{2+2}{3} = \frac{4}{3}$$

My logical effort for the rising output or the going up output will be,

$$P_u = \frac{4}{3}$$

My parasitic for the rising output will be nothing but the 4c seen at the output node and then the 3c seen in this output node of the benchmark inverter of 2:1. I will have the pu value parasitic for going up will be nothing but $4c/3c = \frac{4}{3}$.

Similarly, for the logical effort for going down will be nothing but,

$$g_d = \frac{2+2}{6} = \frac{2}{3}$$

The parasitic for going down will be again,

$$P_d = \frac{4}{4+2} = 2/3$$

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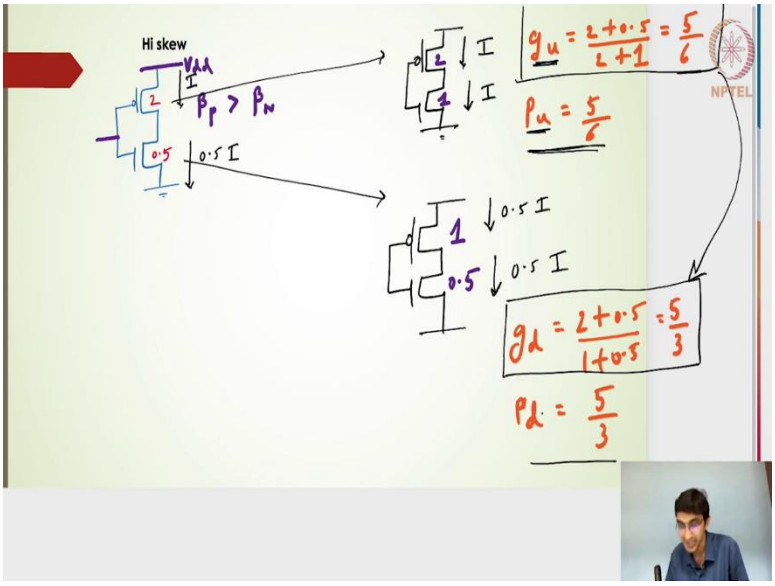

I will write try to derive the benchmark inverters for this particular high skew inverter. This is an high skew network. I have a V_{dd}rail here and then the PMOS transistor and then the NMOS transistor. The PMOS transistor has a size of 2 and then NMOS has a size of

0.5. Which means my β_p is actually higher than that of the β_N and that is why it is called as an high skew inverter.

Now, how do I find out the logical efforts and then the parasitic which has a different size the PMOS and NMOS has a different size. I need to draw two benchmark inverters again, one for the rising output and another one for the falling. In that sense, I will try to draw the benchmark inverter should give me the rising current here will be nothing but I, here the falling current is nothing but 0.5 I, here the rising current is nothing but I.

For my benchmarking inverter it should be nothing but the size of 2:1. I will draw my benchmark inverter with a size of 2:1, which will give me a rising current of I and then the falling current of I. Similarly, for 0.5 width my benchmark inverters, this will be my inverter here and then this connected to another inverter. The size of this particular benchmark inverter should give me 0.5 as the current. I will have 0.5 as the size here and then it should be the size of 1, 2:1 ratio is maintained in the benchmark inverter. This will give me the falling current of 0.5I, and the rising current of 0.5I.

My benchmark inverters are ready now and now I need to evaluate what should be the logical effort for the going up and then logical effort for the going down the output signal. The logical effort for going up will be nothing but,

$$g_u = \frac{2 + 0.5}{3} = \frac{5}{6}$$

Its parasitic for going up will be nothing but,

$$P_u = \frac{5}{6}$$

The logical effort for going down signal is nothing but,

$$g_d = \frac{2 + 0.5}{1 + 0.5} = \frac{5}{3}$$

The parasitic for going down will again be nothing but,

$$P_d = \frac{5}{3}$$

This is how we will evaluate the logical effort and then the parasitic it is a very interesting thing here is the logical effort turns out to be less than 1, $\frac{5}{6} < 1$ especially for the one which is the rising one. The going down it is kind of compensated by the going down the logical effort, it has a very high the logical effort. Similarly, we can see the parasitic is $\frac{5}{6} < 1$ which is the normal case for the 2:1 inverter, we will have a parasitic of 1, but here because of the skewing technique this parasitic for the going up is less than 1 and parasitic for going down is been compensated by $\frac{5}{3}$.

With a higher skew, that means the PMOS is more dominant it is likely that the output will be pulled up and that is the reason we will have a lower logical effort and then the normalized parasitic delay factor. A higher skew will always be associated with a lower value of g_u and the lower value of P_u.

A lower skew inverter, that means the NMOS is kind of dominated, that means the circuit pulls down the output efficiently, in that sense the logical effort for the going down. The g_d and then the normalized parasitic delay the pd for the going down will be less if it is a low skew inverter. Hope this is clear, moving ahead.

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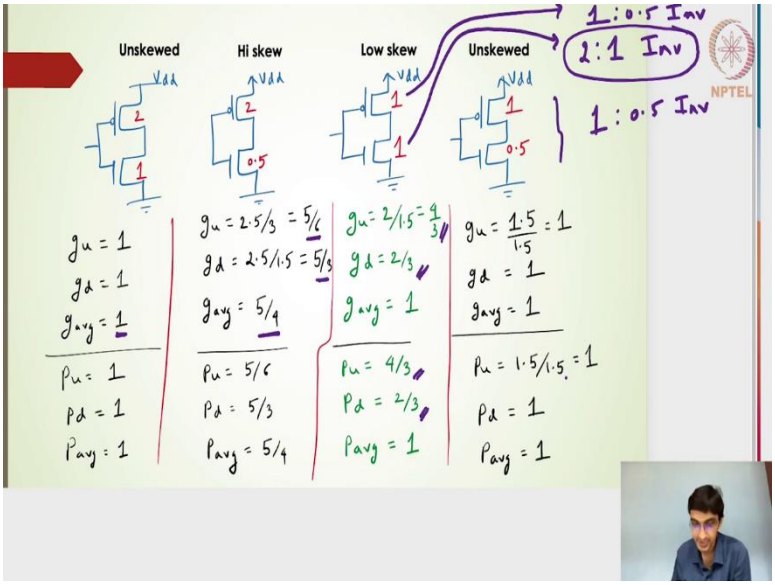

In this particular, I have drawn a series of circuits starting with the unskewed inverter. Unskewed inverter we anyways know the g_u, g_d and g_{avg} is nothing but the same value as 1, also all the parasitic for going up going down and average value is 1. High skew,

recently in the last slide we just had a look at it, it is $\frac{5}{6}$ for going up and then the gd $= \frac{5}{3}$, average turns out to be $\frac{5}{4}$.

It is kind of slightly higher than that of 1 of the unskewed inverter. Parasitic is nothing but $\frac{5}{6}, \frac{5}{3}$ and $\frac{5}{4}$ very very similar to that of the logical effort. For the low skew having 1 and 1 here, that means that the NMOS β here is more than that of the β of the PMOS.

Although, the width is same this one is called as a low skew because the β of this NMOS transistor is higher than the β of the PMOS right. Suppose, if I have this benchmark inverter for this circuit will be 1:0.5. 1 on the PMOS side and then 0.5 on the NMOS side and similarly for this the benchmark inverter will be nothing but 2:1. I am going to write it as the benchmark inverter or inverter here just to ensure that what we are talking about.

The logical effort for going up will be nothing but $g_u = \frac{2}{1.5} = \frac{4}{3}$ and for the parasitic for going up will be nothing but $P_u = \frac{2}{1.5} = \frac{4}{3}$, g_d the logical effort for going down will be seeing a different benchmark inverter which will be 2:1 inverter. It is logical effort for going down will be $g_d = \frac{1+1}{2+1} = \frac{2}{3}$ 1 and the parasitic will be $P_d = \frac{2}{3}$, the average of this turns out to be 1 and 1, because it is a low skew the $g_d < 1$, the $P_d < 1$ as we had seen for the high skew the $g_u = P_u < 1$, but however, it is kind of compensated for the other side. For the low skew the logical effort for going up tends to be more and then the parasitic for going up will also be more than 1.

Unskewed inverter one more unskewed inverter 1:0.5 it is still called as an unskewed inverter because the β of the PMOS and NMOS are remains the same and it will be very very similar so 1:0.5 the benchmark inverter for both of them will be 1:0.5 inverter. Its g_u value g_d value and g_{avg} value will stay at 1 and P_u, P_d and P_{avg} value will stay at 1. Again, hope this is clear.

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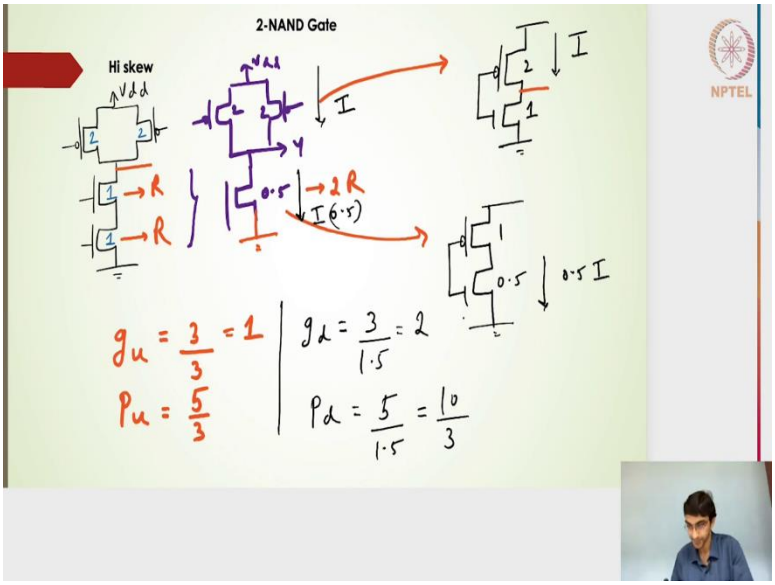

Moving ahead let us take a look at the 2-input NAND gate, a high skewed 2-input NAND gate is written here and it is called as an high skewed because if I look closely into this the equivalent transistor for this 2 series transistor will be nothing but, if it is 1 and 1, I will have the equivalent transistor for this will be 0.5. The reason is very simple this one will give me a resistance of R switching resistance of R, this one will give me a switching resistance of R.

If I want the equivalent resistance, equivalent transistor should have a switching resistance of 2R and it is possible only if I have 0.5 as the width. This is my equivalent resistance of 0.5. 0.5 with respect to 2 in parallel. These 2 are in parallel. I will have 2 of them in parallel size of 2 and 2, this being, if 1 of the branch is on, the other one under worst case condition we say that this input is on or this particular transistor is on and then this is off. we will have 2:0.5, thereby we have this the PMOS being more dominant. That means, that the β of the PMOS is higher than that of the βof the NMOS and that is why it is called as an high skew 2-input NAND gate.

Now, if I want to find out the logical efforts for going up and going down and parasitic for going up and going down, I need to find out the benchmark inverters for the going down signal and going up signal. The benchmark inverter for the going up signal and then the going down signal I am going to rewrite this. This will be nothing but 0.5 is the width, its current for going down should be nothing but 0.5I.

What I need is the benchmark inverter of 1:0.5 is my benchmark inverter which will give me the going down current of 0.5I. My benchmark inverter for going up signal which has the current of now if 1 of the branch is on it will have a current of I, my benchmark inverter will be nothing but 2:1 because it will give me a current of I.

Now, if I have the benchmark inverters ready, I can easily find out the logical effort of the going up signal. The going up logical effort for going up signal will be nothing but,

$$g_u = \frac{2+1}{3} = 1$$

Parasitic for going up will be nothing but whatever is the capacitance seen at the output node is,

$$P_u = \frac{1+2+2}{3} = \frac{5}{3}$$

For going down signal again the input capacitance is,

$$g_d = \frac{3}{1.5} = 2$$

The parasitic for going down will be nothing but,

$$P_d = \frac{5}{1.5} = \frac{10}{3}$$

Hope this is clear for a 2 input NAND gate. We have 2 different benchmark inverters the one for evaluating the logical effort for the going up signal we have the benchmark inverter as 2:1 for the logical effort for going down signal we have the benchmark inverter as 1:0.5, moving ahead.

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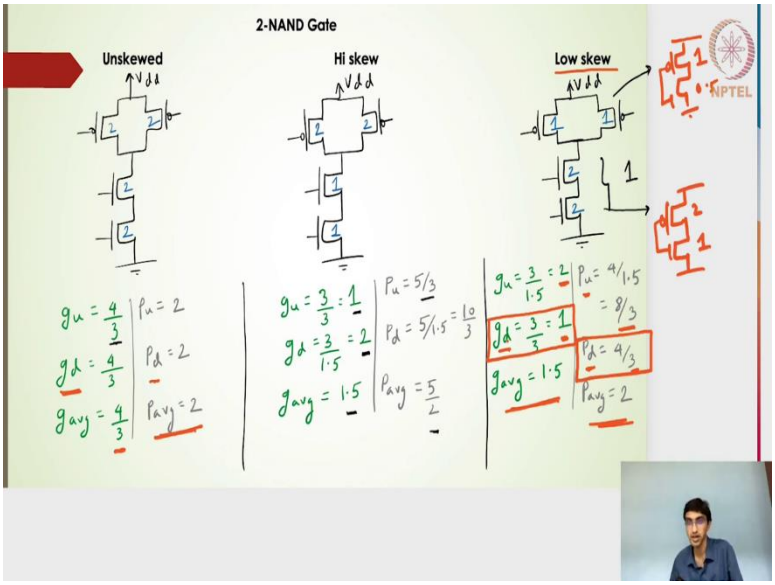

For a 2 input NAND gate I have this unskewed high skew and low skew unskewed this is something we already know $\frac{4}{3}, \frac{4}{3}$ and $\frac{4}{3}$, parasitic is nothing but 2, 2 and 2, for the high skew inverter which we had seen in the previous slide it turns out to be 1, 2 and parasitic is $\frac{5}{3}$ and $\frac{10}{3}$. Its average value turns out to be 1.5 and the average value on the parasitic is turns out to be 2.5.

For the low skew inverter, for the low skew 2-input NAND gate our sizes are 1 and 1 here and 2 and 2 that means, that this one will give me a an equivalent transistor with a width of 1, because this is $\frac{R}{2}$ and then this is $\frac{R}{2}$. The total switching resistance will be R, a transistor with a size of 1 will give me an equivalent switching resistance of R.

On the PMOS side, the width is 1 and 1, the width is 1 and 1, that means the switching resistance is nothing but 1 1 R or rather R 2 R. In that sense I think this width of 1 is going to have a less β than that of on the pull down circuit side. Its equivalent resistance on the pull down side will be nothing but a one single transistor with a size of 1 giving a β of that NMOS which is higher than this particular β of this particular PMOS.

It is the benchmark inverter for this and this I will try to put it in a different color. The benchmark inverter for this with a size of 1 on the PMOS side and then 0.5 on the NMOS side. This particular for the going down signal the benchmark inverter will be 2:1 because its equivalent transistor size turns out to be 1, I will have 2:1.

The logical effort for going up is nothing, but the input capacitance is nothing but

$$g_u = \frac{3}{1.5} = 2$$

Parasitic will be nothing but

$$P_u = \frac{1+1+2}{1.5} = \frac{4}{1.5} = \frac{8}{3}.$$

Logical effort for going down signal we will have,

$$g_d = \frac{2+1}{3} = \frac{3}{3} = 1.$$

Parasitic for going down signal will be nothing but,

$$P_d = \frac{2+1+1}{3} = \frac{4}{3}2.$$

The average is,

$$g_{avg} = 1.5 \ \& \ P_{avg} = 2$$

The 2 input NAND gate, if I actually look into the g average value and the p average value turns out to be actually $1.5 > 1.33$. For an unskewed inverter it is actually 1.33 p average is nothing but 2 which is same as that of the unskewed inverter.

The only advantage in this g_d value which is actually 1 and then the P_d value which is nothing but $\frac{4}{3}$. In a circuit if I have the going output signal coming from the 2-input NAND gate. If I have a 2-input NAND gate and if it is characterized to some extent that we will have lot of outputs going down, then we can actually resize this we can actually skew it in such a way that I will have a lesser g_d value lesser P_d value then having the regular g_d and P_d value.

If I have characterized and if I have noticed the circuit or whatever the digital circuit system where the 2-input NAND gate is going to give me lot many times going down signal then why do not we do it a low skew 2-input NAND gate, that is an advantage of course, one has to pay the price.

If it is low skew on the higher side whenever the output rises I will be having a larger delay because my g_u value and the P_u value is higher. One has to compensate for the other side,

but if it is more number of times the output is going down then why not have this $g_d = 1$ and $P_d = \frac{4}{3}$.