Design and Analysis of VLSI Subsystems
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Lecture - 41
Asymmetric Gates analysis using short-channel current model

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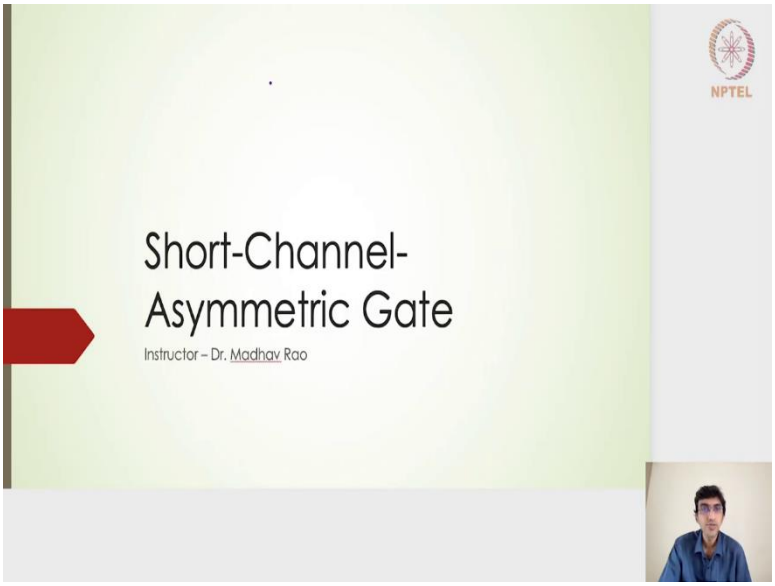

Hello students, welcome to this lecture on the short channel current for the Asymmetric Gates. What I meant by the short channel current is for an asymmetric gate, we were able to estimate the logical efforts using the long channel current model. In this particular lecture we will see how to evaluate the logical efforts for an asymmetric gates using the short channel current model.

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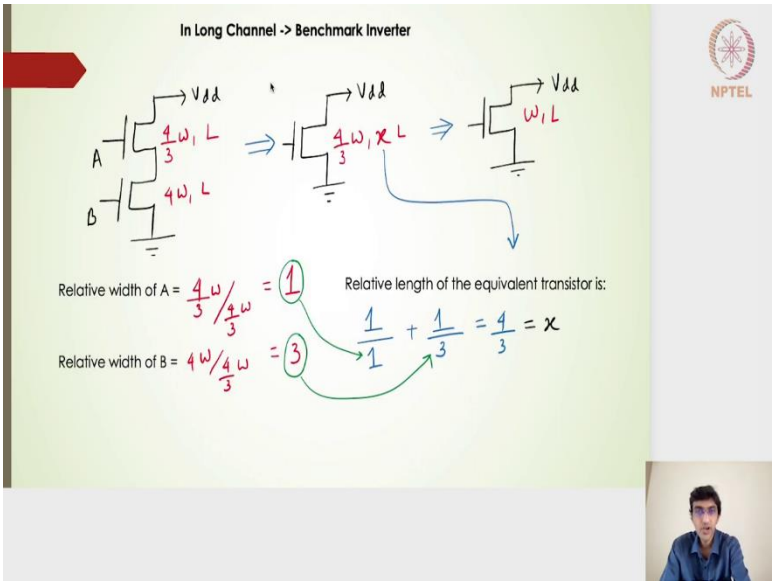

Moving on, what we have here is the long channel, if we have a 4/3 W, the two transistor which would be considered as this particular two transistor which would be considered as the pull down circuit of the two input NAND gate. One having a width of 4/3, the other one having a width of 4W, of course the channel length are same.

Its equivalent single transistor was 4/3 W,xL and then this particular x value which we can evaluate saying that it is nothing but the summation of the reciprocal of the relative widths of the both transistors.

If I consider the relative width of the transistor A it will be nothing but (4/3)/(4/3), and the relative width of the B transistor will be nothing but 4/(4/3) turns out to be 1 and 3.

If I take the reciprocal of this it will be 1 and 1/3 and then if I add it up, I will get this particular x value which is nothing but 4/3 and that is what its equivalent transistors length will be scaled to 4/3.

We will have the equivalent single transistor representing these two series transistors of different widths as 4/3 W and 4/3 L which is nothing but W,L. What it really means is the current, that is the output current of this particular single transistor will be equal to this particular output current of the single transistor, which will be equal to that of the output current of these two series transistors.

That is why we can have a 4/3 and 4 here which will be equivalent to that of the 2:1 inverters NMOS transistor, here there is a 1 here. That is where the 2:1 inverters NMOS

transistor. 1W represents the same as nothing but the 1W which will give me the same current as that of the two series transistors output current.

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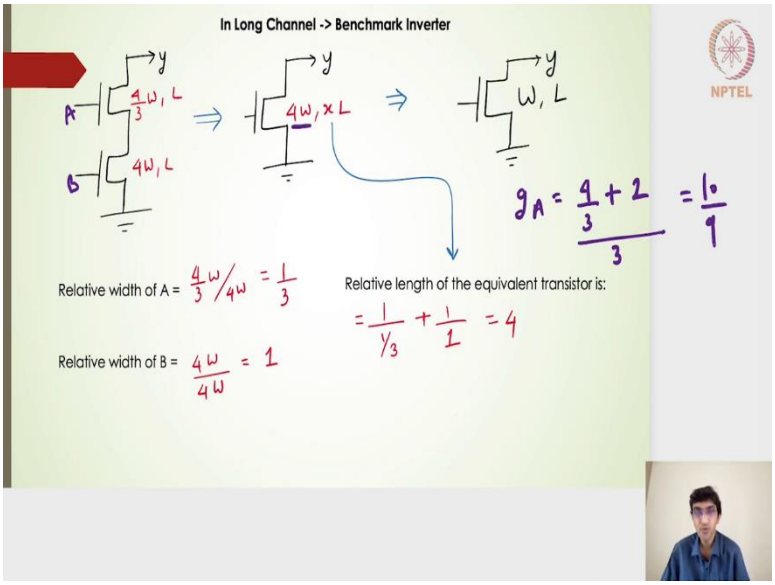

We can also do it this way, if I consider instead of 4/3 here, if I consider 4W I can find out the x value which will be nothing but again the same rule of the sum of the reciprocals of the relative width.

The only thing that will change is now the relative width of these two transistors will now change with respect to this width which is now a modified width for the single equivalent transistor.

For the relative width of this transistor A = $\frac{\frac{4}{3}w}{4w} = \frac{1}{3}$ and then this transistor B = $\frac{4w}{4w} = 1$. The summation of the reciprocals of this, $\frac{1}{1/3} + \frac{1}{1} = 4$. My equivalent single transistor length will be nothing but 4 which turns out to be W,L.

Again it is the same thing as we had seen earlier, but just that the width is different now in this particular transistor. In the earlier case, we had taken a different width and that is why we obtained a different length here we have taken a different width and then that is why we got a length of 4L.

This we were able to calculate, if I want to find out what is the logical efforts of the transistor A or rather the input A and the input B, I know what should be its input

capacitance which is nothing but the width. Whatever the width is given on the NMOS side and then the PMOS side sum it up and then divide it by the 2:1 inverter, divide by the input capacitance seen by the 2:1 inverter.

If I want to find out the logical effort of A here it will be nothing but 4/3, I am assuming it will be a 2- input NAND gate. I will have a 2 size on the PMOS side or the pull up side and then divided by the 2:1 inverter will give me 3. This will be my logical effort, which will be close to 10/9 which is very very less than that of 4/3. Similarly, if I use a short channel current model, what should be its logical effort? that is the question we have.

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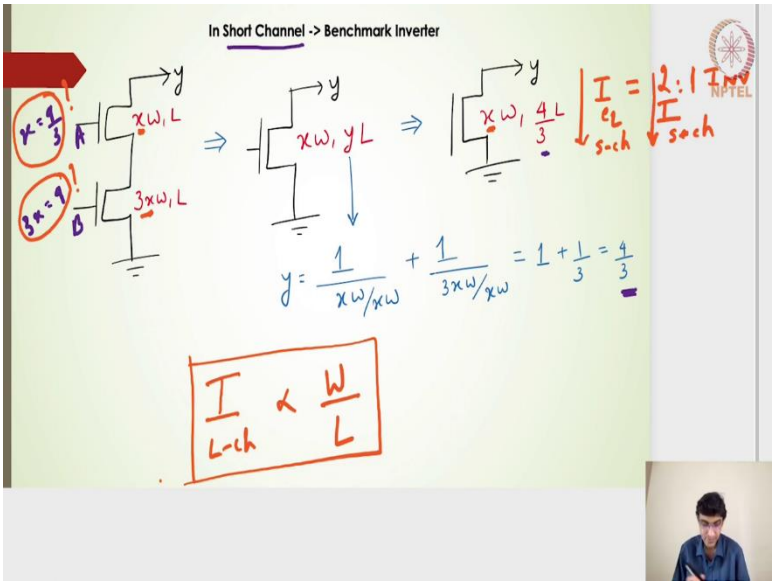

Proceeding further let us try to analyze the short channel current model and then let us say that we have the two transistors I have marked it as xW,L and 3xW,L. Then in our earlier case actually x was 4/3. We had a one transistor of 4/3 here and another transistor as 3 x (4/3) which was nothing but 4, 3x = 4. In the long channel model whatever earlier we had seen it is nothing but 4/3 here and then 4W here 4/3 W here and 4W here.

Now, I am taking an xW and then 3xW it is equivalent single transistor width will be xW. We had taken 4/3 W and then y was estimated to be 4/3 W and y will be what? y will be nothing but we will use the same principles of the sum of the reciprocals of this relative width.

The relative width of the transistor A and the transistor B. The transistor A will be nothing but xW/xW = 1 and relative width of B will be 3xW/xW = 3. It will be nothing but the sum,

$$y = \frac{1}{xw/xw} + \frac{1}{3xw/xw} = 1 + \frac{1}{3} = \frac{4}{3}$$

My y is nothing but 4/3 here and xW. What we really need is to identify what is x whether it is really 4/3that is a question mark and 3x whether it will be really 4 that is the question mark.

Once we identify what is x, I think 3x can be evaluated, If I can identify this x value xW,4/3 L which is going to give me a current of some current here and I am going to write it as equivalent current. This current should be equal to my 2:1, 2:1 inverter current.

I am going to say that this is my 2:1 inverter current. Whatever x is that if the current of xW,4/3 L matches with that of the 2:1 inverter and of course it will be this particular current will also be the short channel current.

I am going to write it as short channel, it will be the short channel current. Whatever is the xW that we are going to design, whatever is the x value this current should match with that of the 2:1 inverter short channel current and that x whatever it could be it may not be 4/3, it may be something else that will be the x value and that x value we will have to put it here, which is xW and then 3xW. We have two transistors in series with an asymmetric gate size, the sizes are not same.

The sizes are different here one is an xW another one is a 3xW. If whatever is the x value here my asymmetric gate size should be of that particular width it cannot be 4/3 and it cannot be 4. Because, as per our short channel current model we need the currents to be same and then the short channel current model may not give us the same current as that we expect in a long channel model.

Remember that the long channel model that W and L for a current they have a very linear relationship, I is the current in a long channel current model is directly proportional. I am going to rewrite this is directly proportional to the width and then to the length.

Whereas in the short channel that may not be the case. It is directly proportional to the W, but L parameter depends on the denominator in terms of the critical voltage and that is something we will see now.

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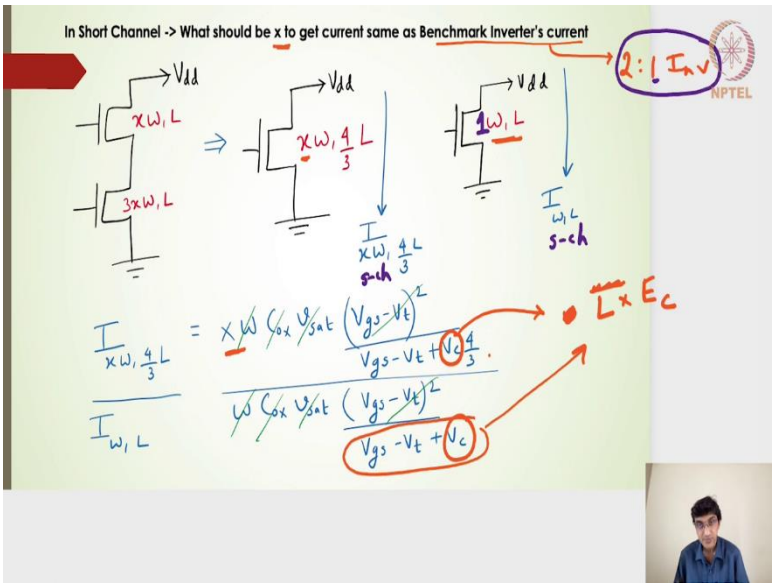

Moving ahead, what we really want is we should find out x to get the current same as that of the benchmark inverters current. The benchmark inverters current is at this point of time we have 2:1 inverter.

The 2:1 inverter this is the current we have W,L because this is my 1W which is on the pull down side of the 2:1 inverter, this one represents this 1W. This current here the output current here will be I_{WL}. Of course, this should be the short channel current and xW, $\frac{4}{3}$L. This particular current will be nothing but $I_{xW,4/3\,L}$, and of course, I will consider the short channel current.

I am going to write S-ch, what we need is these two currents to be the same. I will have a current equation of the 2:1 inverter the unit NMOS current. The unit NMOS short channel current which is written here in this particular denominator point which is nothing but,

$$I_{w.L} = wC_{ox}v_{sat}\frac{(V_{gs} - V_t)^2}{V_{gs} - V_t + V_c}$$

I will write the current of this particular transistor which is $xW, \frac{4}{3}L$ in the short channel which is nothing but,

$$I_{xw.\frac{4}{3}L} = xwC_{ox}v_{sat}\frac{(V_{gs}-V_t)^2}{V_{gs}-V_t+V_c\frac{4}{3}}$$

Then this particular V_c is for the unit channel length of L, what we had said was this $V_c = LE_c$.

If the length is scaled by $4/3$ times, then it should have $\frac{4}{3}L$ xEc. That is where this $4/3$ is coming into the picture. Hope these two equations are clear and what we really need is this current and this current should be same, $xW, \frac{4}{3}L$ whatever the falling current is there that should match with that of the falling current of W,L which is our benchmark inverters current. That is when if we do that then we should be able to find out what is the real x value.

What I have done is I have taken the ratio here and that should be equated to 1,

$$\frac{I_{xw.\frac{4}{3}L}}{I_{w.L}} = \frac{xwC_{ox}v_{sat}\frac{(V_{gs}-V_t)^2}{V_{gs}-V_t+V_c\frac{4}{3}}}{wC_{ox}v_{sat}\frac{(V_{gs}-V_t)^2}{V_{gs}-V_t+V_c}}$$

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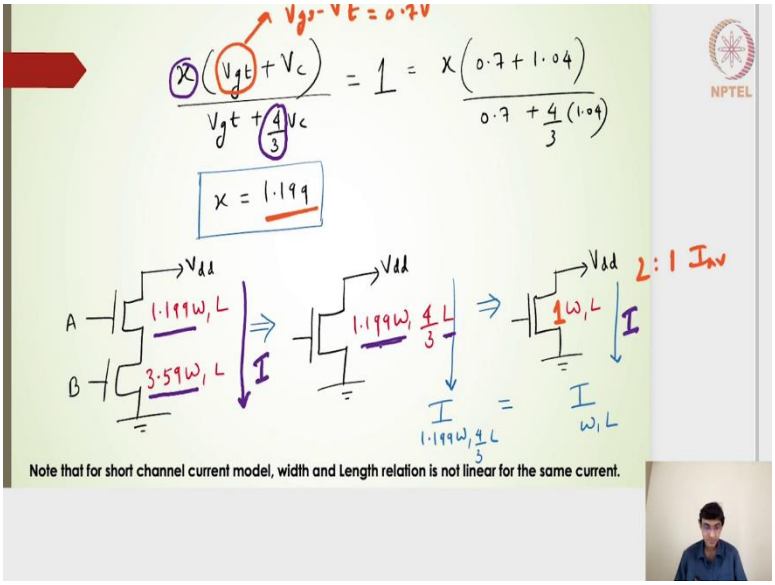

What I have done is I have made the term shorter, $V_{gs} - V_t$ which is actually nothing but 1 volts $- V_t$ we can consider that as nothing but 0.7 volts.

$$\frac{x(V_{gt} + V_c)}{V_{gt} + \frac{4}{3} V_c} = 1 = \frac{x(0.7 + 1.04)}{0.7 + \frac{4}{3}(1.04)}$$

$$x = 1.199$$

The x value turns out to be 1.199. Actually, the A transistor width should be 1.199 W and B transistor width should be 3.59 W, so that I will get the current same as that of the 1W, L.

Whatever the current the benchmark inverters 2 is to 1 inverter the falling current is there that current I will get only if I have 1.199 W and then 3.59 W, on the two transistors which are in series and especially if we are considering a 2- input NAND gate I need to have, and if I want to introduce asymmetricity in the gate widths then I need to have 1.199 W in one transistor and another transistor should have 3.59 W. This current will be same as the current which the benchmark inverter is giving alright.

This is I will call it as an I current. Note that for the short channel current model width and length relation is not as linear as that of the long channel current because of the term there is a x this represents the width. The current in the short channel is directly proportional to the scaling factor of the width.

But on the length side, there are some parameters and it may not be be inversely proportional, it may not be a linear relationship between x and then the $4/3$, the $4/3$ gets accommodated in the denominator with some kind of an expression and that is the reason why we do not have that kind of a linear relationship.

What I eventually see is, if I use a long channel current model then I can easily scale it. I can have a $4/3$ here, I can have $\frac{4}{3}$x 3 = 4 and whatever current I achieve here it will be nothing but $\frac{4}{3}$W and then $\frac{4}{3}$L.

My width and then the currents or rather width and the channel length have a very linear relationship. In the short channel I do not have that. If I consider $\frac{4}{3}$L then the width will be

1.99 and it will not be 1.33 which is $4/3$. There is a slight drop in the width, compared to the long channel current model which is used to give us $\frac{4}{3}$W, here it is 1.199.

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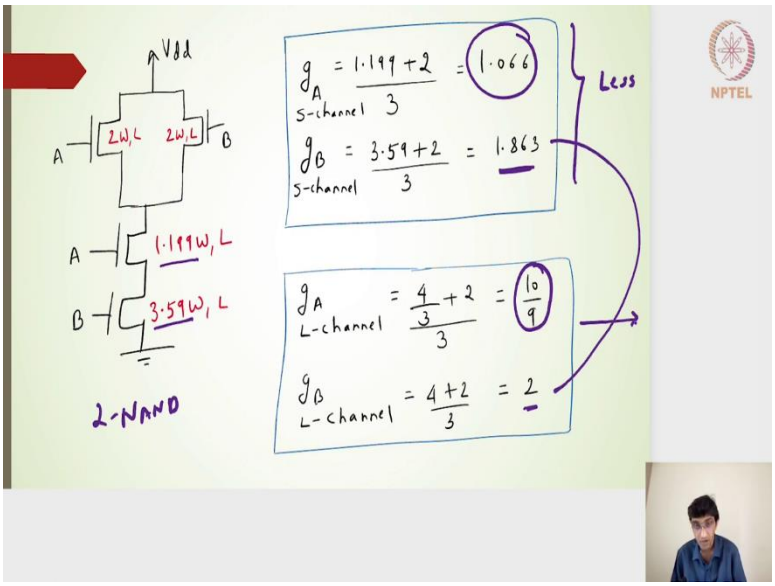

If I consider a 2-input NAND gate here. This is a 2-input NAND gate, the PMOS transistor is 2W, NMOS is 1.199 W and another transistor is 3.59 W. If I want to find out that the logical effort of the input A it will be nothing but,

$$g_{A}{}_{s-channel} = \frac{1.199 + 2}{3} = 1.066 < \frac{4}{3}$$

the logical effort of the input B it will be nothing but,

$$g_{B}{}_{s-channel} = \frac{3.59 + 2}{3} = 1.863$$

In the long channel, if I see the same parameters in the long channel it will be,

$$g_{A}{}_{L-channel} = \frac{\frac{4}{3} + 2}{3} = \frac{10}{9}$$

$$g_{B}{}_{L-channel} = \frac{4 + 2}{3} = 2$$

If I consider this comparison the short channel current model is actually giving me the logical effort less and if I consider $\frac{10}{9}$ and then 1.066 this value is slightly less. The short channel model is likely to give me the logical effort which is less and short channel current model we always say that it is more closer to the accurate results. Eventually this short channel model is going to give me whatever the parameters which we are characterizing the logical efforts or the parasitic.

It will give me a value very very close to the accurate value, so that delay evaluation will also be very very close, whereas the long channel is always a conservative approach we will always have a values which is slightly higher. Even here we are seeing the logical efforts to be slightly higher. Eventually our delay calculation using the long channel will always be slightly conservative.