Design and Analysis of VLSI Subsystems
Dr. Madhav Rao
Department of Electronics and Communication Engineering
Indian Institute of Technology, Bangalore

Lecture - 04
PMOS Transistor

The PMOS transistor in figure 4.1 shows the p+ dopants of source and drain material and n-type body. The p^+ dopant type as a slightly more current. The transistor consists of oxide layer and gate layer. This gate layer is made up of polysilicon or any metal such as aluminum. The cross-sectional structure of PMOS transistor operates the polarities in the opposite way of NMOS transistor.

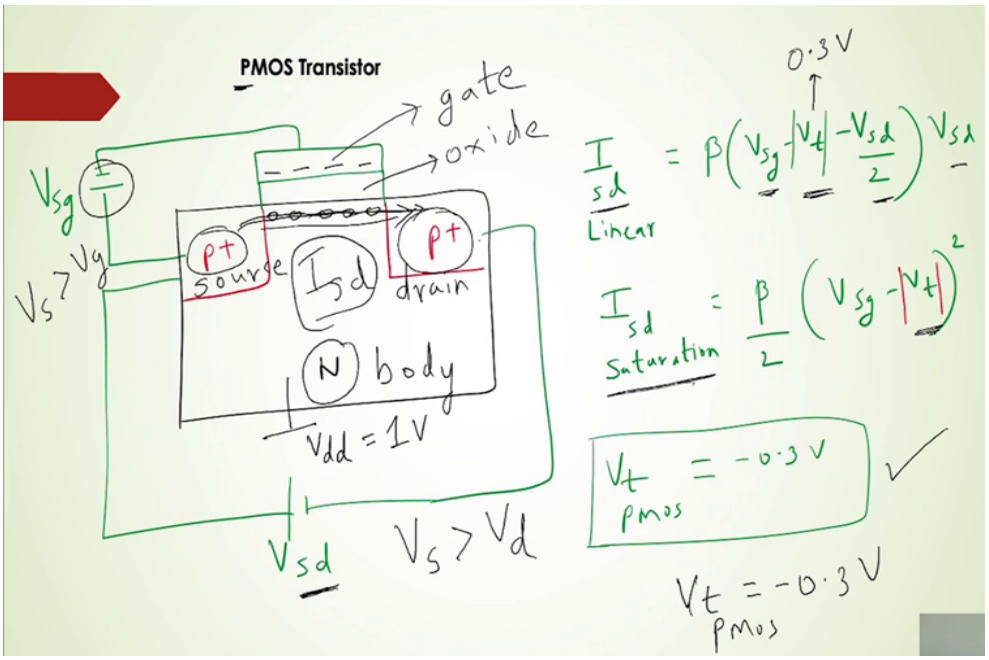

Figure 4.1: PMOS Transistor Structure

Whenever the diffusion of p^+ is observed in cross-section structure, then it is indicated as PMOS transistor. Similarly, the diffusion of n^+ is observed in cross-section structure, then it is indicated as NMOS transistor.

The majority carriers of the N-type body will be the electrons and the minority carriers are that of holes. When the gate is at a high potential, no current flows between drain and source. Thereby the source should have the higher potential with respect to gate. As the gate voltage is lowered by a threshold V_t(V_g will be negative value), holes (minority carriers) are attracted

towards the oxide interface to form a p-type channel immediately beneath the gate. Once the inversion layer or channel is formed, the holes are propagating from source to drain region and hence current I_{sd} starts flowing into the device. Also, the source is kept higher potential with respect to drain and it's represented as V_{sd}. Such that the current starts flowing from source to drain end.

When $V_{ds} > V_{gs} - |V_t|$ *or* $V_{sd} < V_{sg} - V_t$, the transistor is operating in linear region. For 65nm technology node the $V_{tpmos} = -0.3V$. The current equation for PMOS transistor is

$$I_{sd,linear} = \beta(V_{sg} - |V_t| - \frac{V_{sd}}{2})V_{sd} \tag{4.1}$$

In saturation region $V_{sd} > V_{sg} - V_t$, the channel is pinched off or at the drain point the channel is tapered. Thereby the current doesn't increase and it remains constant. The current expression is

$$I_{sd,sat} = \frac{\beta}{2}(V_{sg} - |V_t|)^2 \tag{4.2}$$

The current vs voltage characteristic of transistor is shown in figure 4.2. For NMOS transistor the representation of voltage is V_{gs} and V_{ds} and current is I_{ds}, similarly for PMOS transistor the voltage is V_{sd} and V_{sg} and current is I_{sd}. In the characteristics the plot of x-axis is V_{ds} and y axis is I_{ds}.

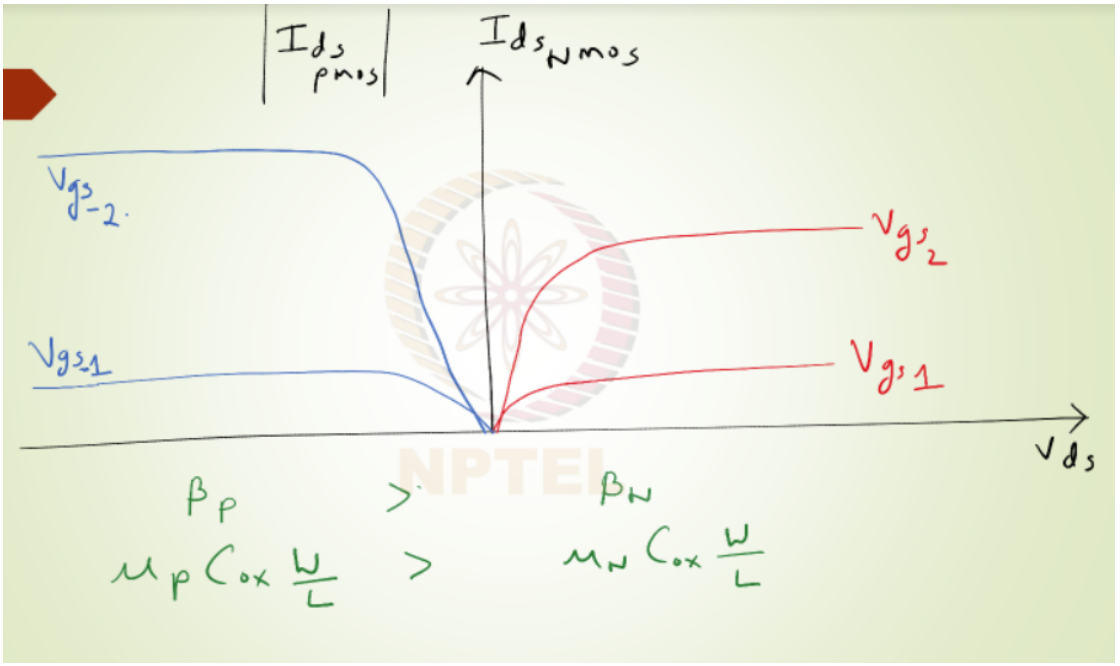

Figure 4.2: Current vs Voltage Characteristic of PMOS and NMOS Transistor

In nmos transistor, for different values of V_{gs} like 1V, 2V and V_{ds} of 0v, 0.1v and so on and for pmos transistor the vgs like -1v, -2v (or V_{sg} like 1v, 2v) and V_{sd} of 0.1v, 0.2v and son on, the current starts increasing. Thus, it indicates the linear and saturation region shown in figure 4.2.

$$\beta_p > \beta_n$$

Where,

$$\mu_p C_{ox} \frac{W_p}{L} > \mu_n C_{ox} \frac{W_n}{L}$$

When $\mu_p = \frac{\mu_n}{L}$ the mobility of holes is approximately half that of the mobility of the electrons. Thus, PMOS has higher current than NMOS. If $C_{ox} \frac{W}{L}$ dimensions of PMOS and NMOS are same, then PMOS can't provide higher current than NMOS.

In another case, when dimension of $W_p = W_n$, $L_p = L_n$, $C_{oxp} = C_{oxn}$ and $\mu_p < \mu_n$, then the saturation value will be in terms of $\frac{\beta_n}{2}(V_{gs} - V_t)^2$ and $\frac{\beta_p}{2}(V_{gs} - |V_t|)^2$ where PMOS current is exactly half of NMOS current, that is NMOS current is slightly more.

In Long channel model for 65nm technology node there is a particular process in place a fabrication process to build up this transistors and it uses the following parameters is shown in table 4.1.

Table 4.1: Long channel model for 65nm technology node

Long channel model for 65nm technology node: NMOS Transistor	**Long channel model for 65nm technology node: PMOS Transistor**
Mobility =μ $= 80cm_2/v - sec$	Mobility =μ $= 40cm_2/v - sec$
$V_t = 0.3V$	$\|V_t\| = 0.3V$
$t_{ox} = 1.05nm$	$t_{ox} = 1.05nm$
$\frac{W}{L} = \frac{4}{2}$	$\frac{W}{L} = \frac{4}{2}$
$2ƛ = 50nm$	$2ƛ = 50nm$

From the above table, the lambda $ƛ = 25nm$ is a very primitive length for 65nm technology node. Similarly, the lambda values are present for 180nm technology node and 90nm technology node. For a different process or a technology node lambda will change, but the other dimensions will remain the same. Thus, this lambda is kind of a scalable design rules, which will help in manufacturing the transistors or the overall design.