Design and Analysis of VLSI Subsystems
Dr. Madhav Rao
Department of Electronics and Communication Engineering
Indian Institute of Informational Technology, Bangalore

Lecture - 37
Optimizing the Stages for a General Circuit

Hello students, welcome to this lecture on the optimization. In this particular lecture we will see how to optimize the number of stages for a general circuit. What it really means is if I have a particular a logic synthesis circuit with me in the form of a gates and we have an output, we have a set of inputs and then we have a digital circuit which consists any kind of a gates like a NAND, NOR and OR and we have an output, but it is at a logical level and then if it is possible to add more stages in the form of the inverters at the end of the output and then take that as an output. The output coming from the inverters added inverter stages can that be considered as an output and if that is the case then whether it will further reduce the delay.

In that sense we are trying to optimize the stages, we are trying to add extra straight stages in the form of an inverter and then try to reduce the delay, that is how the overall optimizing the stages for already a generalized logical circuit. Hope that is clear, we will proceed further.

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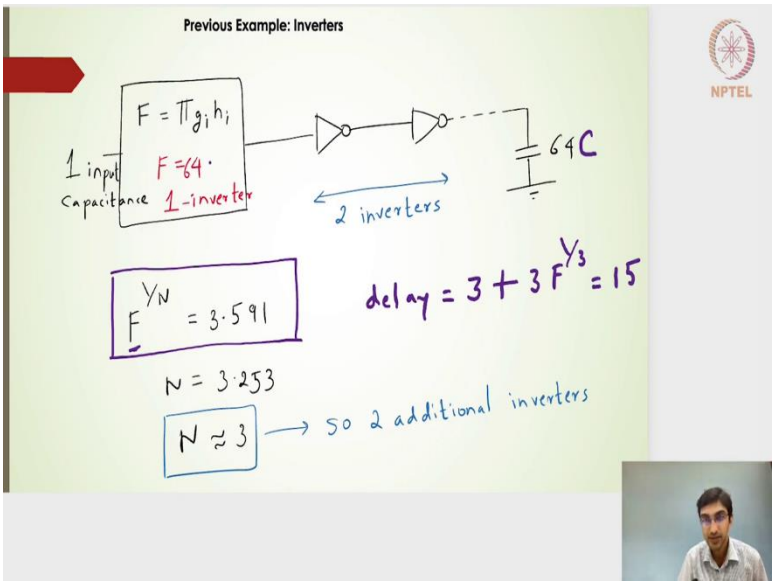

This was one of the examples which we had seen earlier, where we had 1 inverter and the 1 inverter was of a size of a 1 and it was connected to a load of 64C. Where one C is nothing but one unit NMOS parasitic or the input capacitance and that particular inverter was seeing 1 input capacitance, that is 1C.

Its 1 inverters gate size was 1 and then the load was 64C. We had seen that if we add 2 more inverters make it a 3 stage circuit then we will get the reduced delay. The optimum number of stages in this particular case was,

$$F^{1/N} = 3.591$$

$$N = 3.253$$

$$N \approx 3$$

In this particular case, the path effort is nothing but 64/1, because we are adding only the inverters, there is no logical effort or in fact the logical effort of the inverter is 1, it will not get incorporated into the F. We see the path effort as 64/1 and we have 3 number of stages.

It turns out to be 3.59 or rather we want $F^{1/N} = 3.591$ which will give me the lowest possible delay. Finally this N = 3.253 and then if I choose an N = 3, I will get some delay and if I choose an N = 4, I will get one more delay. N = 3 turns out to give us the lowest delay, that is why we had chosen 2 more additional inverters in this particular circuit. If I have N = 3 stages, the minimum delay was nothing but,

$$\text{delay} = 3 + 3F^{1/3}$$

Where F = 64.

Practically this becomes our the lowest delay possible circuit. That is what we have said that 2 additional inverters and then finally we went on to decide what should be the size of these 2 additional inverters. The size of this particular inverter was anyway is given. In that sense it should be perfectly fine.

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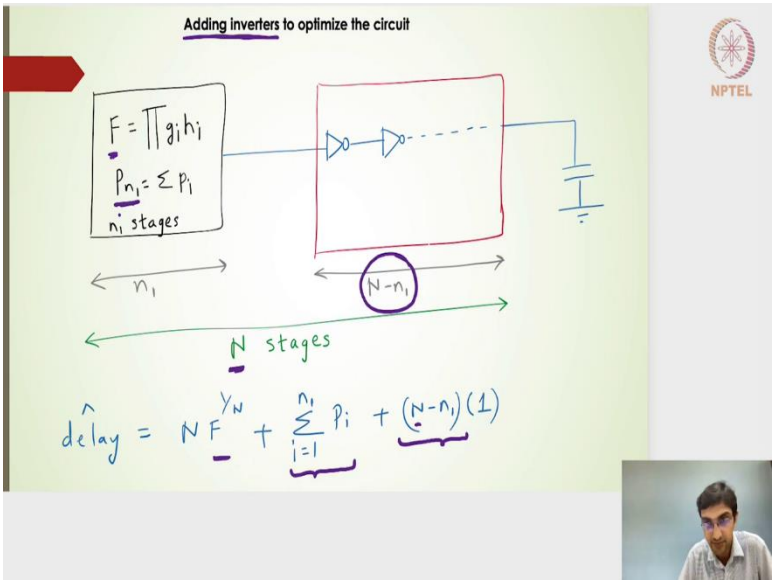

What if the first inverter which we had used in the earlier case, and let us say it is kind of loaded with some kind of a load capacitance here. If this particular first stage inverter is kind of a replaced by any other circuit. It could be a NAND gate followed by a NOR gate followed by another NAND gate and so on.

If I have a logic level gate level design here and wherein, I know that input capacitance or the input size for that particular circuit is anyways known to us and then the source the load capacitance is known to us. Can we now add multiple stages possibly resize some portion of the circuit so that I will get the minimum delay, right? What we have in this particular case is because this is now not a single inverter anymore this is now a digital logic gates. Multiple gates NAND, NOR going to another NAND or an inverter.

We have a circuit here wherein I should be able to find out what is the path effort. I have a circuit here which sees some kind of a load capacitance here. I should be able to estimate the path effort for this particular circuit which will be nothing but the product of all $g_i h_i$.

Let us say that this particular circuit is n_1 stages and we want to add few more inverters here, that will be N - n_1 inverters we are adding. So, that we get overall stages to be N, the overall N stages are designed in such a way that I will get the minimum delay.

The parasitic for this particular circuit, the already available logical the gate level circuit is $P_{n1} = \sum p_i$, which is given by this. The path effort is given that means, I know what is g_i should be able to know what is h_i for this particular part of the circuit.

If that is available, if I know what is F, if I know what is the parasitic can I add few number of inverters here so that I will get the minimum delay? With an assumption that this particular circuit is not giving me or we do not really know that whether it is giving me a minimum delay, if this particular part of the circuit is directly connected to the C_{load}, we do not really know whether it is giving me the optimum minimum delay or not.

what we are trying to do is whether we can add few more inverters N - n_1 inverters here and then make this circuit such that we will get the minimum delay. We are optimizing the number of stages here or rather we can say that we are adding the number of inverters, wherein the number of inverters will be N - n_1. Hope you know the design is clear to everyone.

If I want to find out the delay for N stages delay, for the N stages it will be nothing but,

$$\widehat{delay} = NF^{1/N} + \sum_{i=1}^{1/N} p_i + (N - n_1)(1)$$

We have this parasitic we need to find out what is the parasitic of this particular part of the circuit and then the additional inverters which we are going to add the parasitic of that as well.

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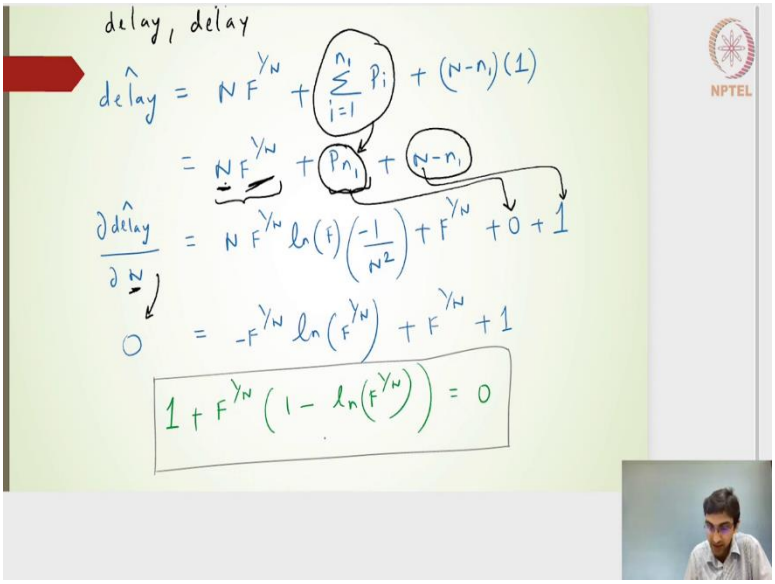

Moving forward and I have used in this particular case a $\widehat{delay}$ here which says that this is the best delay. I am just trying to use a different term. Let me rewrite it again. Delay means it may not be the best for a given number of stages it may not mean it is not necessarily the best delay, what we are saying is the $\widehat{delay}$ is our minimum delay.

From here on I am going to use $\widehat{delay}$ here which represents that for the end stages this is the minimum delay. For N stages the minimum delay is given by this particular expression,

$$\widehat{delay} = NF^{1/N} + \sum_{i=1}^{n_1} p_i + (N - n_1)(1)$$

This particular summation of p_i for n_1 stages I am going to say that this is P_{n1} and we will proceed with the same concept saying that what should be that number of N what is that optimum N so that I will get the minimum delay.

$$\widehat{delay} = NF^{1/N} + P_{n1} + (N - n_1)(1)$$

The first order differential of delay with respect to N should be 0. That is what I have stated here and then I have taken the derivative of this particular expression. Derivative of this particular expression is nothing but the partial derivatives. Consider this first and then do the derivative of this and then in the next stage we will do this particular derivative and take this as the constant value.

$$\frac{\partial \widehat{\text{delay}}}{\partial N} = NF^{1/N}\ln(F)\frac{-1}{N^2} + F^{1/N} + 0 + 1$$

$$0 = -F^{1/N}\ln\left(F^{1/N}\right) + F^{1/N} + 1$$

$$1 + F^{\frac{1}{N}}\left(1 - \ln\left(F^{\frac{1}{N}}\right)\right) = 0$$

P_{n1}, this is the parasitic of the gate level circuit which we have and this is not going to change with respect to the N variable. N variable is actually defined by the n_1 stages or rather N - n_1 stages, n1 stages is constant and then we are trying to add more number of inverters, that it becomes n. If n is a variable the number of inverter circuits that we are adding is going to vary, but n_1 stages is not going to vary at all, n_1 stages is a constant. It is a constant gate level circuit that has been given to us and then we are trying to add the number of inverters, that it reaches to the n stages. In that particular case if I have the parasitic of the n_1 which we know that if I change the gate level the parasitic does not change for any gate.

If I change the gate sizes the parasitic will not change. In that particular case the derivative of Pn_1 with respect to n is going to be 0, is what is hinted here. N - n_1, the n_1 stages it is not going to vary at all. What can vary is N with respect to the derivative of N will give us the value of 1.

This turns out to be a very similar expression to what we had earlier seen and the solution of $F^{1/N} = 3.591$, this is what I have written here.

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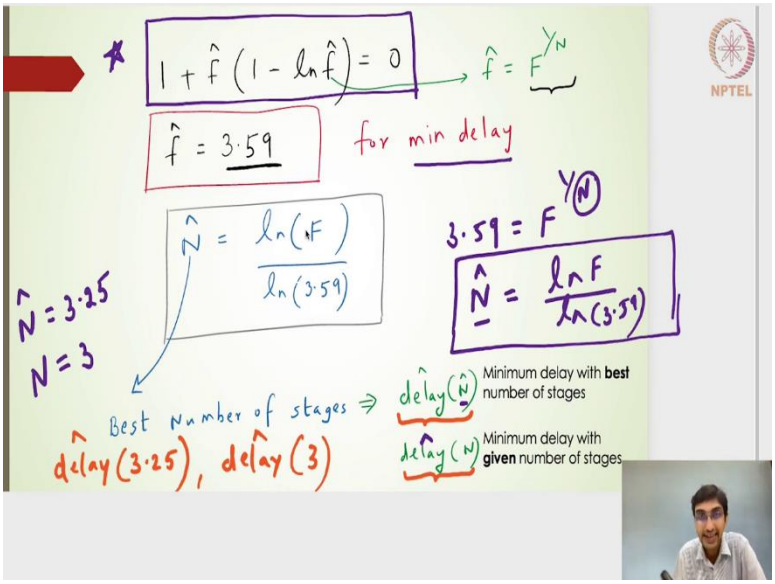

Moving forward, I have taken $F^{1/N} = \hat{f}$ which is nothing but the best stage effort we can identify for optimizing the circuit or for getting the minimum delay. $\hat{f} = 3.59$ this is what gives us the best stage effort for the minimum delay.

If I want to find out the best number of stages,

$$\hat{N} = \frac{\ln (F)}{\ln (3.59)}$$

This particular expression holds valid for any kind of a circuit. If I have the n_1 stages which could be in a combination of NAND, NOR, OR and inverter XOR anything. If I want to add more inverter, that it becomes an N stage, this particular expression is still valid.

This particular expression is still valid for not only the inverter stages, but also for a general circuit and the solution of this particular expression turns out to be 3.59. If I have 3.59 as $F^{1/N} = \hat{f}$ and if I take the log here so that I can find out what should be the best number of stages.

It turns out to be $\frac{\ln (F)}{\ln (3.59)}$, if I take the log on both the sides it will be 1/N and then N goes here log of 3.59 will come here. What I am saying is this is my $\hat{N}$ the best number of stages

that means, $\widehat{N} - n_1$ is now the best number of inverters that I can add so as to get the minimum delay. Hope this is clear to everyone.

Now, we have identified $\widehat{N}$. The best delay for the best number of stages we can identify. This will be the minimum delay with the best number of stages. We can also find out the minimum delay for any stages which is other than $\widehat{N}$. That will give me the minimum delay with the given number of stages so there needs to be little bit more explanation here.

In the previous case of an inverter which was followed by a load capacitance of 64C, we got the best stage of N as from 3.59 we got the best stage as 3.25, this is our $\widehat{N}$, but 3.25 is practically impossible, I cannot have a fractional number of stages.

We finally went into N = 3. What I am saying is with these two new variables of $\widehat{delay}$ with respect to $\widehat{N}$ it is nothing but we can consider this to be the best or the minimum delay, if we were to do 3.25 very very theoretical way of finding the best delay or the minimum delay with the best number of stages as 3.25, but it is practically impossible.

The other variable is $\widehat{delay}$ which is nothing but the minimum delay for the N value as 3, which is a practically the number of stages that is possible gate level circuit and we should be able to estimate the minimum delay for N = 3 and that turned out to be 15 value, the normalized value turned out to be 15.

This is what the $\widehat{delay}$ of $\widehat{N}$ represents, a $\widehat{delay}$ of 3.25 for our earlier example and delay cap of N represents the $\widehat{delay}(3)$ for the practically possible circuit. Hope this is clear, the $\widehat{delay}(\widehat{N})$ and $\widehat{delay}(N)$.

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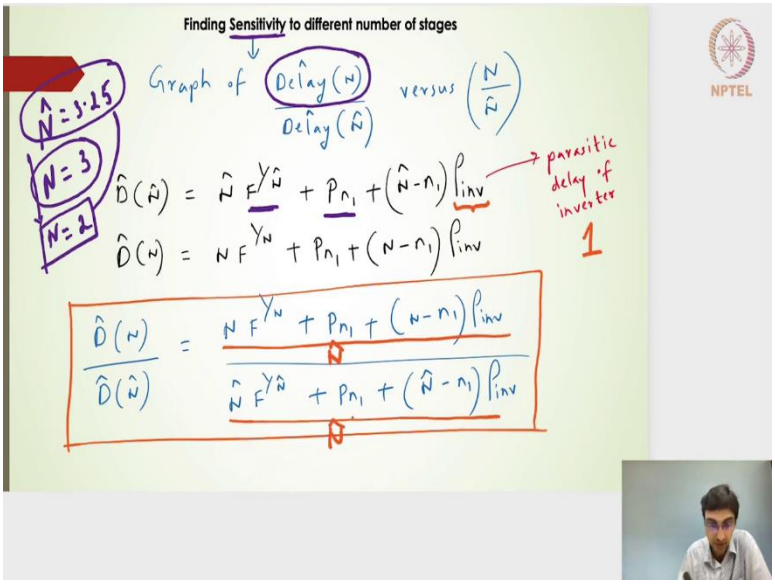

Moving further, what we need to find is the sensitivity with respect to the number of stages. What it really means is in our earlier circuit design where we had only the inverters, if I was to choose $\hat{N}$ = 3.25 what was the delay practically impossible and if I go with N = 3 what was the delay.

If I use N = 3 here my delay is going to be slightly more than 3.25. In that case if I am supposed to go beyond this lets say N = 2, what will be its outcome in terms of the delay with respect to the $\hat{N}$ = 3.25? This graph of delay cap with respect to N and of course the ratio of the delay caps for N and $\hat{N}$ versus N/$\hat{N}$.

What is this going to give me the value is the ratio of these delays represents that how far my practically possible number of stages is with respect to the best number of stages. Theoretically the best number of stages that is possible for the circuit and $\widehat{delay}(N)$ will give me how far it is with respect to the best case.

Because most of the times when we have a digital circuit because of the logical output or whatever other reasons we may not be in a position to have exactly 3.25 or whatever that value $\hat{N}$. If I go to the number of stages above how much of the deviation will I expect?

That is what this particular graph or is going to give us with respect to N/$\hat{N}$ That says that how sensitive is with respect to the number of stages. How sensitive the delay is with

respect to the number of stages and we are going to derive this expression for a general circuit.

General circuit in the sense n1 stages is made up of NAND, NOR, AND, OR, XOR whatever that gates we have with the combinational circuit gates and then we are going to add a few number of inverters so as to make it N stages. Hope you know this particular sensitivity to the different number of stages is clear.

If I want to write the expression of the best or the minimum delay with respect to the best number of stages,

$$\hat{D}(\hat{N}) = \hat{N}F^{1/\hat{N}} + P_{n1} + (\hat{N} - n_1)\rho_{inv}$$

This is something you will find it in the textbook and that is why I have put it down, but it is nothing but the parasitic of the inverter and at this particular point of time we are going to take it as the value of 1.

$$\hat{D}(N) = NF^{1/N} + P_{n1} + (\hat{N} - n_1)\rho_{inv}$$

I want to take a basically a ratio of this with respect to this. That is what I am going to write the ratio on the left hand side and then the ratio on the right hand side, finally, I will be able to get this particular expression.

$$\frac{\hat{D}(N)}{\hat{D}(\hat{N})} = \frac{NF^{1/N} + P_{n1} + (\hat{N} - n_1)\rho_{inv}}{\hat{N}F^{1/\hat{N}} + P_{n1} + (\hat{N} - n_1)\rho_{inv}}$$

What we want is the ratio of the delays with respect to N/$\hat{N}$. We will eventually divide $\hat{N}$,

$$\frac{\hat{D}(N)}{\hat{D}(\hat{N})} = \frac{\frac{NF^{1/N} + P_{n1} + (\hat{N} - n_1)\rho_{inv}}{\hat{N}}}{\frac{\hat{N}F^{1/\hat{N}} + P_{n1} + (\hat{N} - n_1)\rho_{inv}}{\hat{N}}}$$

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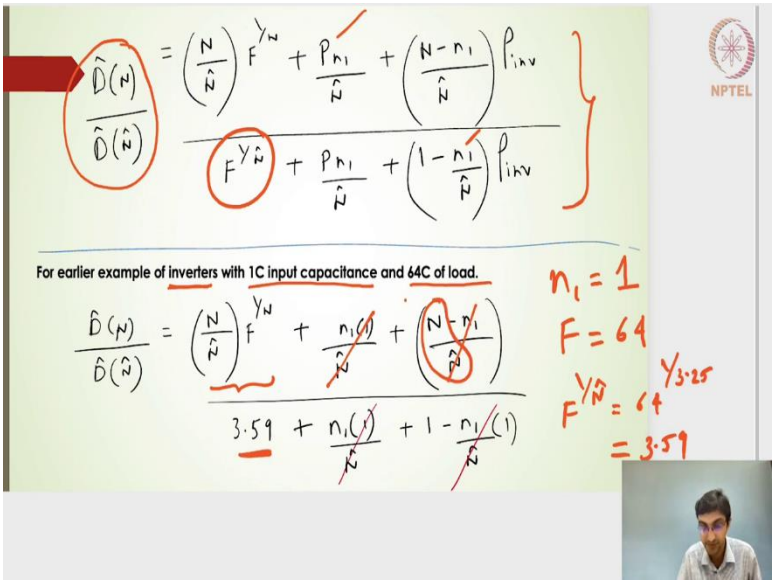

Now, I have this ratio of the delays here on the left hand side and then because I have divided the numerator and denominator with $\hat{N}$ I am going to get this kind of an expression.

$$\frac{\hat{D}(N)}{\hat{D}(\hat{N})} = \frac{\frac{N}{\hat{N}}F^{1/N} + \frac{P_{n1}}{\hat{N}} + \frac{(\hat{N}-n_1)}{\hat{N}}\rho_{inv}}{F^{1/\hat{N}} + \frac{P_{n1}}{\hat{N}} + (1-\frac{n_1}{\hat{N}})\rho_{inv}}$$

If supposed to know the P_{n1} value which we will know because if there is any kind of a general circuit and the combinational circuit we should be able to extract what is a P_{n1}.

We should be able to know this particular value also then we can plug in this particular value and then n_1 value and then we will have this ratio as a function of $\frac{N}{\hat{N}}$. I will have some kind of a function with respect to $\frac{N}{\hat{N}}$, this is our general expression. For any kind of a general circuit I should be able to get the data points of the ratio of the delays with respect to $\frac{N}{\hat{N}}$ given the P_{n1} values, given the n_1 values. This is anyways 1 unless otherwise it is specified different.

I should be able to get the data points and then I should be able to draw a graph. Now, what we will do is just for the simplification we will go ahead and say that we will take the earlier example of the inverter with 1C input capacitance and 64C of the load, that I will know what is P_{n1}.

The earlier the Pn1 will be nothing but 1 stage inverter, I will know what is N - n_1, n_1 is nothing but 1 stage and I will leave it to N - 1 here. What I am going to do is n_1 is 1 here, F = 64 because of the previous example and that is about it.

Then I am going to put that value in this particular expression and then further evaluate. What I have done here is and we know this $F^{1/\hat{N}} = 64^{1/3.25}$ = 3.59, we knew that 3.59 which was $F^{1/\hat{N}}$.

The best $\hat{N}$ was suggested was 3.25 and we were not able to take 3.25 and that is why we went with another value of N = 3. $F^{1/\hat{N}}$ which is the best number of stages will give me 3.59.

$$\frac{\hat{D}(N)}{\hat{D}(\hat{N})} = \frac{\frac{N}{\hat{N}}F^{1/N} + \frac{n_1(1)}{\hat{N}} + \frac{(N-n_1)}{\hat{N}}}{3.59 + \frac{n_1(1)}{\hat{N}} + (1-\frac{n_1}{\hat{N}})(1)}$$

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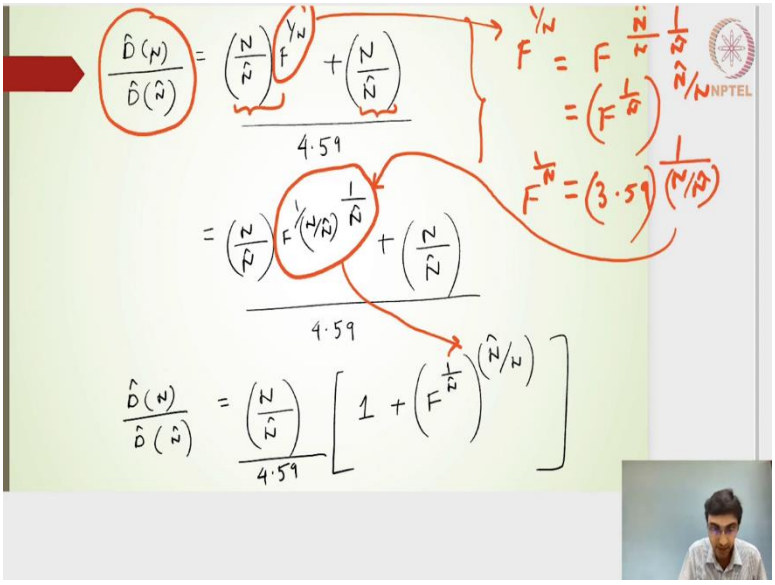

Moving forward, this is what I have.

$$\frac{\hat{D}(N)}{\hat{D}(\hat{N})} = \frac{\frac{N}{\hat{N}}F^{1/N} + \frac{N}{\hat{N}}}{4.59}$$

Now, what we are doing is we want to take this ratio or we want to plot this particular ratio with respect to $\frac{N}{\hat{N}}$. Somewhere here this particular term I need to create $\frac{N}{\hat{N}}$, F in the form of $\frac{N}{\hat{N}}$ because this particular term is in the form of $\frac{N}{\hat{N}}$ and this particular term is in the form of $\frac{N}{\hat{N}}$. If I take this separately,

$$F^{1/N} = F^{\frac{\hat{N}}{N}1/\hat{N}} = F^{1/\hat{N}}$$

$$F^{1/N} = (F^{1/\hat{N}})^{\hat{N}/N} = 3.59^{1/\frac{N}{\hat{N}}}$$

Substitute this particular expression, we get

$$\frac{\hat{D}(N)}{\hat{D}(\hat{N})} = \frac{\frac{N}{\hat{N}}F^{1/(N/\hat{N})^{1/\hat{N}}} + \frac{N}{\hat{N}}}{4.59}$$

$$\frac{\hat{D}(N)}{\hat{D}(\hat{N})} = \frac{\frac{N}{\hat{N}}}{4.59}\left[1 + (F^{1/\hat{N}})^{\hat{N}/N}\right]$$

Hope this is clear to everyone.

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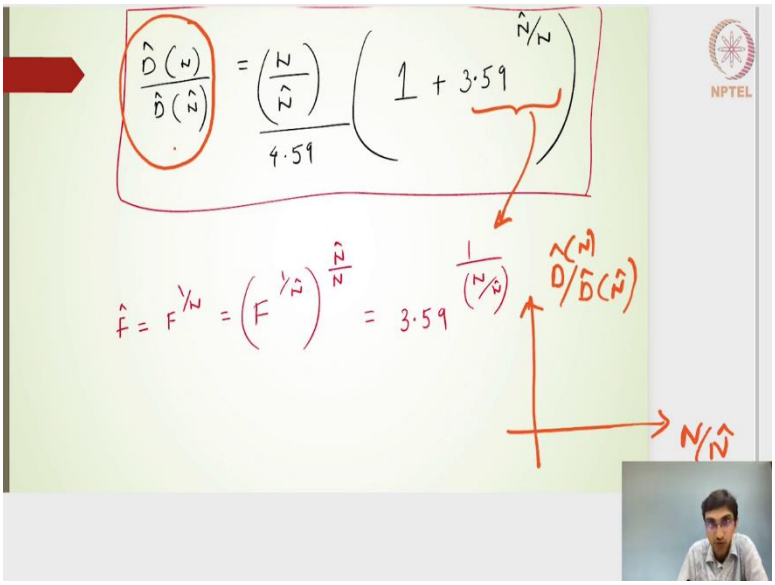

$$\frac{\hat{D}(N)}{\hat{D}(\hat{N})} = \frac{\frac{N}{\hat{N}}}{4.59}\left[1 + 3.59^{\hat{N}/N}\right]$$

$$\hat{f} = F^{1/N} = \left(F^{1/\hat{N}}\right)^{\hat{N}/N} 3.59^{1/(\frac{N}{\hat{N}})}$$

This is for an example of an inverter where we had n_1 stages was almost equal to 1 inverter and followed by the number of inverters that we need to add so that we will get the minimum delay.

If I want to draw this particular expression, draw or plot this particular expression for the ratio of the delays with respect to $\frac{N}{\hat{N}}$, I am going to have on the x axis $\frac{N}{\hat{N}}$ and on the y axis I will have the ratio of the delays, this is what I want. I will keep putting the values of $\frac{N}{\hat{N}}$ as 0.25, 0.1, 0.5, 1, 1.5, 2, 2.5, 3 and so on and then I will get the respective ratio of the delay ratio values and then I should be able to plot it out, this is what is expected.

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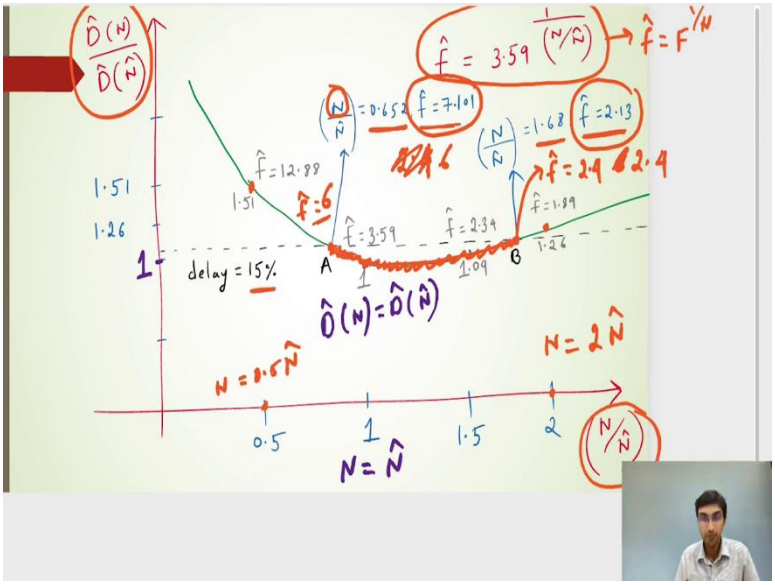

From that particular expression what we are doing in this particular graph is taking the ratio of the delays here on the y axis and on the x axis we have the ratio of the stages. This implies that if I have $N = \hat{N}$, the number of stages turns out to be the best number of stages which we have evaluated theoretically if that is possible then we will get the minimum delay.

The minimum delay turns out to be the ratio of the delays here is nothing but 1 which represents that the $\widehat{D}(N) = \widehat{D}(\widehat{N})$ because the $N = \widehat{N}$. This will be the best delay we can achieve for a given circuit if $N = \widehat{N}$.

Now, if I were to choose $\widehat{N}$ or rather N=0.5$\widehat{N}$ and I were to choose $N = 2\widehat{N}$. In that particular case I know for this particular case the ratio is given as 1.51 that means, the delay of N stages is going to be 51 percent more than the best delay that was possible. Here if I were to choose N is equal to 2 double the number of stages the delay here turned out to be 1.26, 26 percent more than we were getting for the best number of stages, hope these two points are clear. If I were to choose 0.5 and or the value of 2 here for the ratios of the number of stages that means, the number of stages is 0.5$\widehat{N}$ or double $\widehat{N}$ then the delay was going 51 percent and 26 percent above the minimum delay. Hope those two points are clear.

What should be our tolerance range because let us say the value of 1 having a value of 1 always is practically not possible. What should be our accepted tolerance level so that we will get a minimum delay which is maybe 10 percent or 15 percent or 20 percent above the minimum delay.

In that case I have drawn a line here the dotted line here, which represents that the acceptable delay level is 15 percent. If you are not able to achieve the minimum delay a 15 percent higher than the minimum delay is kind of reasonably acceptable for designing our circuits.

I have drawn this particular dash line. This dash line is actually intersecting this particular profile at points A and at point B. Point A if I were to choose the delay is 15 percent more than that means, that the ratio of the delays is 1.15.

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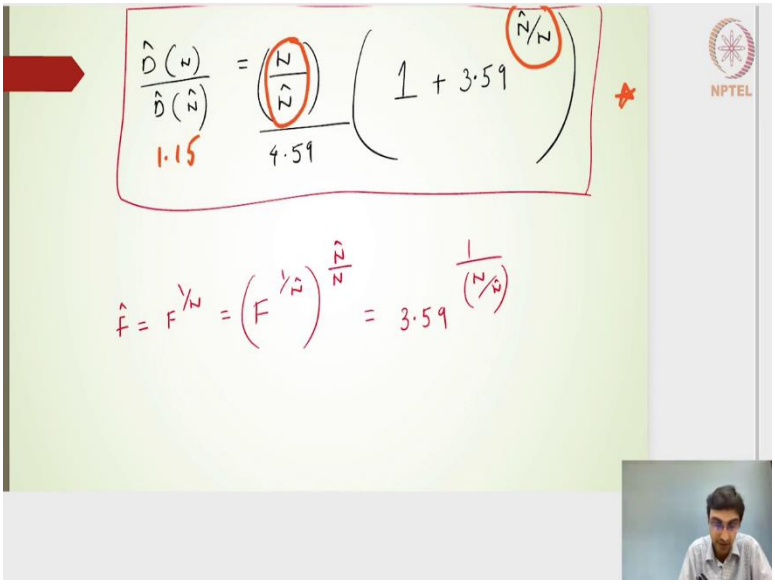

If I put it back in this particular equation if it is 1.15 here I should be able to evaluate what should be $N/\hat{N}$ heuristically. I will keep plugging the values of $N/\hat{N}$ until it satisfies 1.15. If I go back $\frac{N}{\hat{N}} = 0.652$ and similarly for point B, which is intersecting with this delay 15 percent line I will get this $\frac{N}{\hat{N}} = 1.68$.

For 0.652 I want to know if N is 0.652 times $\hat{N}$ what is my $\hat{f}$ the stage effort and similarly if $N = 1.68\hat{N}$ what should be my individual stage effort which is $\hat{f}$. Turns out that I can find it out from here, $\hat{f} = 3.59^{1/(\frac{N}{\hat{N}})}$ and this we have achieved because we know that $\hat{f} = F^{1/N}$.

If I go back to the previous slide $F^{1/N}$ can also be rewritten as multiply and divide by $\hat{N}$ on the exponent side I should be able to get $3.59^{(\frac{N}{\hat{N}})}$. I am going back to the present slide. $3.59^{1/(\frac{N}{\hat{N}})}$ this is something we have as 0.652 or 1.68 I can easily plug in here and find out what is the best stage effort. The best stage effort for the 15 acceptable delay line above the minimum delay turns out to be 7.101 or 2.13.

This particular stage effort is acceptable what we are saying for the inverters circuit. If we have an n_1 stages made up of inverters then this is what is acceptable. Generally, what happens in any other combinational circuits if I have n_1 stages which is made up of combinational circuits and then we are going to add the inverters? What happens is this $\hat{f}$ stages we can accept it from 2.4 to the 6th value.

If I were to draw this particular ratio of the delays with respect to the ratio of the $N/\hat{N}$ I will get a profile. I will draw the 15 percent delay line. This point A and B generally turns out to be, rather I should write it as instead this is 6 and this is 2.4.

If I were to draw the 15 percent delay line, the intersection point for A turns out to be close to 6, the $\hat{f} = 6$ and the intersection point the B which will give me the $\hat{f} = 2.4$. Generally for designing the digital circuits we will consider the $\hat{f}$ of 2.4 to 6. 3.59 turns out to be the best one. If it is possible to achieve that we will definitely go with $\hat{f} = 3.59$ because it is going to give me the lowest or the minimum delay that is possible.

But if it is not practically possible we will try to achieve any points between this particular range of A to B, which is nothing but giving an $\hat{f} = 2.4$ to an $\hat{F} = 6$ which will determine the number of stages here and so on. Once we have the number of stages we can find out what is $\hat{f}$, from the $\hat{f}$ we can find out what is the gate sizes that is required, we will try to limit our designing in this particular range from A to B. Hope this is clear.