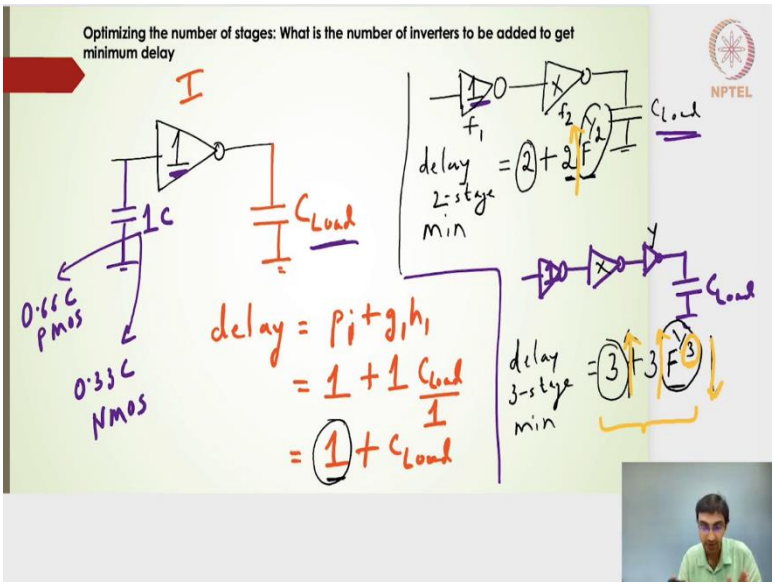
Design and Analysis of VLSI Subsystems
Dr. Madhav Rao
Department of Electronics and Communication Engineering
Indian Institute of Informational Technology, Bangalore

Lecture - 36
Optimizing the Stages for an inverter path

(Refer Slide Time: 00:16)



Hello students, welcome to this lecture on trying to learn how to optimize the number of stages for a given circuit, so that we get the minimum delay. Let us begin with one inverter here, the inverter has an input size, let me take input size of 1. What it means is at the input of this particular inverter it sees a capacitance of 1C including both the PMOS and then the NMOS transistors.

Ideally, it is quite not possible to have the PMOS as 0.66C for the PMOS, 2/3 parts will go to the PMOS and then 1/3 parts will go to the NMOS, 0.33C for the NMOS. It is not quite possible, but just for our theoretical understanding we will take a gate size of 1 for this inverter and let us say that this sees a load capacitance, some kind of a load capacitance. The minimum delay for 1-stage will be nothing but,

$$\text{delay} = p_i + g_i h_i$$

$$\text{delay} = p_1 + g_1 h_1$$

$$\text{delay} = 1 + 1\frac{C_{load}}{1}$$

$$\text{delay} = 1 + C_{load}$$

The delay will always be $1 + C_{load}$. Now, let us take another example of having two sizes or two inverters. The 1st stage is 1, the 2nd stage let us say it is X and then there we have the C_{load} here. Now, the delay for 2-stages and I am talking about the minimum delay.

$$\underset{\text{min}}{\text{delay}_{2-\text{stage}}} = 2 + 2F^{1/2}$$

What I mean is each of these stages f_1 and then the f_2 which is nothing but the stage efforts, it sees an equal stage efforts. That is the reason why I have taken twice into the same stage effort which will be $F^{1/2}$.

Now, let us say I have three inverters. In this particular 3rd case I have now three inverters and then I have the C_{load}. I am talking about the same C_{load} everywhere, same $C_{load}$and I am talking about the same you know the 1st stage having the same gate size.

Here also it is 1 and let us say the size is X now, the size is Y now for the 2nd and 3rd stage respectively. Now, the delay for the 3 stage and the minimum delay is nothing but the parasitic has increased now to 3 instead of 2 or instead of 1 in the earlier case,

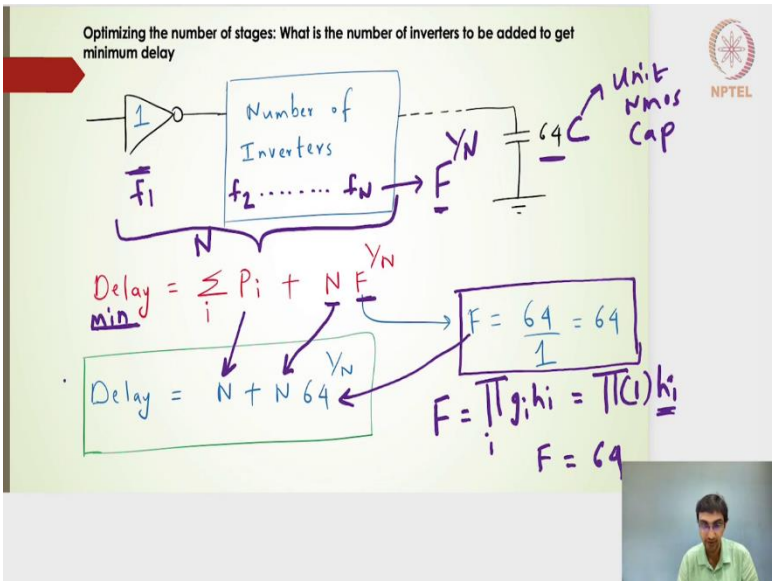
$$\underset{\text{min}}{\text{delay}_{3-\text{stage}}} = 3 + 3F^{1/3}$$

If I get started the parasitic of 1 for 1-stage, the parasitic of 2 for the 2nd stage, the parasitic for the 3 for the 3rd stage is increasing, the parasitic value is increasing, but if I consider this $F^{1/2}$ and $F^{1/3}$. This particular value and then the F value is nothing but the product of all $g_i h_i$ turns out to be $\frac{C_{load}}{1}$.

This $F^{1/2}$, $F^{1/3}$, this particular value has decreased but the number of stages this is going to increase. I am going to use a different pointer so that it becomes very clear for you to see, 2 has increased, 3 has increased you know from 2 to 3 it has increased, but the $F^{1/2}$ and then $F^{1/3}$ it has decreased and the parasitic has increased, starting from the 1st stage, 2nd stage, and 3rd stage.

There clearly is some minimum point in the delay for the number of stages here. It is not necessary that if I keep on adding the inverters, the delay is going to increase, because of this $F^{1/n}$ factor there may be the number of stages, there may be an optimum number of stages where the delay will be less. Hope you know the number of stages does not necessarily cause in the delay, hope that is clear.

(Refer Slide Time: 06:39)



Let us take an example here, we need to optimize the number of stages and what should be the number of inverters to be added to get the minimum delay, the 1st stage is anyways 1. The same example what we had seen in the earlier slide and then we have the 64, what it means is it is actually 64C, where 1C represents the unit NMOS transistors capacitance.

This parasitic capacitance or the input capacitance all are considered to be 1C. A width of 100nm, C is considered as having a 1C capacitance. How many number of inverters I need to add here? Then once we add the number of inverters, once we identify the number of inverters that needs to be added here so that I will get the minimum delay and then we will try to identify what should be its gate size.

If I want to find out the minimum delay,

$$\text{delay}_{\text{min}} = \sum p_i + NF^{1/N}$$

If I add two inverters or three inverters of n number of inverters here in this particular block, then this parasitic will be nothing but N+1 because 1 is the 1st stage inverter.

Considering this to be an N stage inverter, the parasitic will be nothing but N and this one is nothing but each of these stages will see the stage effort of f_1, f_2, f_3, f_4 up till f_N and each one of this stage effort should be equal. I am going to do N into the individual f's.

The individual f's could be f_1 or f_2 or f_N which is equal to nothing but the total path effort $F^{1/N}$. If all the number of stages is N then I will be able to find out the path effort and then 1/nth root of that path effort will give me the individual stage efforts, the individual best stage efforts and that is what I am going to put it here for finding out the minimum delay, that is what we get here. The individual best stage efforts which is arriving from the path effort.

If I want to calculate the path effort which is nothing but,

$$F = \prod g_i h_i$$

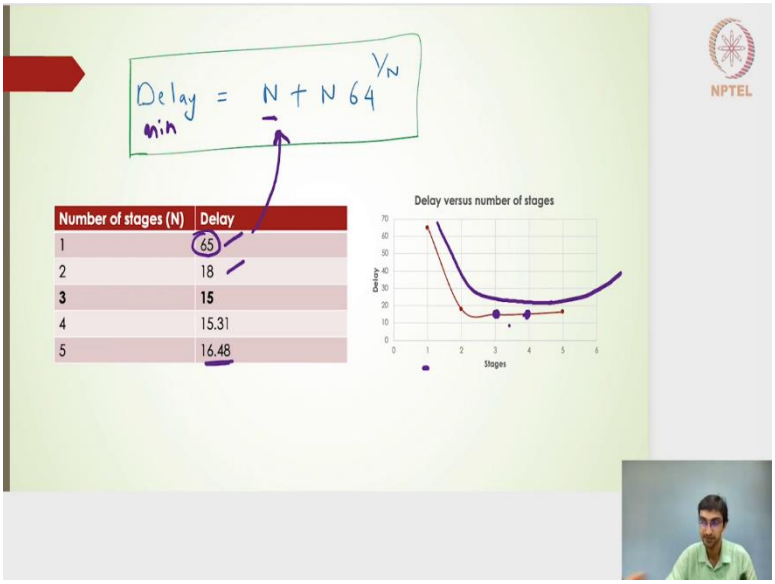
g_i for the inverter is always 1. It is always 1 here g_i and then the g_i. If I have a lot of inverters here of the different sizes x, y and z, all those x, y and z in this particular h and the product of h_i will get cancelled and what remains is,

$$F = \frac{64}{1} = 64$$

$$\text{Delay} = N + N64^{1/N}$$

Hope this expression is clear to everyone, moving forward.

(Refer Slide Time: 09:57)



Now, I have the minimum delay expression with the number of stages and if I put a table here, if N = 1, what is the delay if N = 2? What is the delay if N = 3? What is the delay? and so on.

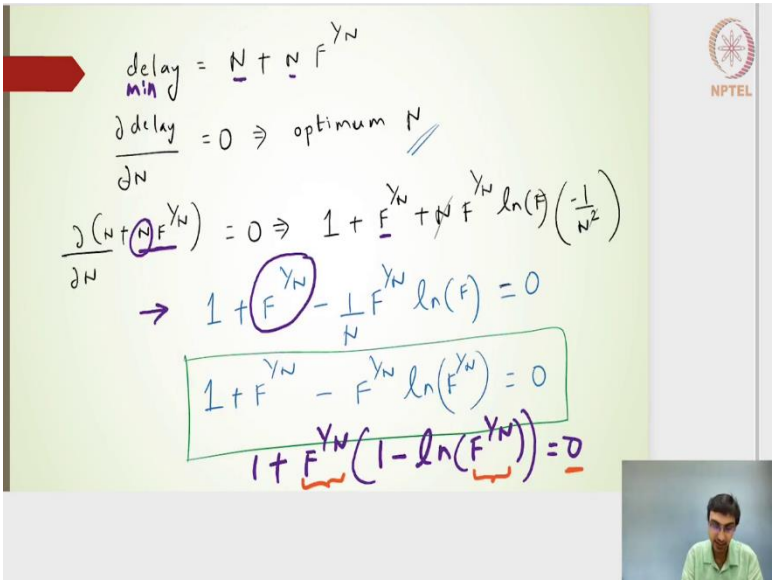
Turns out that for N = 1 it is 65, for N = 2 it is 18 and this values are taken clearly from this particular expression and if N = 3, the minimum delay turns out to be 15, which is very very less compared to 65. If N = 4, I will get 15.31, if N = 5, I will get 16.48 and then so on.

If I draw this particular graph of delay versus number of stages what we are seeing is, starting from the 1 stage moving towards the higher number of stages somewhere and the 3 value or between 3 and 4 value it is going to reach the minimum delay and then it starts from a higher value goes to the minimum value and then it starts increasing.

Although I have not represented, I have not got the data points for the higher number of stages, but it is likely to increase the delay, if it is beyond the 4 stages it is likely to increase. We get an optimum point somewhere between 3 and 4 which will give me the minimum delay.

Similar how we identify the optimum X and Y value, optimum gate sizes the number of stages could also be optimized to get or to achieve the minimum delay, hope this is clear.

(Refer Slide Time: 11:52)



We have an expression for the minimum delay with respect to the N value, where N is the number of stages. If I want to find out the minimum delay

$$\frac{\partial \text{delay}}{\partial N} = 0$$

So that I will get the optimum N value. If I do the differentiation of this,

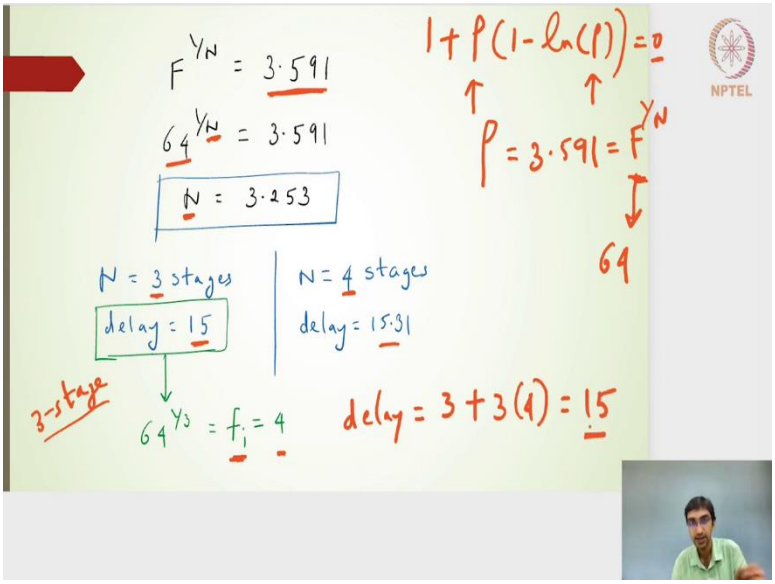
$$\frac{\partial(N + NF^{\frac{1}{N}})}{\partial N} = 0 \Rightarrow 1 + F^{\frac{1}{N}} + NF^{\frac{1}{N}} \ln(F) \frac{-1}{N^2}$$

$$1 + F^{\frac{1}{N}} - \frac{1}{N} F^{\frac{1}{N}} \ln(F) = 0$$

$$1 + F^{\frac{1}{N}} - F^{\frac{1}{N}} \ln\left(F^{\frac{1}{N}}\right) = 0$$

I can find a solution of $F^{\frac{1}{N}}$ by a heuristic method. Heuristic method means if I keep on plugging the values for this $F^{\frac{1}{N}}$ and then I should be able to find a closer value which is going to give me for this particular expression it is going to give me 0.

(Refer Slide Time: 13:58)



What I am going to do is from this particular expression $1 + F^{\frac{1}{N}}$, I am going to write it as,

$$1 + \rho(1 - \ln(\rho)) = 0$$

I am going to keep putting the values of a ρ starting from let us say 0 or 1 or 2 or 3 or 4, and somewhere between 3 and 4 I should be able to find, somewhere between 3 and 4 I should be able to find I know it is the expression is going to result into a 0 value. Keep on putting the values between 3 and 4, I should be able to find $F^{\frac{1}{N}}$ or ρ value turning out to be,

$$\rho = 3.591 = F^{\frac{1}{N}}$$

If that is the value, what is the F value, F is equal to nothing but 64, f we had calculated earlier was 64,

$$64^{\frac{1}{N}} = 3.591$$

$$N = 3.253$$

The optimum number of stages is 3.253, theoretically it is 3.253, but when you are putting the number of stages or number of inverters it either has to be an integer value, it either has to be a 3 value or a 4 value, it cannot be 3.253 stages.

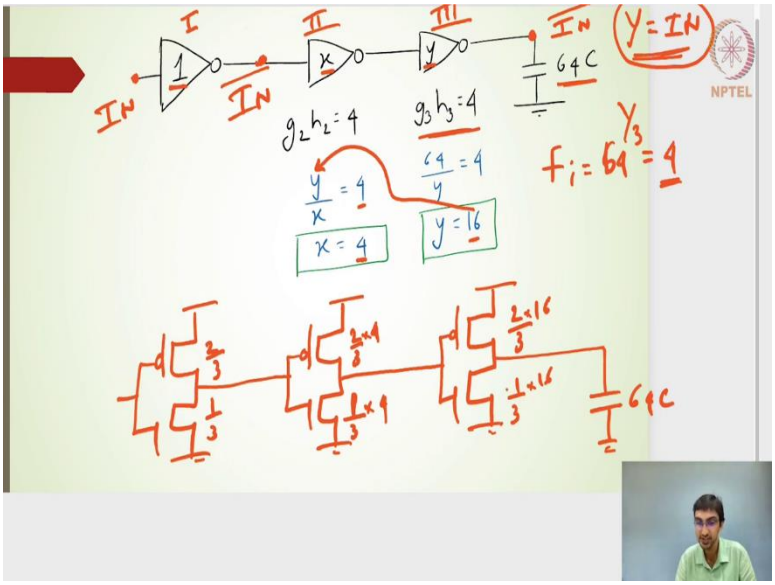
We calculate what is the delay if I have 3 stages and what is the delay on the other side if I have 4 stages, turns out that the delay for the 3 stages is lower than the delay for the 4 stages. We will use the 3 stage inverters so as to achieve the minimum delay,

$$64^{\frac{1}{3}} = f_i = 4$$

The overall delay will be nothing but the 3 stage parasitic,

$$\text{delay} = 3 + 3\left(64^{\frac{1}{3}}\right) = 3 + 3(4) = 15$$

(Refer Slide Time: 16:32)



Finally, this is what the circuit will look like. I have the 1st stage, I have the 2nd stage, I have the 3rd stage, 3 stage circuit is going to give me a minimum delay of 15 and minimum normalized delay of 15 for a load capacitance of 64C and then the input gate size of 1. If I want to find out what is the gate size of x and y here, I know the fi value here is nothing but $64^{\frac{1}{3}}$ turns out which is nothing but 4 here.

The individual g_ih_i if I can equate it to 4 I should be able to find out the gate size as y and x. If I do g_3h_3 = 4 I should be able to find out what its y, because g_3 for this particular 3rd stage is 1, h_3 is nothing but 64/y which is y = 16. Similarly, if I do for the 2nd stage g_ih_i = 4, I should be able to find out for the 2nd stage $g_i = 1$, h2 is nothing but y/x which will be 4 and x will be the value of 4, y is taken considering once we find out the 16 value as y

we can put it here and then find out the x as nothing but 4. My transistor sizing for this particular inverter will be nothing but $\frac{2}{3}$x16.

Then $\frac{1}{3}$x16 and similarly here the transistor sizing for the 2nd stage inverter is nothing but $\frac{2}{3}$x4 and $\frac{1}{3}$x4, this is how my circuit will look like. Where the output is 64C and at the input side, I have the inverter which is having $\frac{2}{3}$ and then $\frac{1}{3}$, this gets connected to the input here.

This is my gate level circuit and then this is my transistor level circuit design with the widths of the transistor mentioned which is going to give me a minimum delay. One more point to note here is I have used 3 number of stages, in this case my input and then my output here will be inverted.

My output here because it is 3 stage, the output here will be nothing but inverted input, but if there is a specification that we need to get not an inverted output. In that case if Y has to be same as that of the input in that case I will choose even number of stages.

In that case N = 3 may not be an appropriate design because my output will be violated, because the output is nothing but a complement of the input what we are getting. But if my output needs to be equal to that of the logical expression need not to be a complement expression. Then in that case I will try to choose the even number of inverters and it turns out that N = 2 and N = 4, I will choose N = 4 because the delay of N = 4 turns out to be very close to the minimum delay.

In that case I will choose N = 4 and recalculate the sizes of x, y and maybe the z because that will be the 4th inverter and then redefine or re-evaluate the widths of these individual transistors.