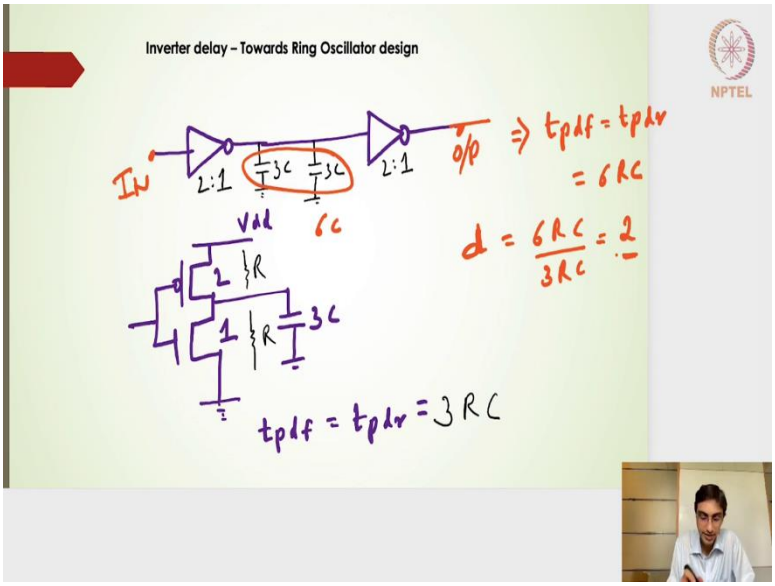
**Design and Analysis of VLSI Subsystems**
**Dr. Madhav Rao**
**Department of Electronics and Communication Engineering**
**Indian Institute of Informational Technology, Bangalore**

**Lecture - 33**
**Ring Oscillator design**

(Refer Slide Time: 00:16)




Hello students, welcome to this lecture on estimating the Ring Oscillator Design and its frequency. The ring oscillator circuit is very important in measuring not only the fabrication process, whether it has worked well for a particular technology node as well as it can provide a clock frequency on its own. Let us have a look at the design first and then we will try to understand why it is so important for verifying the manufacturing process.

Let me try to draw this inverter first and then through the inverter the ring oscillator will be designed. Let me take up a single inverter. If I take up a single inverter and let me draw the gate level circuit that it becomes much easier for us to estimate what should be the delay. This is the input the PMOS and NMOS transistor tied together giving an input.

The parasitic capacitance here will be nothing but 3C, assuming it will be a unit inverter having a size of 2:1, that is 1 for the unit NMOS transistor and the size of 2 for the PMOS transistor. Overall, I will get a 3C capacitance. The overall delay,

$$t_{pdf} = t_{pdr} = 3RC$$

It will be nothing but 3RC. Let me use this 2:1 inverter and then try to connect one more 2:1 inverter. If I use one more 2:1 inverter what we are seeing is its own parasitic will be of 3C capacitance and at the input side this particular second stage inverter is going to give me one more 3C capacitance at the input side.

Overall put together this will be nothing but 6C capacitance. Now, the overall delay for the two inverters which are there from input side to the output side. I am going to write it like this, O/P is the output one. I will get a propagation delay of

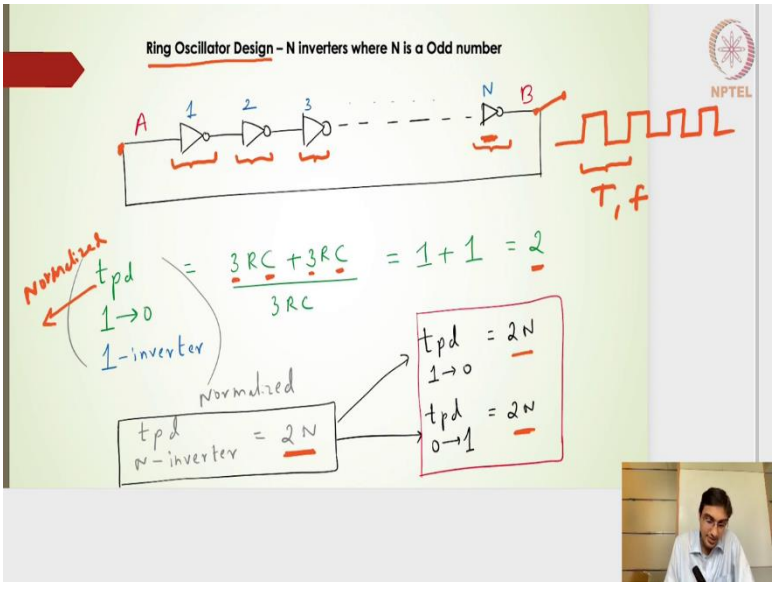
$$t_{pdf} = t_{pdr} = 6RC$$

If I try to normalize this, the delay normalize will be nothing but,

$$d = \frac{6RC}{3RC} = 2$$

Now, the question is what if I connect one more inverter here and so on. If I do N such cascaded inverters, I will actually get the overall delay as 2N.

(Refer Slide Time: 03:45)




Moving forward the ring oscillator is actually designed by the cascaded inverters design and the output of N such inverter, the output of the Nth inverter is fed back as an input to the first inverter. That is how we will get the output of this which is nothing but the input of this. If I probe at any point A and B that will give me some kind of a signal which is

nothing but we call it as an oscillating signal. It will oscillate from 0 to 1 and it will be a self sustained oscillating signal, this could be considered as a clock signal also. Now, let us see why we are getting this kind of a clock signal and which periodically repeats. There is a time period and then there is an associated or characterized frequency with this particular ring oscillator output signal. If I consider the first inverter here, the 1 represents the first inverter, 2 represents the second inverter, 3 represents the third and then the N represents the N inverter.

If I consider the first inverter and if I provide a high signal here. If I take out this particular inverter which is cascaded to the next stage. If I want to find out what is the delay of this, I will provide an input signal here high input and then I will measure what is the output here. It will be a low output, but how much time it takes? from 1 to 0 for the first inverter it will take 3RC, 3C coming from its own parasitic capacitance. The next 3RC, where the 3C is coming from the input of the input capacitance of the second stage,

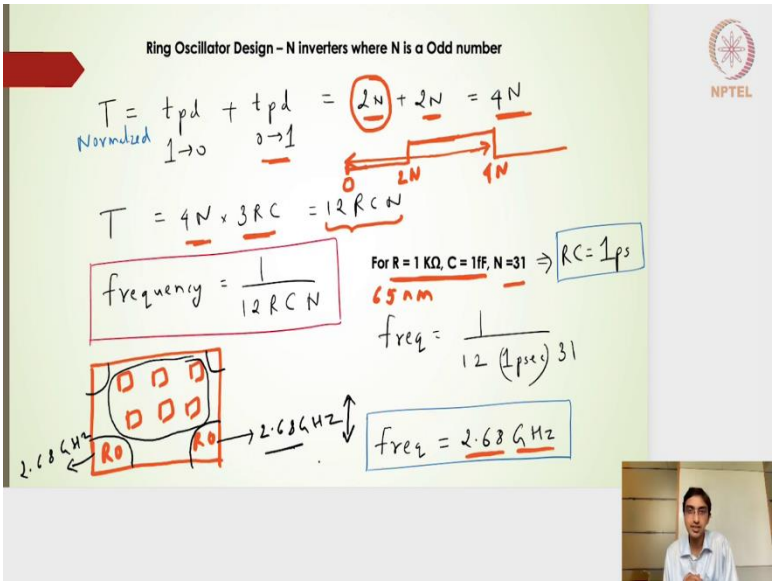
$$t_{\substack{pd \\ 1\rightarrow 0 \\ 1-\text{inverter}}} = \frac{3RC + 3RC}{3RC} = 1 + 1 = 2$$

If I have N such inverters, the delay from point A, the input to the point B, which is the output will be nothing but,

$$t_{\substack{pd \\ N-\text{inverter}}} = 2N$$

The normalized delay for the N inverters, this is a normalized value, what I have calculated here, the absolute value will always be multiplied by 3RC. The normalized value of the N inverter will be nothing but 2N and I have written it as the falling delay and then the rising delay turns out to be 2N and 2N. Note that the B output of this is also connected to the input of 1. Even if I am trying to consider what should be the delay of this Nth inverter it will be nothing but the 3RC coming from its own parasitic capacitance as well as the input capacitance of the first inverter and that is why we have a 6RC, here as well for the Nth inverter divided by 3RC will be nothing but 2. That is why for the N such inverters I will get 2N, hope that is clear.

(Refer Slide Time: 06:46)




What we are seeing is for 1 to 0, we have 2N delay and then for 0 to 1 we have 2N delays. If I take odd number of inverters, if the input is 0 after 2N delay I will get the high output which is fed back to the input. After 2N delay this is the time T is equal to 0 and after 2N delay I will get the high output which is nothing but the input again and then after 2N delay I will actually get the low output.

$$T_{Normalized} = t_{\substack{pd \\ 1\to0}} + t_{\substack{pd \\ 0\to1}} = 2N + 2N = 4N$$

The time period overall from 0 to getting the next cycle will be from 0 to 4N. The overall time period will be,

$$T = 4N \times 3RC = 12RCN$$

The frequency here will be nothing but,

$$\text{Frequency} = \frac{1}{12RCN}$$

If R and C if it is 1ps, 1fF and 1KΩ or you can consider 10KΩ and then 0.1fF and if I put an N value of 31 here. The overall time period will be nothing but,

$$\text{freq} = \frac{1}{12(1\text{psec})31}$$

$$\text{freq} = 2.68\text{GHz}$$

Now, this is a very important parameter because this RNC value I have considered it for 65 nanometer technology node and this becomes a very important parameter because when we are developing a chip I have lot of area covered for other circuits.

There are lot of circuits here and then there are lot of interconnects connecting to the circuit. Somewhere at the corners we will have the ring oscillator design and while we fabricated, while the everything is done. Once we get the chip out of it, we should be able to test out the frequency of this ring oscillator.

For a 65nm technology node if it gives a frequency of 2.68 gigahertz that represents even the corners while it is fabricating, even the corners are giving a frequency of 2.68, that means the fabrication process has been done perfectly. There is no problem in the fabrication. Generally, the fabrication process is such a way that in the middle region there will not be any problems, the problems arises only when the circuits goes closer to the boundary.

That is when most of the diffusion process or the deposition process tends to have a different profile, that is the reason why we have the ring oscillator circuits attached at the corner and if you know this particular value of N = 31. 31 stage inverter ring oscillator will be created at the corners and if it creates, if it gives or after the verification if it gives 2.68 gigahertz then we say that the chip is working perfectly fine.

If there is any kind of a deviation with respect to 2.68, then we will have to give it back to the manufacturers or there is always a tolerance level which we can characterize for this particular chip and then proceed further. In that sense I think the ring oscillator is very very useful. The other aspect of the ring oscillator is it provides a kind of a clock frequency. A frequency of 2.68 can be self generated by the circuit without giving any kind of an external power.

Sometimes the ring oscillator is also used, if you want an external you know not only the one clock, but if you want a different clock it can be generated well within the circuit. Especially it is used for many of the mixed signal circuits where the analog circuits are also there and we want an external clock.

In that sense the ring oscillator design is very very useful and it turns out to be a very simple design where we have a cascaded inverters fed back to the input of the first inverter. Hope you have understood this particular aspect of the ring oscillator.