Design and Analysis of VLSI Subsystems
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Lecture - 32
Logical effort for short - channel current model

Hello students, welcome to this lecture on the Logical Effort and the Ring Oscillator. In this particular lecture we will look at evaluating the logical effort for the short channel current model. We will first look into the long channel current model and then whatever we have done the logical effort estimation, we will try to conclude that or validate that and then we will proceed further with the short channel current model. What are the necessary changes that is incorporated while estimating the logical effort.

The logical effort in that sense is very important because using the linear delay model, we can use this logical effort parameter to estimate the overall delay of the critical path in any complex digital circuit. I think the logical effort is very important and in the later stages we will also have a look into the ring oscillator, which is kind of designed from the series of the inverters.

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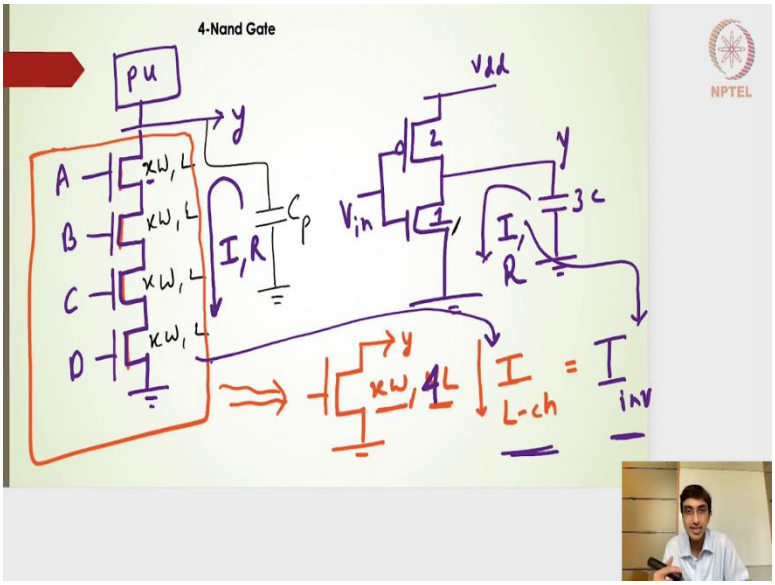

Let us proceed further, I have an empty slide here that means, I have written the 4 input NAND gate here. What I am going to do is, I am going to draw on the pull down circuit

for input NAND gate and I am going to not draw the pull up circuit, the 4 transistors which are in parallel in the pull up circuit that is something I am going to avoid that.

This is my output and then this here I will have my pull up circuit, I am just connecting that. In the pull up circuit I will have 4 of the PMOS transistors in parallel, in the pull down circuit I will have 4 of the NMOS transistors in series. I have this transistors A, B and then C and D, there are 4 inputs.

If I really want to estimate what should be the size of this, we have taken the size of 4 here for each of the transistors so that I will get an equivalent current of equal to that of 2:1 inverter. Let me draw the 2:1 inverter also, and then you should be able to find out the overall, why do we have the size of 4.

This is 2:1 inverter, the load capacitance here, if I assume there is no external load to the y output. The parasitic capacitance will be 3c here and this being a PMOS. I am going to have this is the Vin for the inverter. The current here will be I am just representing a current of I, that is taken from the falling resistance of R. The falling resistance of R because of this particular falling transistor size is 1, that is what we know.

In this particular case, let me rewrite this width as xW, xW, xW and then xW and I am writing this xW, that means that one W is the unit NMOS transistor width and x times the W means, x times x is a scaling factor multiplied by whatever width we have for a unit NMOS transistor.

I will have xW here, xW here, xW here and xW here. I am also going to write the channel length here. I am going to represent it as a channel length L here, channel length L here, channel length L here and channel length L here. This is the dimensions of the circuit, dimension of the transistor basically what we have designed for the 4 input NAND gate and especially on the pull down circuit.

What we really want is the capacitor current or the capacitor discharging current. I am going to draw a capacitor here. Let us say that we have a load capacitance or rather in fact, I should write it as a parasitic capacitance C parasitic. What we really want is this C parasitic capacitance that is coming from the pull up circuit as well as this xW,L channel, that will be incorporated into this parasitic capacitance seen at the output node.

This particular discharging current should be I with the following resistance of R, that is what we want. If you look into this 4-series transistors, I can also conclude this has equivalent to one series transistor connected to the y node. Just to estimate the falling resistance or to estimate the falling discharging current, I can make it an equivalent single transistor with NL channel length, keeping the same width of xW equivalent to NL.

If I consider each of this channel resistance. The equivalent of the 4 transistors I can rewrite it in the terms of a single transistors having the channel length of NL. The current for this particular transistors I can equate I or I can express this using a long channel and I can take whatever the saturation current or the linear current, this should be equated to the current here of the inverter which is 2:1.

This particular current and this I current which is nothing but the long channel current coming from the four series transistors which have made it equivalent to a single transistors of having the same width and then the N times or the 4 times the channel length. I have written here N which is nothing but N = 4 here. If there are N transistors I can have it as NL.

This current coming from the 4 series transistor, we should equate it to the 2:1 inverter, in this case it is the current is I here. If I equate it then I should be able to find this x value as nothing but 4. That is how we have arrived at the logical efforts of the normalized parasitic factor, where we have ensured that the output current or the capacitor discharging or the charging current which is nothing but the output current of any gate circuit made it equivalent to that of the output current of the 2:1 inverter and that is how we have identified the sizes and that is how we have calculated the logical effort or the normalized parasitic factor. This is how we have arrived the value of x and this is how for a 4 input NAND gate we said that the x = 4, for a 2 input NAND gate the x value is 2 and then so on. Hope this is clear, moving ahead.

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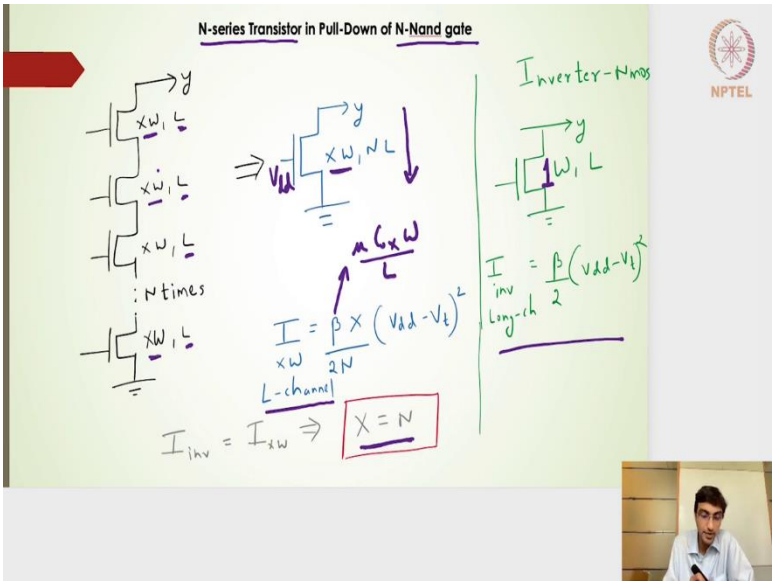

What we really have is I am just trying to summarize in this particular slide is this XW value, XW value, an XW value if we have an N-series transistors, in the form of an N input NAND gate. If I take out the pull down circuit, I will have N-series transistors of the size XW, L; XW, L. The channel length does not change mostly in most of our digital circuit we will keep the channel length to the lowest possible and the feasible fabrication level which is the single channel length.

What we can change is only the width and if I have XW width, I can equate it to XW,NL and if I want to find out what is this current here. I can use the long channel current expression, I have used the saturation current, it will be nothing but,

$$I_{\substack{xw \\ L-channel}} = \frac{\beta X}{2N}(V_{dd} - V_t)^2$$

This beta is for a unit NMOS transistors.

Where, $\beta = \mu C_{ox}\frac{W}{L}$

If I am scaling this by X times, the width by X times. I should have multiplied by X and if I am scaling this channel length by N times, I will have NL. This current has to be equated with that of the W,L. In the 2:1 inverter I will have 1 width, channel length of L.

$$I_{\substack{inv \\ long-ch}} = \frac{\beta}{2}(V_{dd} - V_t)^2$$

This one I have to equate it to this, so that I will be able to find out the X value which is nothing but turns out to be N.

$$I_{inv} = I_{XW} \Rightarrow X = N$$

In a long channel model it becomes a linear proportion, for a 4 series transistor. For a 4 input NAND gate X value turns out to be 4, for a 2 input NAND gate the X value turns out to be 2, for a 3 input NAND gate it turns out to be the value of 3, this is how we get. If you use a long channel model we will get a linear relationship between the scaling of the width with that of the number of transistors that are in series, hope this is clear.

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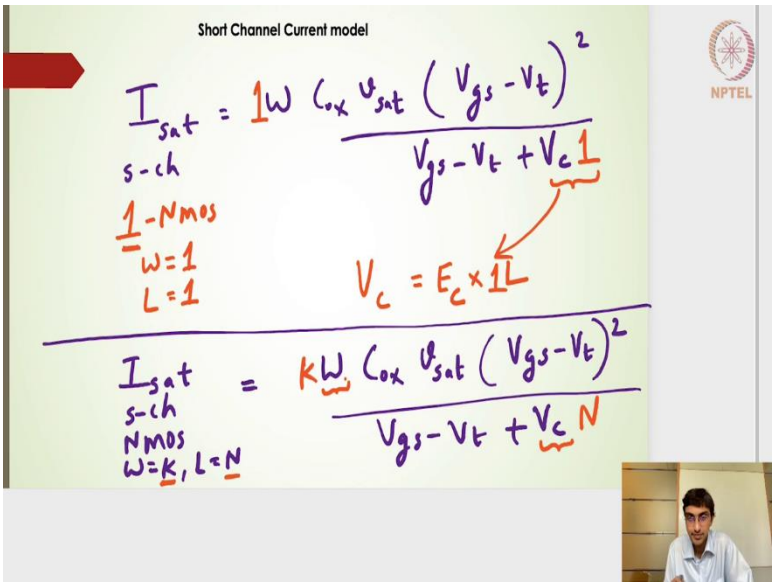

Now what is the difference between the short channel model, if you use a short channel current model? Let us write down the current equation of the short channel. I am going to write down the saturation current, it is much simpler, saturation current for the short channel.

$$I_{\substack{sat \\ s-ch}} = \frac{WC_{ox}V_{sat}(V_{gs} - V_t)^2}{V_{gs} - V_t + V_c}$$

For a unit NMOS, what I am going to write is for an NMOS of size of 1. This is the size of 1, that means my width is 1 and let me write as width is the unit NMOS, the channel is 1 what it represents is the minimum or the unit NMOS transistor.

The V_c will be 1 here, 1 W and then 1 V_c and I have written the V_c of 1 here is because remember that the critical voltage is directly proportional to the channel length. If I bring it the V_c value it is nothing but,

$$V_c = E_c x 1L$$

In this case the channel length is 1.

If I want to rewrite this particular current for a different scaled NMOS transistor. Let me write it as,

$$I_{\substack{sat \\ s-ch \\ NMOS \\ w=k,L=N}} = \frac{WC_{ox}V_{sat}(V_{gs} - V_t)^2}{V_{gs} - V_t + V_c}$$

I need to accommodate something else because now the width is scaled by K times, I am going to write it as,

$$I_{\substack{sat \\ s-ch \\ NMOS \\ w=k,L=N}} = \frac{kWC_{ox}V_{sat}(V_{gs} - V_t)^2}{V_{gs} - V_t + V_cN}$$

Where V_c for the unit NMOS transistor and then W is for the unit NMOS transistor for the short channel, hope this is clear to everyone.

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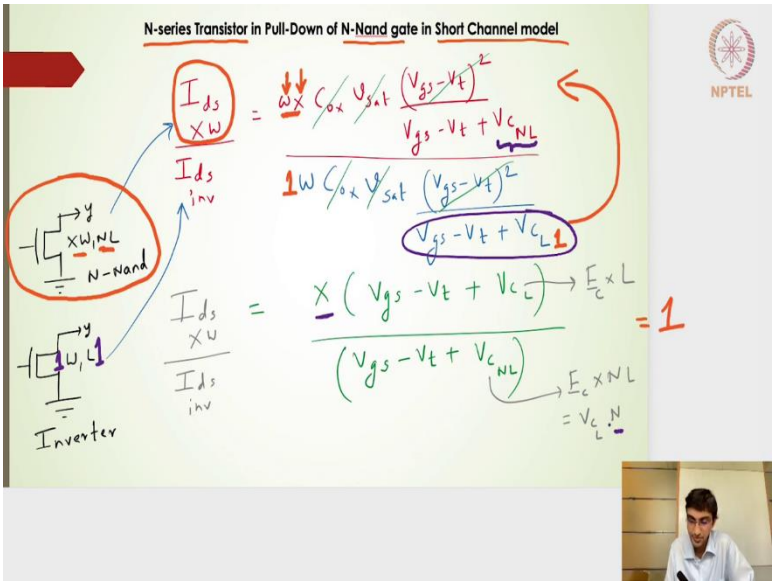

With this particular short channel current model and how it differs for a different dimensions of the NMOS transistor, we will now then try to see for the N-series transistors, that means in a pull down circuit for an N-NAND gate, while we are taking the short channel current model I will have the current equation. This represents the equivalent transistor coming from the N series transistors which are put in the pull down circuit of the same dimensions of XW, very very similar to our long channel current model where we had N such series of transistors and then we made it equivalent to one transistor of XW and NL. The channel length is increased by NL and XW.

We will have this particular current. This is the current here,

$$\frac{I_{ds}}{\frac{XW}{I_{ds}}_{inv}} = \frac{WXC_{ox}V_{sat}\dfrac{(V_{gs}-V_t)^2}{V_{gs}-V_t+V_{c_{NL}}}}{WC_{ox}V_{sat}\dfrac{(V_{gs}-V_t)^2}{V_{gs}-V_t+V_{c_L}}}$$

W stands for 1 unit transistor and X is the scaling factor. W is for the 1 unit NMOS and then X is the scaling factor and then here I have written it as the critical voltage VcNL, what it represents is the critical voltage for the N times the channel length. If I consider a 2:1 inverter where I have the scaling is 1 here and then the scaling is 1 here for the channel length. I will get a inverter current as W, the scaling is anyways 1 here. 1W and then Vc of L where the scaling is actually 1 here, these 2 currents has to match. What I have done is taken the ratio of this 2 current should be equal to nothing but 1.

$$\frac{I_{ds}}{\underset{XW}{I_{ds}}} = \frac{X(V_{gs} - V_t + V_{c_L})}{V_{gs} - V_t + V_{c_{NL}}}$$

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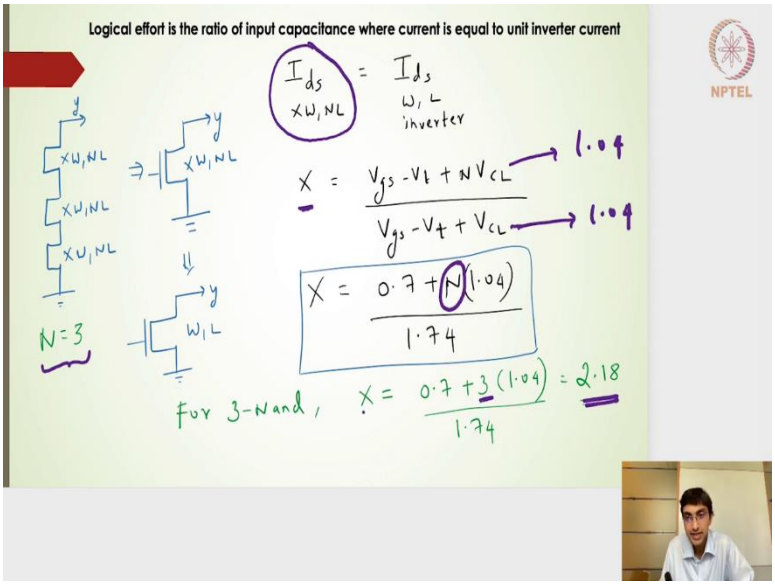

What we have seen is, if N = 3 here it will get the equivalent transistor which we can make is XW = NL will be nothing but 3L and if I equate the currents. I need to find out the X value here turns out to be,

$$I_{\underset{XW,NL}{ds}} = I_{\underset{inv}{ds}}$$

$$X = \frac{(V_{gs} - V_t + NV_{c_L})}{V_{gs} - V_t + V_{c_L}}$$

If I put the critical voltage values for the unit NMOS transistor, it is nothing but,

$$X = \frac{0.7 + N(1.04)}{1.74}$$

X is now as a function of N and it is not equal to N. In a long channel current model what we had seen was XW as equal, it was equated to N because both these currents will be nothing but X/N here will be equated to the inverters current. Both the currents values will be in this particular current value X it will be nothing but the inverters current which will be scaled by X/N times in the long channel current model. Whereas, in the short channel

current model it will not get scaled to X by N times rather it will have some component in the denominator and then the numerator.

If I put the value of all the 3 input NAND gate. For N is equal to 3, I will have the X value as,

$$X = \frac{0.7 + 3(1.04)}{1.74} = 2.18$$

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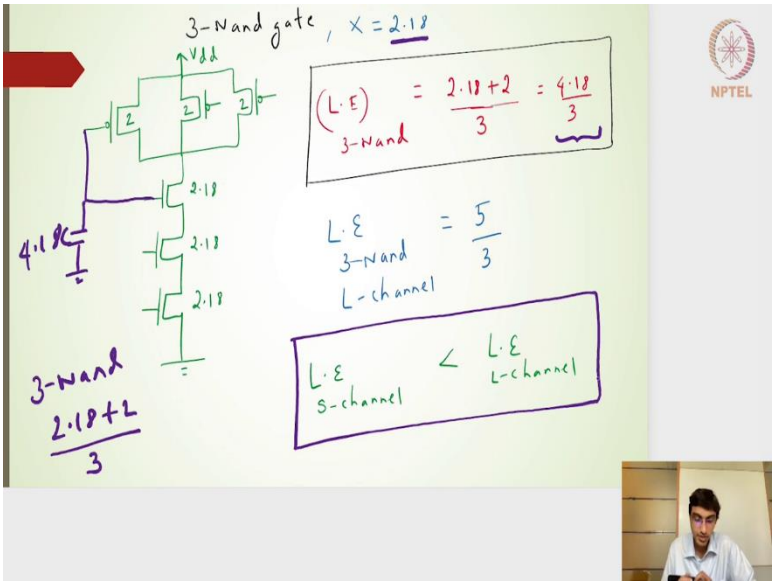

For a 3 input NAND gate, I will have X = 2.18 which is in fact better because, if I use the long channel current model it will give me the X value of 3. Having an X value of 3 what it means is the in the input side the gate capacitance is 2 + 3 = 5. If this 3 input NAND gate is kind of loaded, this is loaded at the output stage to the first stage any circuit then it has to drive the 5c capacitance. Whereas, the short channel current model gives us a value of 2.18 on the pull down side.

The overall capacitance here, if I connect this two as 1 input. The overall capacitance here is 4.18 which is lower than that of the 5c, that means the overall delay will be slightly less than when I use it and then when I estimate it using the long channel current model.

For the logical effort now turns out to be nothing but,

$$(\mathrm{L.E})_{3-\mathrm{NAND}} = \frac{2.18 + 2}{3} = \frac{4.18}{3}$$

In the short channel model, I will get $\frac{4.18}{3}$, and then $\frac{5}{3}$ using the long channel. The short channel logical effort is always less than that of the long channel you know the logical effort for estimated from the long channel current model. This is something we had seen for the pull down circuit especially for the 3 input NAND gate.

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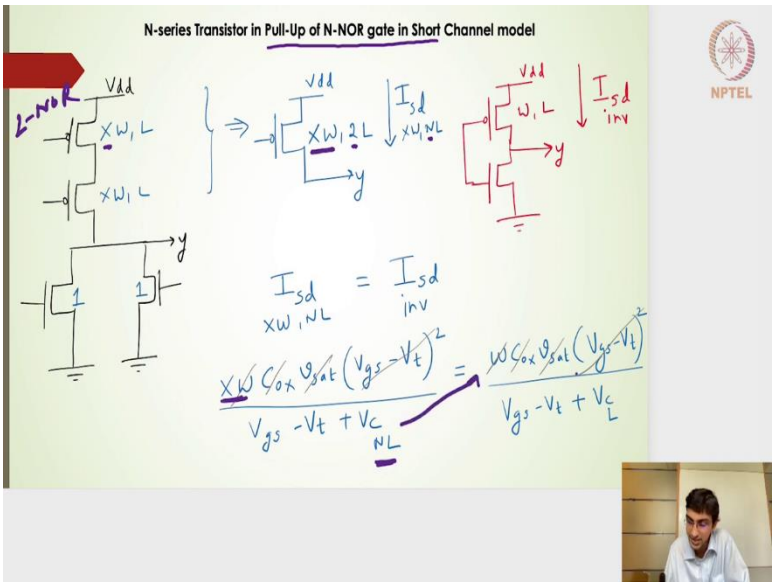

Let us proceed further and take a look at the N series transistors in the pull up of the N-NOR gate. If I have an N input NOR gate I have the N transistors which will be in series and if I have N such transistors in series what should be the short channel model what should be the logical effort we are getting.

Here for example, I have taken only two transistors, it is a 2 input NOR gate which can be easily be extended into an N input NOR gate. For a 2 input NOR gate here what we have done is XW and XW,L and then 1 and 1. If I use a long channel model here this X value will be nothing but 4, because a 2 input NOR gate, 2 of the PMOS transistors will be in series.

If I want to get a current equal to that after 2:1 inverter, I should get a current of I and that is the reason why X has to be 4, assuming the mobility of the holes in the long channel current model is half that of the mobility of the electrons and that is why the width is should be twice that of the unit NMOS transistors and that is the reason why we get the X as 4, if we have 2 of the PMOS transistors in series.

If I take this PMOS transistors, two of the PMOS transistors, the equivalent of that will be XW, 2L and its current will be XW, NL, its current will be XW,NL, where N represents the value of 2 and if I want to equate this current with that of the inverters current of having W,L. I am going to take I_{sd} of inverter which is the inverters pull up circuit charging current. I am going to take the saturation current again.

$$=$$

$$\frac{WXC_{ox}V_{sat}(V_{gs}-V_t)^2}{V_{gs}-V_t+V_{c_{NL}}}=\frac{WC_{ox}V_{sat}(V_{gs}-V_t)^2}{V_{gs}-V_t+V_{c_L}}$$

I have accommodated the XL here, the width X here and accommodated NL, in this N = 2 or in terms of N to the channel length here in the critical voltage expression. If I equate these 2 currents so that we can find the width, we can estimate the logical effort for an N input NOR gate. The logical effort definition says that the output current should be the same and that is the reason why we have equated or we have brought both the currents to be same.

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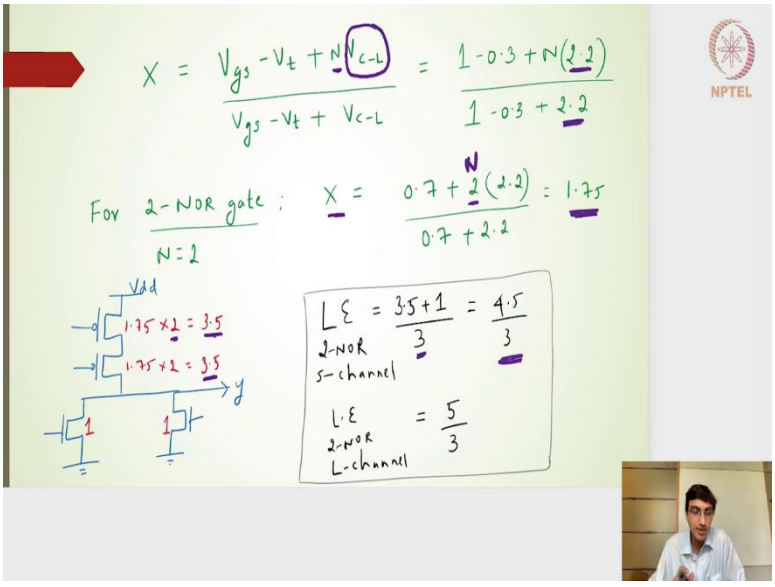

$$X=\frac{V_{gs}-V_t+NV_{c\_L}}{V_{gs}-V_t+V_{c\_L}}=\frac{1-0.3+N(2.2)}{1-0.3+2.2}$$

For the PMOS the critical voltage is 2.2, whereas, the critical voltage for an NMOS is 1.04, there is a slight difference there and that needs to be accounted for.

For a 2 input NOR gate we have this N is equal to 2,

$$X = \frac{0.7 + 2(2.2)}{0.7 + 2.2} = 1.75$$

Remember that this 1.75 has to be scaled by 2 times and turns out to be 3.5. There is 2 times ensuring that the mobility of the holes is considered to be half that of the mobility of the electrons and that is the reason we have considered multiplied by 2 here. That brings us to 3.5 and then a size of 1 and 1. The logical effort for a 2 input NOR gate in a short channel is turns out to be,

$$LE_{\substack{2-NOR \\ S-channel}} = \frac{3.5 + 1}{3} = \frac{4.5}{3}$$

If I look into the long channel 2 input NOR gate the logical effort of the input side, the logical effort of the input for a 2 input NOR gate turns out to be,

$$LE_{\substack{2-NOR \\ L-channel}} = \frac{5}{3}$$

It is conservatively higher than that of the 4.5 divided by 3. What we have concluded is the logical effort what we have calculating from the short channel model or the long channel model. The short channel model will always give you a less logical effort, which is actually very very good in terms of the delay the overall delay will be anyways be lesser if you consider the short channel model.