Design and Analysis of VLSI Subsystems
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Lecture - 30
Logical effort and Parasitic delay
CMOS - Logical Effort

Hello students, welcome to this lecture on the Logical Effort, and in this particular lecture we will see mostly on circuits the logical effort and then the c normalized parasitic values, which are estimated for the circuits which are designed especially for the digital circuits which are designed through the CMOS technology.

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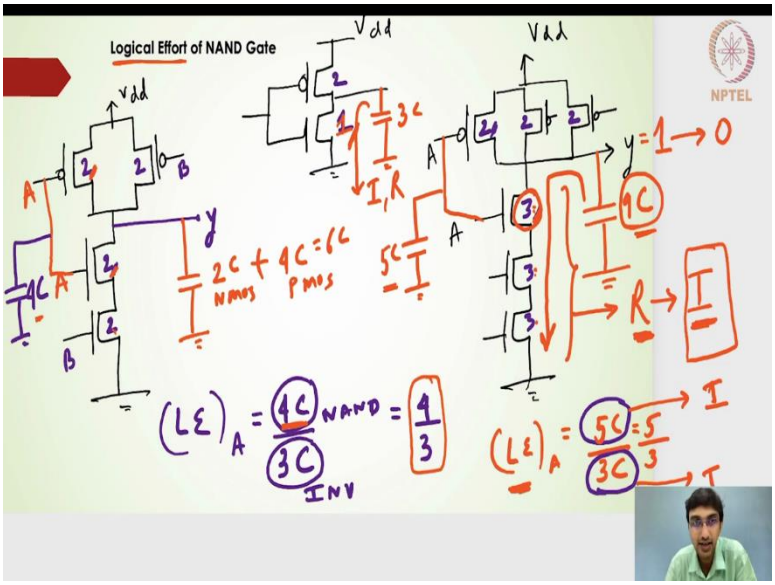

Let us begin with the NAND gate. I am going to draw a NAND gate here and let us say that I am going to draw the 2 input NAND gates and then try to find out the logical effort of those 2 input NAND gates.

In the NAND gate I will have pull up and pull down circuits, where the pull up will be in parallel and pull down circuit will be in series this will be Vdd and because its a PMOS I need to have a bubbled gates and the PMOS side and then on the NMOS side it will be like this the sizes is very important here and as we know this is a 2 input. I will make it the size of 2 and 2, the falling resistance will be equal to R which matches to that of our inverters falling resistance.

On the pull up side on the PMOS side I will have the sizes as 2 and 2, that on the worst-case condition one of the transistors will be on and then we will have the rising resistance will be nothing but equal to R which is nothing but equal to that of the inverters rising resistance.

This is my circuit and of course this will be my output node in a linear delay model I will have. We will have the overall capacitance seen at the output node will be nothing but 2 + 2 + 2. Where this 2 is coming from the NMOS side and then +4 capacitance. I am going to write 2C + 4C, 4C capacitance is coming from the pull up side or I am going to write it as a PMOS side. The total is nothing but 6C capacitance, but I think what we want is a logical effort by definition it says

$$\text{logical effort} = \frac{\text{input capacitance}}{\text{inverters input capacitance}}$$

What we are saying is here I am considering the input capacitance for one of the gates. If I am considering this as A and A here, this two will be tied together and then let me pick another color. The overall input capacitance here will be nothing but this 2 and then this 2, it will be nothing but 4C. This 4C capacitance will be utilized to find out the logical effort for the input A here I am just considering the input A at this point of time. You can also have the logical effort for the B in this case it will be nothing but same as the logical effort of A.

$$(\text{LE})_{\text{A}} = \frac{4\text{C}}{3\text{C}}$$

This 3C is coming from that of the inverters input capacitance and then this 4C is coming from the 2 input NAND gates input capacitance.

$$(\text{LE})_{\text{A}} = \frac{4}{3}$$

Similarly, if I draw the 3 input NAND gate, I will have three of the PMOS transistors in parallel and then I will have three of them in series. I have drawn this and this should be bubbled because its a PMOS transistor bubbled here and then I will have all of them NMOS transistors, I am considering one input because all the other inputs will also see the same input capacitance this is V_{dd} the other is nothing but ground.

This is my output node and let me put the sizes here for a 3 input NAND gate we know that the size should be 3 here, 3 here, 3 here. So, that I will get the following resistance as R which is similar to that of the inverters falling resistance and the sizes should be 2 here. At the input side if I connect this two because its the same input, I will have the overall capacitance at the input side is nothing but 2 + 3 = 5C.

The logical effort by definition as it says for the input A is,

$$(\mathrm{LE})_{\mathrm{A}} = \frac{5\mathrm{C}}{3\mathrm{C}} = \frac{5}{3}$$

What we have done is we have considered the input capacitance of this particular gate and we took that in the numerator and in the denominator it is nothing but the inverters input capacitance.

But what it really means is this particular capacitance of 3C and then 5C will ensure it is actually coming from the sizes of the transistor, this 3 transistor is the size this 2 is the size, the sizes are designed are selected in such a way that I will have the same output current. What do you mean by an output current. If I draw this particular capacitance here I will have a total capacitance of 2C + 2C + 2C + 3C = 9C here.

In this case it is nothing but 2C + 4C =6C this is the output capacitance. Now if I am considering the falling output, I am interested in this particular discharge path because the y is going from 1 to 0 that is when we are considering the falling output. The transistor sizes, now the size of 3 here is selected in such a way that I will get an equivalent falling resistance of R which is similar to that of the inverters falling resistance, that is one case.

If I have the switching resistance or the falling resistance as R I am likely to get a current of I, this current of I which is nothing but the discharging current of this 9C capacitance which is attributed because the falling resistance the summation of all these 3 switching resistance is R is what accounts to this particular current the discharging current.

If I have the same resistance R in a 2:1 inverter will give me a falling resistance of R, I am likely to get the current of I even for an inverter which is giving a falling output, that means that the inverter which will see a 3C capacitance at the output will also give me a discharging current of I.

Even for 2:3 size or for a 3 input NAND gate 2:3 size means two size for the PMOS three size for the NMOS which will give me the 9C capacitance, but the 9C capacitance actually having a discharging current of I because it sees a falling resistance of R, which matches with that of the 2:1 inverter which also has a falling resistance of R and a discharging current of I.

In that sense if I have for both the gates the same current I here same current I here, then I can consider taking the ratio and then that particular ratios giving the same output current that is what the output current means the discharging current of the 9C or whatever 2:1 inverter giving a discharging current of I for a 3C capacitance.

If I have the same currents for the 3 input NAND gates and then for the 2:1 inverter then I can consider the ratio and that will be the logical effort. What it really implies is if I have the width of 2:3, the width of 3 is more than the width of 2:1 inverter on the NMOS side.

Let me draw the 2:1 inverter somewhere here, this is the ground this is the V_{dd} this is the size of two this is the size of one I will complete the PMOS. I will have a bubbled gate I will have the non-bubbled gate representing the NMOS and this is my output what I am saying.

The capacitance at the output is nothing but 3C, a size of one is giving me a current of I or a resistance of R. I am going to write I and then R here for the 3 input NAND gate for getting the same current I and then for getting the same falling resistance of R, we need to size it we need to scale it up to 3 times more. The logical effort here implies that for this particular 3 input NAND gate I need to have the more effort when I compare that with that of the inverters.

The more effort means 5/3 times more effort is required, as to get the same current, that is what it represents. The logical effort by definition says it there is an additional effort for the 2 input NAND gate or for a 3 input NAND gate and how much more effort with respect to that inverter will be nothing but based on the input capacitances, that will be 5/3 for a 3 input NAND gate.

Similarly, for a 2 input NAND gate I will have to size it up two times more at the NMOS side. The NMOS side the inverter is 1 here it is 2, it is twice more. My logical effort will be nothing but 4C/3C (4/3), but it also says is the logical effort for a 3 input NAND gate

is more than the logical effort of the 2 input NAND gate and it is quite obvious 3 input NAND gates will need to size it up three times here and for my 2 input NAND gate I need to size it 2 times, its input capacitance will be 4C here the input capacitance is 5C.

Hope this is clear kind of very important at this particular point of time when we are designing the gate sizes.

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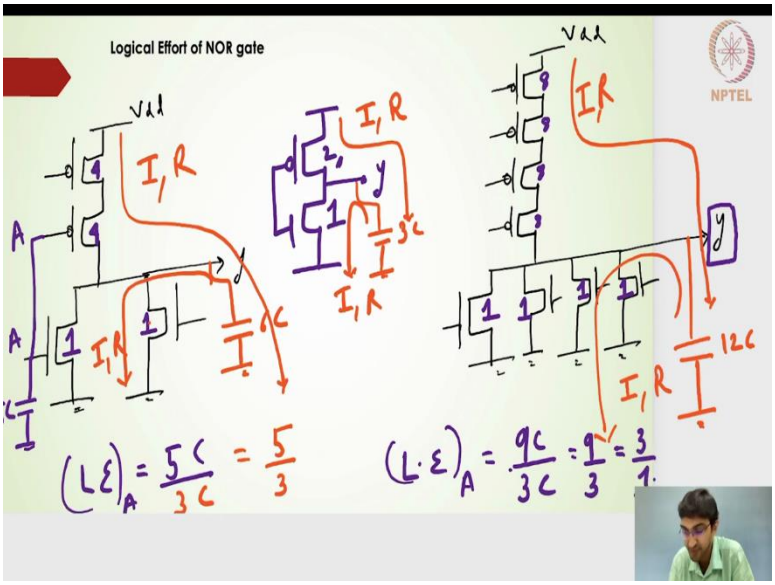

I need to summarize for the NOR gates. So, let me quickly draw the NOR gate 2 input NOR gate, again a 2 input NOR gate I will have on the PMOS side I will have a series of two PMOS transistors and then on the NMOS side I will have it parallel.

This is my NMOS and this is my output, this is V_{dd} and this will be my PMOS transistor the sizing of this particular PMOS transistor is done such that I will have equal falling and equal rising resistance to that of the inverters 2:1 circuit. Here I will size it to 4 and 4. So, that I will get R/2 from this individual PMOS transistors and put together I will get in rising resistance of R here I will make it 1 and 1.

My logical effort if I consider one of these inputs which are tied, if I consider input this to be an A input, I will get the capacitance of 5C here.

$$(\mathrm{LE})_{\mathrm{A}} = \frac{5\mathrm{C}}{3\mathrm{C}} = \frac{5}{3}$$

I am going to draw that V_{dd} rail and then 1 and then the ground rail and the size of 2:1 which will give me an output here y.

If I consider the capacitance here it will be nothing but 3C here which will have the current of I and then the resistance of R, similarly if I consider the output capacitance here which will be nothing but 1 + 1 + 4 = 6C here and then this one while it is falling, I will get a current of I and the resistance of R and while it is charging, it will have a current of I and then the rising resistance of R.

Similarly for the charging for this 3C, I will have a current of I and then the rising resistance of R. It matches both the benchmark inverter of 2:1 matches with that of 4:1 which is nothing but 2 input NOR gate and then I can take the ratio of 5C and then the 3C. Eventually I will get the logical effort for a 2 input NOR gate is 5/3 and similarly just to complete we will draw a 4 input NOR gate.

I will not draw I will skip the 3 input NOR gates because we have anyways done the 3 input NAND gate. The 4 input NOR gate I will have four transistors in series on the pull up side and then four of them in parallel on the pull down side. I am just going to draw this transistors complete it and then I will have this four of the series transistors complete the Vdd rails and then anyways we have the ground, this will be my output y putting the sizes now, this is four of them.

I will have it as an 8 here, 8 here, size of 8 here size of 8 here which will give me an equivalent of R/4, R/4, R/4 and R/4 for the individual transistors and then put together it will be a rising resistance of one R which will be equal to that of the benchmark inverter 2:1 ratio inverter rising resistance.

On the pull down side I will have the size of 1, 1 and 1. So, that I will get in the worst case condition one of them will be on and then I should be able to get the output discharge to 0 and that is why I have the size of one here. The output capacitance just for our one understanding I will have some capacitance which will be nothing but 8 + 1 + 1 +1 + 1 = 12C.

The output capacitance while it is discharging it will be discharging with a current of I and then the falling resistance of R and while it is charging. It will have a rising resistance of

R and then the charging current will be nothing but I. In that sense the logical effort in this case will be nothing but logical effort of one of the inputs I am considering it as an A input,

$$(LE)_A = \frac{9C}{3C} = \frac{9}{3}$$

This is for the 4 input NOR gates, of course 9/3 will become nothing but 3/1.

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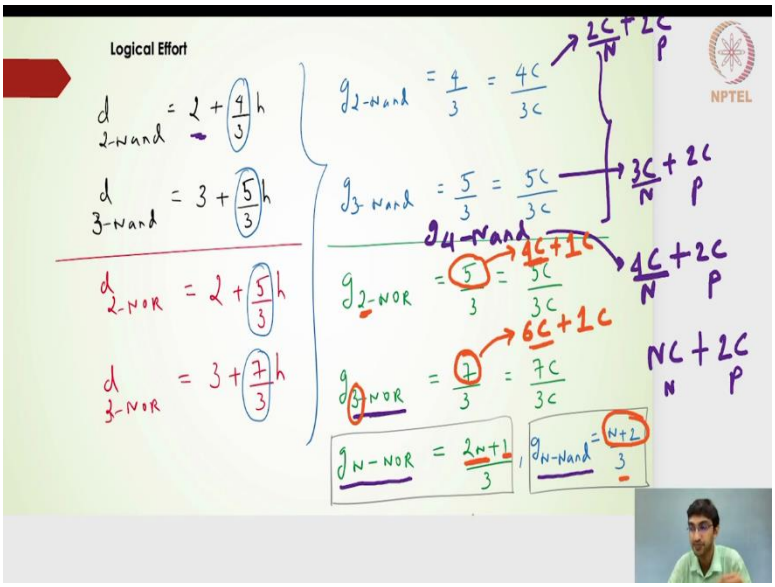

Hope this is clear, moving ahead. What I have done is I have summarized, it for the 2 input NAND gates and 3 input NAND gates the delay and the 2 input NOR gates and then 3 input NOR gates and finally, we have evaluated for the N input NOR gates and then the N input NAND gates.

Let us quickly take a look at it, this is the delay values for 2 input NAND gates is,

$$d_{2-NAND} = 2 + \frac{4}{3}h$$

For the 3 input NAND gates we will have 5/3, for the 2 input NOR gates we had seen 5/3 and then for the 4 input NOR gates we had seen 9/3, for the 3 input NOR gates it will be 7/3. The logical effort turns out to be,

$$g_{2-NAND} = \frac{4}{3} = \frac{4C}{3C}$$

For the 3 input NAND gate we have seen 5C/3C. For the 2 input NOR gate, it is 5C/3C and then for the 4 input NOR gate it is nothing but 9C/3C, for the 3 input NOR gate it is nothing but 7C/3C. If I put together if I want a generic expression for an N input NAND gate, if I look into this aspect right 4C and then 5C. This 4C is actually coming from 2C from the NMOS side and then NMOS which is in series with other NMOS and then this 2C coming from the PMOS side this 5C, if I consider it is actually 3C coming from the NMOS side.

I am going to write it as N and then this is P. I am going to write it as N and then this is going to be the 2C coming from the PMOS side. If I similarly calculate the logical effort of a 4 input NAND gate. The 4 input NAND gate it will be nothing but, I am going to write it as 4 NAND and then the logical effort it will be nothing but, I have to size it accordingly. I will have four times the width and then this will come from NMOS which is at the output node the NMOS transistor which is very close to the output node +2C coming from the other the PMOS input, 4C + 2C that is coming from the PMOS.

The overall what I am saying is the number of inputs increases for the NAND gate for the 2 input it is 2C, for the 3 input it is 3C, for the 4 input it is 4C, for the N inputs it will be NC on the NMOS side, plus 2C from the PMOS side, that is what I have here. To generalize it will be nothing but N for the N input it will be,

$$g_{N-NAND} = \frac{N+2}{3}$$

This is coming from the inverters or 2:1 which is nothing but the benchmark inverter giving the same output current, $\frac{N+2}{3}$, that becomes our general expression for finding the logical effort for an N input NAND gate.

Similarly, if I want to find out the logical effort for an N input NOR gate, if I pick this 5/3, the 5/3 is actually coming from 4 capacitance the width of the 2 input NOR gate especially on the PMOS transistor width is 4. Its input side the capacitance will be 4C and 1C coming from the NMOS side.

This 7/3 this particular 7 is actually coming from a 3 input NOR gate the width will be 6. 6C on the PMOS transistors input gate capacitance plus 1C coming from the NMOS width

will be 1. Its input gate capacitance will be 1C for the 4 input NOR gate it is actually 9C which is actually coming from 8C because the width is 8.

Its input capacitance will be 8 on the PMOS transistor and its the subsequent NMOS transistor will have a capacitance of 1C because the width will be one, that is how it will be 9C. If I look closely into it for a 3 input it is actually 6C for a 2 input NOR gate it is actually 4C. For an N input NOR gate it turns out to be,

$$g_{N-NOR} = \frac{2N+1}{3}$$

Hope this is clear. The logical effort general expression for NOR gate and NAND gate is nothing but $\frac{2N+1}{3}$ and $\frac{N+2}{3}$.

Kind of very very important when we try to estimate the overall delay for a critical path of a large digital circuit and in this particular critical path let us say that you will observe lot of NAND and the NOR gates of different inputs, then I think using the linear delay model we need to estimate what is the logical effort and then this particular generic expression will be very very handy to use in those larger circuits critical path.

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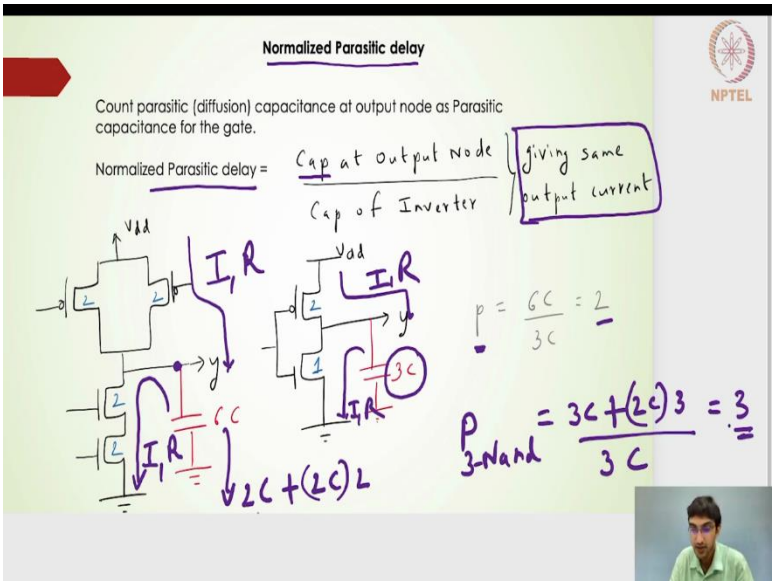

Moving ahead now, I think the logical effort is done and the other component is the normalized parasitic delay. Again, I have taken an example here of the 2 input NAND gates. So, as to get the equal falling and the rising resistance as that of the 2:1 inverter here,

we will see a capacitance of 6C here coming from 2 on the NMOS side and then 2 and 2 on the PMOS side.

The 6C capacitance has arrived from 2C on the NMOS side plus there are two parallel legs or there are two PMOS transistors which are parallel. I will get 2C into 2 and the normalized parasitic definition is

$$\text{Normalized Parasitic delay} = \frac{\text{Cap at output node}}{\text{Cap of Inverter}}$$

What are these capacitance these are nothing but the capacitances which are seen at the output node. Whatever we see the overall or the effective capacitance seen at the output node, that we have to consider in the numerator side for calculating or evaluating the normalized parasitic delay divided by the capacitance of the inverter.

In a 2:1 inverter I will see a parasitic capacitance of 3C, that is what the capacitance seen at the output node. 3C will come here and it is giving the same output current. The same the definition of the logical effort and the definition of normalized parasitic delay remains the same in that perspective.

Because if we need to compare the output node capacitance in this particular case where the output node capacitance actually discharges having the same output current, while it is falling and while it is rising it should have the same rising current of I which is same as that of the inverters rising current of I.

I am going to write it I. If I have the same rising current what it means is the rising resistance is nothing but R and of course, the falling resistance will be nothing but R and then this will be I comma R, that is what the definition is. Once I have the same output current then I can actually do the ratio of the capacitance seen at the output node for that particular gate and with respect to that of the capacitance at the output node for the benchmark inverter 2:1.

In this particular case if I take a standalone 2 input NAND gate,

$$P = \frac{6C}{3C} = 2$$

Again, for a parasitic normalized parasitic delay for the 3 input NAND gate will be nothing but, I will have a size of 3 here on the pull down circuit. I will have a 3C capacitance connected to the output node plus this one will remain the same. I will have 2C, 2C and then 2C coming from another third transistor.

$$P_{3-NAND} = \frac{3C + (2C)3}{3C} = 3$$

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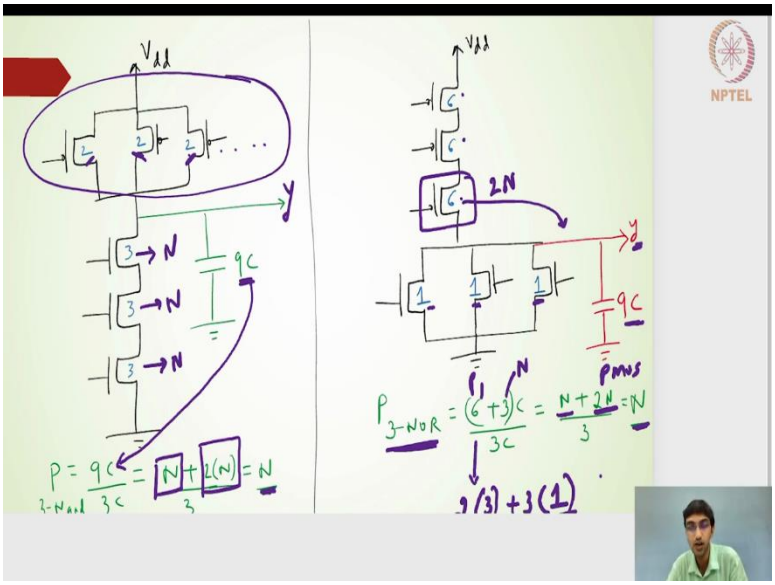

Moving ahead, just to generalize this for a 3 input NAND gate and this is what we have the sizes in the schematic, the output node capacitance is 9C. The parasitic delay is nothing but for a 3 input NAND gate is,

$$P_{3-NAND} = \frac{9C}{3C}$$

Where 9C taken into the numerator and then this 3C coming from the benchmark inverters 2:1 ratio inverter giving an output capacitance of 3C.

Both of them is giving the same output current. In general, if I want to find out that the parasitic delay for an N input NAND gate, this sizes for an N input NAND gate will be nothing but N and this sizes will remain to be 2 because for a NAND gate the worst case is one of the transistors on the pull up side will be on and then that is how the output will reach to a logic one.

I will have, if suppose I have this N such transistor, this on the PMOS side the N such transistors are going to contribute to 2C x N times. It will be 2N times the capacitance and then this N is coming from the transistor which is closest to the output.

This NC will be incorporated into the output capacitance seen at the output node y.

$$P_{N-NAND} = \frac{N + 2N}{3} = N$$

For an N input NAND gate the parasitic delay is N the logical effort is nothing but $\frac{N+2}{3}$, hope that is clear.

I have drawn a 3 input NAND gate and then generalized for an N input NOR gates what should be the parasitic delay. For a 3 input NOR gate we need a size of 6 here, 6 here and 6 here. This 6C is going to contribute to 6 times the capacitance at the output node and on the pull down side we have the sizing as 1, 1 and 1. In worst case I will have the following resistance of 1R which will effectively give me a output current of one I.

All this transistors 1C, 1C and 1C individually will contribute to 1C, 1C and 1C at the output side.

$$P_{3-NOR} = \frac{(6 + 3)C}{3C}$$

If I consider that, this 2N is coming from the PMOS side for an N input NOR gate I will have 2 times N for the PMOS transistor which is closest to the output node. This one will give me for an N input NOR gate I will have a 2 times the N size and that will contribute to 2NC capacitance at the output node.

On the NMOS side each of this NMOS is going to contribute towards 1C capacitance.

$$P_{N-NOR} = \frac{N + 2N}{3} = N$$

The parasitic delay for a 3 input NOR gate is still N or for a 3 input NOR gate it is 3, for an N input NOR gate it is N parasitic delay, for N input NAND gate is also N.

Whereas the logical effort for a N input NOR gate turns out to be $\frac{2N+1}{3}$ which will always be larger than the logical effort for an N input NAND gate. In that sense although the

parasitic delay of the NOR and NAND gates are same. The logical effort for the N input NOR gate will always be larger than that of then N input NAND gate. A NAND gate is almost is always preferable in designing the digital circuits. Hope this is clear.

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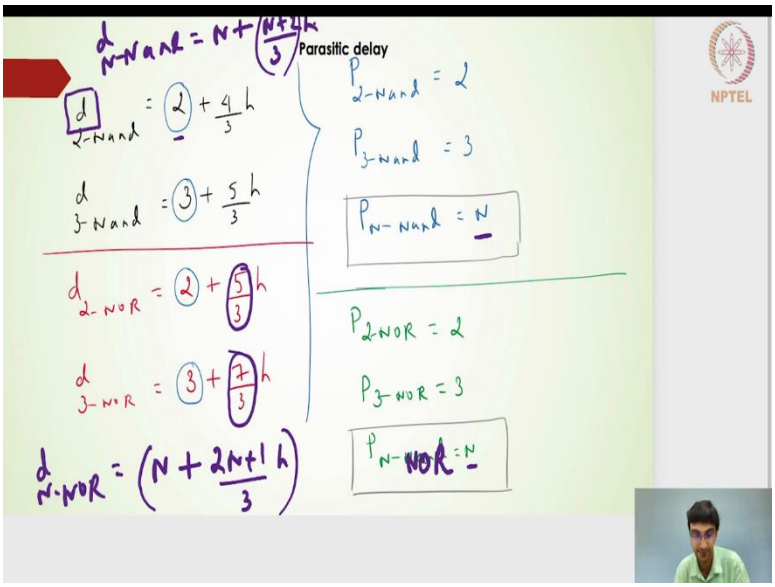

That is what this is what I have summarized. For the N input NAND gate and then for the N input this should be NOR. For N input NOR gate it is N, the overall delay is nothing but the p+gh, 2 plus again its a normalized delay. For a 2 input NAND gate it will be $2+\frac{4}{3}$h, for a 3 input NAND gate it will be $3+\frac{5}{3}$h and for a 2 input NOR gate it will be $2+\frac{5}{3}$h, the logical effort of a NOR is 5/3 and then for a 3 input NOR gate it is (7/3)h.

The overall delay for the N input NOR gate will be nothing but,

$$d_{N-NOR} = N + \frac{2N+1}{3}h$$

If I want an absolute value of the delay it will be nothing but this I have to multiply by 3RC, because we have always taken a ratio, while we are calculating the normalized delay we have taken the ratio with respect to the benchmark inverters delay which is nothing but 3RC. Similarly, the delay for an N input NAND gate will be nothing but,

$$d_{N-NAND} = N + \frac{N+2}{3}h$$