Design and Analysis of VLSI Subsystems
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Lecture - 26
Delay of FO4 inverter

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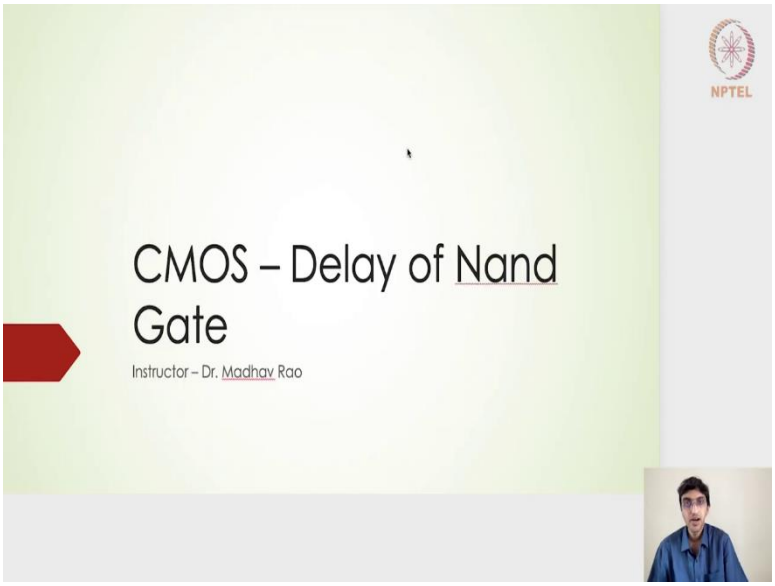

Hello students. Welcome to this lecture where we will be estimating the Delay of a NAND Gate. Till now we have seen only the inverter as a classic example and then we had used the transistors current equation to arrive at the propagation delay falling. Then at some point of time we had approximated that to an RC network and from the RC network we said it is log2 into RC.

Finally, we ignored the log2 expression stating that the input may not be always a step input. There will be some kind of an input transition and to have it more a conservative approach, we said that the falling delay or the rising delay will be nothing but a product of RC.

In our last class we had seen an Elmore delay method and we had established a kind of an expression involving the summation of the product of R and C. That particular Elmore delay method we are trying to apply into the NAND gate, especially we will look into the 3 input NAND gate and then see what is the overall propagation delay falling and then the rising.

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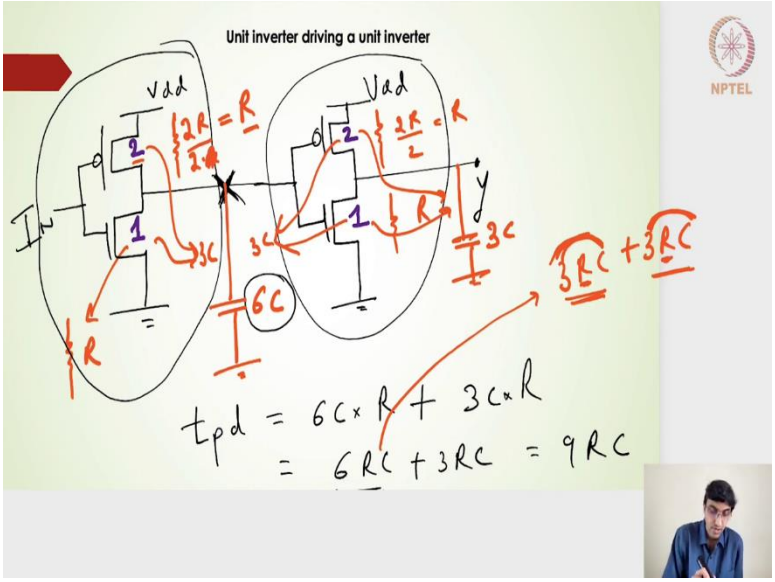

To understand that what we will quickly go over the unit inverter circuit, which is driving another unit inverter, quickly establish that particular propagation delay in terms of R and C. What we wanted to know was if I have an inverter here, a PMOS connected to an NMOS and it is a unit inverter.

That means the size of this particular unit inverter is nothing but 2:1, where k=2 for the PMOS and k=1 for the NMOS. This is my input and then this is connected to another inverter of the same size because it is of the second stage is also the unit inverter we have, here is the PMOS. Bubble transistor will be nothing but PMOS and then this gets connected to the next stage inverter. Again, the size is nothing but of the unit inverter 2:1.

Overall, what we see is a capacitance here, the overall capacitance at this particular output node is nothing but $2 + 1 + 2 + 1 = 6C$. This one will contribute to 3C and then the input side this one will contribute towards the 3C. Overall capacitance is 6C and if I look into the switching resistance of the PMOS side which is $\frac{2R}{2}$.

This PMOS will always have $\frac{2R}{2}$, that will be nothing but R and the switching resistance of this NMOS will also be nothing but R. I am going to write it somewhere here the switching resistance of the NMOS is nothing but $\frac{R}{1}$ which is nothing but R. On the PMOS side it is 2 times R because the mobility of the holes is half that of the mobility of the electrons.

The resistance naturally will be higher too and we have considered for the long channel model it is 2 times R the switching resistance and because the scaling width is twice. We had used $\frac{2R}{2}$ turns out to be R, and then here also the switching resistance nothing but $\frac{2R}{2}$ for the PMOS, which will be nothing but R and then here the switching resistance is nothing but R, R/1 will be nothing but R.

The overall we want to find out the propagation delay of this particular circuit. The propagation delay whether it is rising or falling will be nothing but this particular capacitance at the output of the first stage 6C multiplied by the switching resistance it will be either the PMOS or the NMOS. Because if this particular node is rising we will have the switching resistance incorporated with that of the PMOS transistor.

If this particular output is falling then we will have the switching resistance incorporated or included with that of the NMOS side. It will be nothing but R plus and the output side, if this is the output and then this is the input. This output based on the X as an input.

Now second stage if I am considering, the second stage output coming from the input, for the second stage it will be nothing but the overall capacitance here will be seen at the output node will be nothing but 3C. Because this is the 2 coming here and then this is the 1 coming here. 3C capacitance multiplied by one of the switching resistance either it is a PMOS or NMOS. I will get this one 3C x R. Overall I will get

$$t_{pd} = 6CR + 3CR = 9RC$$

This 6 RC is kind of very interesting what it means is if I have this particular inverter first stage inverter cascaded to another stage. I will get at this particular output I will get the propagation delay falling or rising will be nothing but 3RC + 3RC. 3RC is coming from its own stage capacitances and then the next 3RC is coming from the next stage, the next stage input capacitance multiplied by its own switching resistance.

It is very interesting, this 3C is actually coming from the next stage input capacitance also called as a load capacitance multiplied by its own switching resistance. Here the 3C is actually coming from its own capacitance and then this R is coming from its own switching resistance.

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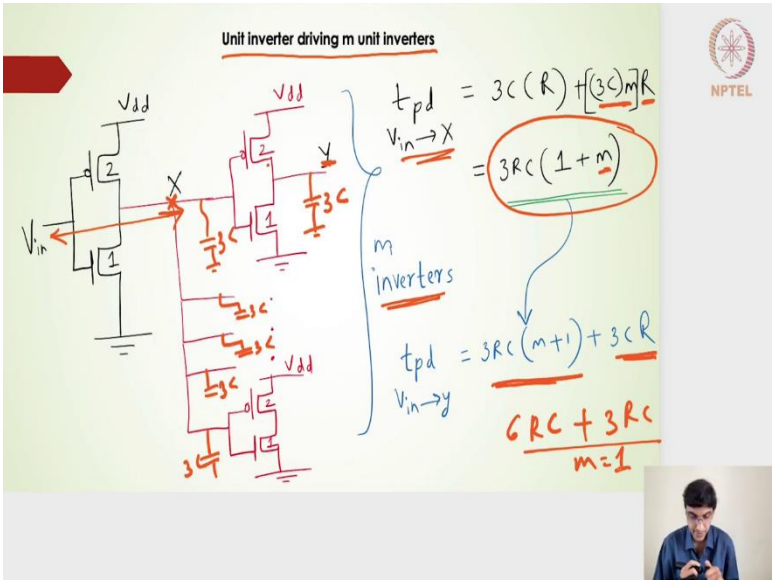

Moving further, what if I have a unit inverter driving m unit inverter. In the last slide we had taken a unit inverter driving only single unit inverter. Here it is driving m such unit inverter, the propagation delay of the first stage means input to the output X here.

This particular path input to output of the first stage will be nothing but 3CR coming from its own stage plus m times because there are m such inverters now connected to this particular X node, there are m such inverters. Each inverter is going to give a capacitance of 3C, each inverter is going to give a capacitance of 3C. That is what I am drawing here each inverter giving a capacitance of 3C, each inverter is giving a capacitance of 3C. I will have m inverter, that means that I am going to have 3C multiplied by m times the capacitance that is loaded at the node multiplied by the switching resistance of R, whether it is discharging or charging based on the NMOS transistor or the PMOS transistor.

My propagation delay from Vinput to X is

$$t_{\substack{pd \\ vin\rightarrow x}} = 3C(R) + [(3C)m]R = 3RC(1 + m)$$

and propagation delay from input to Y output will be nothing but,

$$t_{\substack{pd \\ vin\rightarrow y}} = 3RC(m + 1) + 3CR$$

Propagation delay from V input to X, if m is equal to 1, I will get 6RC + 3RC. That is what we had calculated earlier in the last slide, but this is a more generic circuit where we have m such inverters. Hope this is clear, moving ahead.

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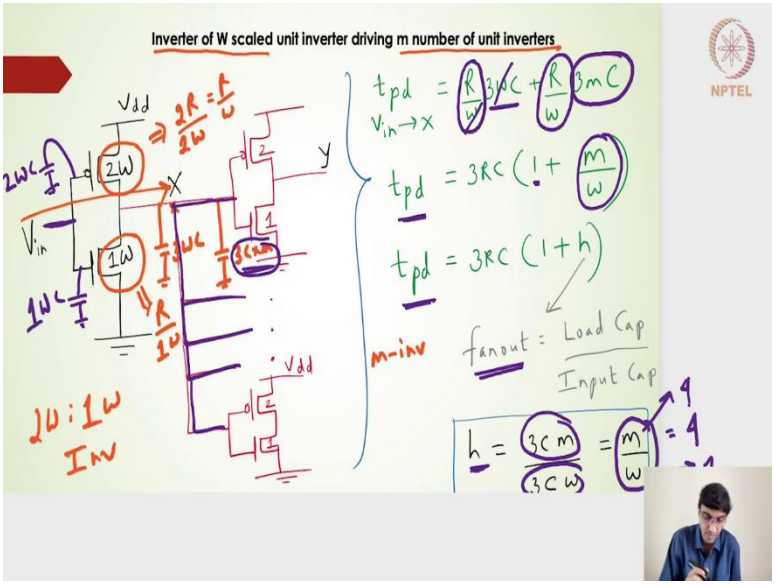

What if I have in the next stage it is not only m inverters, but also the sizes are different. What it means is this m inverters are unit inverters or m number of unit inverters. All the second stage circuits are nothing but m unit inverters, but there are m such numbers of unit inverters, the first inverter the driver inverter has a scaling of 2w.

It is no longer a unit inverter, it is now 2w on the PMOS side and 1w on the NMOS side, now, that 2w:1w inverter. 2w:1w inverter is now driving m unit inverters, m such 2:1 inverter. Again, at this particular X node if I want to see the capacitances coming from this first stage, the capacitances will be nothing but 3wC from its own first stage capacitances, it's switching resistance is nothing but 2R/2w on the PMOS side. It will be nothing but R/w and on the NMOS side it is nothing but R/1w. The output of the first stage is connected to m such inverter. The overall capacitance is seen at the output node coming from the second stage m such inverters will be nothing but 3C x m inverter. The propagation delay from Vinput to X this particular node is given by,

$$t_{pd}{}_{V_{in} \rightarrow X} = \frac{R}{w} 3wc + \frac{R}{w} 3mc$$

The overall propagation delay is nothing but,

$$t_{pd} = 3RC(1 + \frac{m}{w})$$

This $\frac{m}{w}$ is nothing but a fan out. The propagation delay from V input to X is nothing but,

$$t_{pd} = 3RC(1 + h)$$

Where h is nothing but the fan out and this is the propagation delay of the 1 stage, the first stage we have not included the propagation delay of the second stage. It is only of the first stage, that means a signal given at the input and the signal propagating to the X node what is the propagation delay, 1 + h is nothing but the fan out is actually defined as,

$$\text{fanout} = \frac{\text{load capacitance}}{\text{Input capacitance}}$$

If I am looking into the first stage which is nothing but the inverter, the load capacitance is nothing but 3Cm, like it is kind of loaded. The input capacitance of the second stage is kind of getting loaded into the first stage output. That is the load capacitance 3C into m and divided by its own input capacitance. The input side if I consider the capacitance here at the gate and then the capacitances here at the gate of the NMOS and PMOS transistor it will be 1 wc and then 2 wc. Put together both the input tied together, the gate of the PMOS of the first stage and then the gate of the NMOS of the first stage is tied together into the V_{in}. The V_{in} is a overall input gate capacitance of 3wC. The ratio of the input capacitance is 3Cw and then the load capacitance of the first stage is the 3C m. That will be the ratio of those two will be nothing but the fan out or the electrical effort, we also call it as an electrical effort is nothing but m/w.

$$h = \frac{3Cm}{3Cw} = \frac{m}{w}$$

The fan out definition is very simple, it is nothing but the ratio of the load capacitance with that of the input capacitance for that particular stage. It is not how many number of wires I am feeding in, it is not the number of wires I take it to the next circuit like this, this is my one wire, this is my one wire, this is my second wire, this is my third wire, this is my fourth wire, this is my fifth wire.

Generally we get confused, fan out is basically the number of wires that is fed into the second stage circuits that is not the case. The fan out is purely a capacitive ratio definition is the ratio of the load capacitance with that of its own input capacitance, that will be my fan out. Hope this is clear to everyone.

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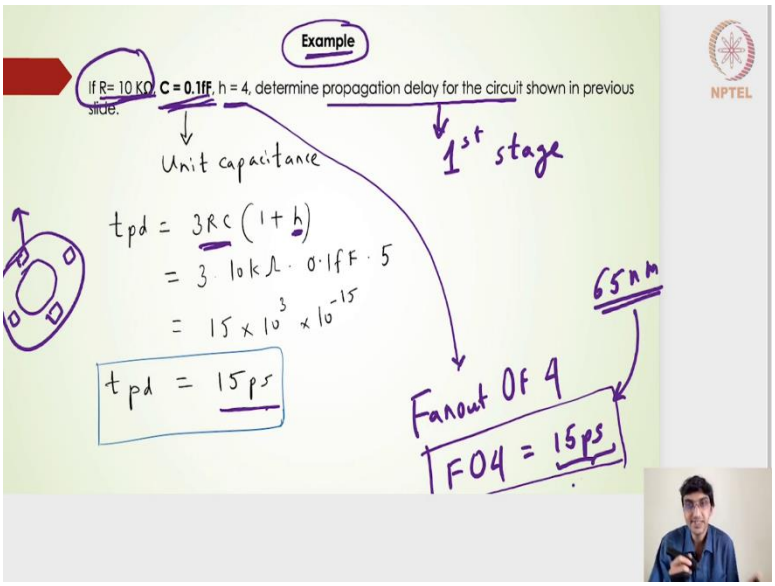

Let us take an example here if the switching resistance of the PMOS or the NMOS, whatever I am seeing $R = 10K\Omega$. The R is nothing but the unit PMOS or unit NMOS switching resistance. Individual $C = 1fF$, that means the unit NMOS capacitance the drain to body capacitance is considered as 1C, which is 0.1 femto farads. The fan out is $h = 4$ for the first stage, determine the propagation delay for the circuit shown in previous.

This propagation delay what we are considering for the 1st stage is only for the 1st stage and not for the second stage. For the first stage,

$$t_{pd} = 3RC(1 + h)$$

If I go back to the previous circuit the fan out is 4, this particular value is nothing but 4 what it means is m/w = 4.

If I have consider m/w to be actually 1 and then m is equal to 4. I have 4 inverters. 1 unit inverter driving 4 unit inverters and for the next stage, that is a basic example what we have in this particular exercise.

$$t_{pd} = 3\ 10K\Omega\ 0.1fF \times 5$$

$$t_{pd} = 15x10^{3}x10^{-15} = 15ps$$

This kind of example or exercise is a very important example. It is basically the fan out of 4. We call it as the Fanout of 4, we also write it as fan out of 4 is nothing but 15ps, which is nothing but a unit inverter driving 4 unit inverters. 4 unit inverter driving a 4 unit inverters and this becomes a very standardized values.

If I want to find out what kind of given technology node there will be fan out of 4 circuits at the corners of the chip. In the chip we will have a different circuits, but at the corners of a chip we will always have this fan out of 4 circuits to ensure whether all my manufacturing process or the design process everything is accurate. The fan out of 4, will give me an specified value.

For a 65 nanometer technology node we will get this fan out as 15ps because the switching resistance is close to 10kΩ, capacitance is close to 0.1fF. The fan out of 4 should give me 15ps, what it means is in a wafer design if I have lot of circuits, in this portion at the corners I will have this FO4 circuits and if it gives me 15ps after the wafer or the chip is manufactured and if it gives me 15ps rest assure that all the manufacturing processing, fabrication processing, the technological processing is accurate. We can use this particular chip for the intended applications, that is where you will see in the textbook or in the literature the fan out of 4 is often used. Hope this is clear.