**Design and Analysis of VLSI Subsystems**
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**Lecture - 23**
**Switching Resistance**

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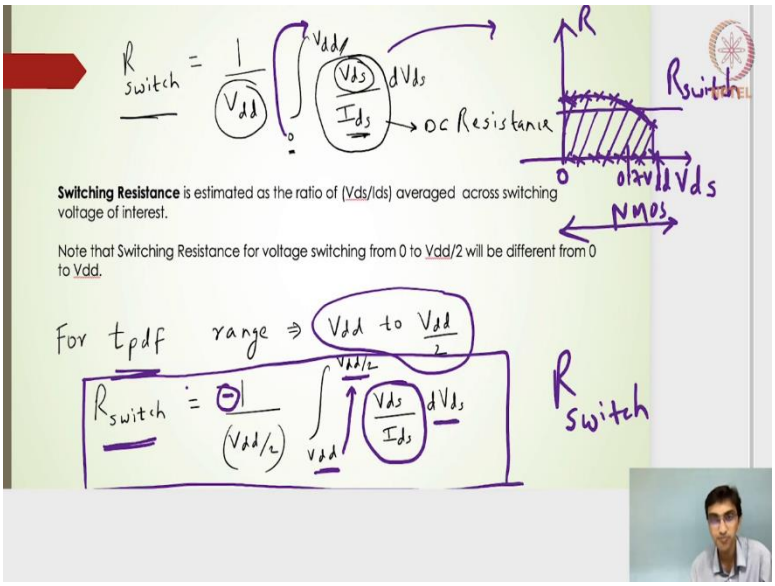


Hello students, welcome to this lecture. The switching resistance by definition it is nothing but an average of all the DC resistance for the voltage range we are interested in. This is nothing but an average of all the DC resistance. $V_{ds}$ divided by $I_{ds}$ is nothing but a DC resistance.

DC resistance means, for a given current $I_{ds}$ value and for a probed $V_{ds}$ value what is that particular resistance. This is nothing but a DC resistance picked at every point in the voltage and then the average of that whatever the range we are interested in, if its 0 to $V_{dd}$. This is the range 0 to $V_{dd}$, we want the $1/V_{dd}$ will which will give us the average. It is basically a voltage weighted DC resistance and the average of that.

Then the average of the voltage weighted DC resistance is nothing but the switching resistance. This is what we will use it for our the equivalent RC model for any kind of a digital circuits. Let me use one more example, what it means is, if I have a resistance axis a resistance profile with respect to the $V_{ds}$ value of the transistor. In this particular sense I am going to use the NMOS transistors and then have a particular point from 0 to Vdd, we

know that when the voltage is $V_{dd}$ the NMOS transistor is in saturation, we will have a very large current and then we will have a very small resistance. Similarly, for an inverter circuit as the output node voltage drops the $V_{ds}$ values keeps dropping and somewhere at 0.7 it will change to the linear region and then till it is 0.

If we have actually looking for the switching resistance value for a range of 0 to $V_{dd}$ or $V_{dd}$ to 0. We might actually end up saying something like this the resistance values. I am just drawing an example not sure whether this is the real profile and what is the integration of 0 to $V_{dd}$ or $V_{dd}$ to 0 does it takes all these resistance values. It takes all these resistance values across this $V_{dd}$ value.

It is basically drawing integration is nothing but an area. It is basically taking an area of this and this particular range of $1/V_{dd}$, that I will actually get some kind of an average value, this becomes a switching resistance. Hope you understood this particular aspect of the switching resistance which we are going to incorporate into our RC equivalent model for the transistor-based circuit's.

This is what the definition says and if we are interested in the propagation delay falling or rising, this particular range will not be 0 to $V_{dd}$. This particular range of 0 to $V_{dd}$ it will not be like that it will be either $V_{dd}$ to $V_{dd}/2$ or 0 to $V_{dd}/2$ something like that. Where in the switching resistance is for 0 to $V_{dd}/2$ or $V_{dd}$ to $V_{dd}/2$, that is what I have written here.

For $t_{pdf}$ range is from $V_{dd}$ to $V_{dd}/2$.

$$R_{switch} = \frac{-1}{\frac{V_{dd}}{2}} \int_{V_{dd}}^{V_{dd}/2} \frac{V_{ds}}{I_{ds}} dV_{ds}$$

That is what the switching resistance from $V_{dd}$ to $V_{dd}/2$ and the DC resistance calculation, $dV_{ds}$ is likely to decrease because it is ranging from $V_{dd}$ to $V_{dd}/2$.

This is going to be decreasing that is why for every resistance is a scalar quantity and we will have a positive value of the resistance, we will never have a negative value of the resistance and that is why a negative sign is here to accommodate for the decreasing change in this integral expression.

This is what the expression for finding the switching resistance for evaluating the propagation delay, which is from output node voltage starts from $V_{dd}$ to $V_{dd}/2$, this is what the expression will be.

For calculating or for finding the equivalent switching resistance for the propagation delay rising the integral will start from 0 to $V_{dd}/2$. There we will not have this negative sign. Hope this is clear the definition of the switching resistance and then expression for the switching resistance is clear.

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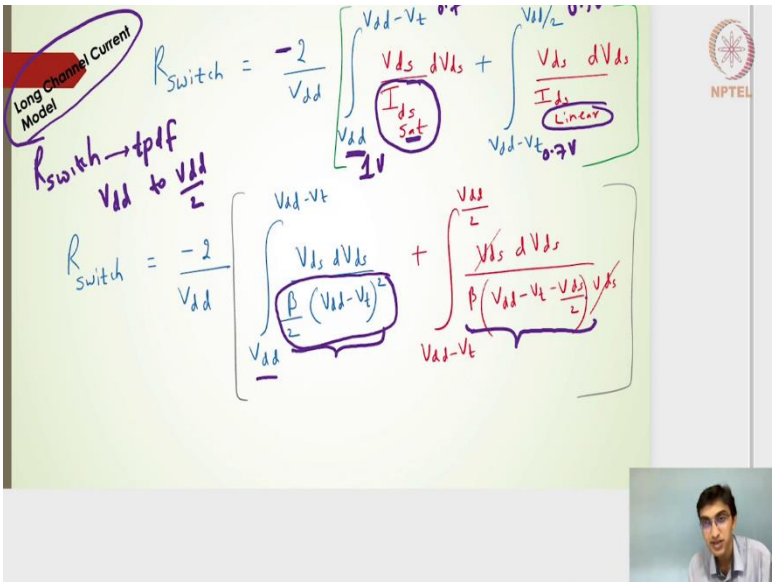


Let us try to calculate the switching resistance for the long channel current model and then we will try to calculate it for the short channel current model. $V_{dd}/2$ here for the range of $V_{dd}$ to $\frac{V_{dd}}{2}$ for the propagation delay falling so, I am trying to find the switching resistance.

For the propagation delay falling that means, this is the output range is actually nothing but $V_{dd}$ to $V_{dd}/2$.

$$R_{switch} = \frac{-2}{V_{dd}} \int_{V_{dd}}^{V_{dd}-V_t} \frac{V_{ds}}{I_{ds,sat}} dV_{ds} + \int_{V_{dd}-V_t}^{V_{dd}/2} \frac{V_{ds}}{I_{ds,linear}} dV_{ds}$$

In this I will have 1 by $V_{dd}/2$, the 2 goes here and there is a minus sign and then this particular range is now change from $V_{dd}$ to $V_{dd} - V_t$ and then $V_{dd} - V_t$ to $V_{dd}/2$ because here the current when we take the $V_{ds}$ by $I_{ds}$ in our expression for the switching resistance.

The current in this particular range of the voltage when it is within the $V_{dd}$ to $V_{dd} - V_t$ it will be the saturation region and when it is $V_{dd} - V_t$ to $V_{dd}/2$, in the last time also we had seen from 1 volts to 0.7 volts it will be in saturation region and then from 0.7 volts 2.5 volts it will be in the linear region.

We will have a separate current expression, that is why we will have to separate the integrals, we can easily write the expressions here as,

$$R_{switch} = \frac{-2}{V_{dd}} \int_{V_{dd}}^{V_{dd}-V_t} \frac{V_{ds}}{\frac{\beta}{2}(V_{dd} - V_t)^2} dV_{ds} + \int_{V_{dd}-V_t}^{V_{dd}/2} \frac{V_{ds}}{\beta(V_{dd} - V_t - \frac{V_{ds}}{2})V_{ds}} dV_{ds}$$

$$R_{switch} = \frac{-2}{V_{dd}} \left[ \frac{2}{\beta(V_{dd} - V_t)^2} \left( \frac{V_{ds}^2}{2} \right)_{V_{dd}}^{V_{dd}-V_t} + \frac{1}{\beta} \left( \ln \frac{V_{dd} - V_t - \frac{V_{ds}}{2}}{-1/2} \right) \right]$$

$$R_{switch} = \frac{-2}{V_{dd}} \left[ \frac{V_{dt}^2 - V_{dd}^2}{\beta(V_{dd} - V_t)^2} - \frac{2}{\beta} \left( \ln \frac{V_{dd} - V_t - \frac{V_{ds}}{4}}{V_{dd} - V_t/2} \right) \right]$$

$$R_{switch} = \frac{2}{V_{dd}} \left[ \frac{V_{dt}^2 - V_{dd}^2}{\beta(V_{dd} - V_t)^2} + \frac{2}{\beta} \left( \ln \frac{\frac{3}{4}V_{dd} - V_t}{V_{dd} - V_t/2} \right) \right]$$

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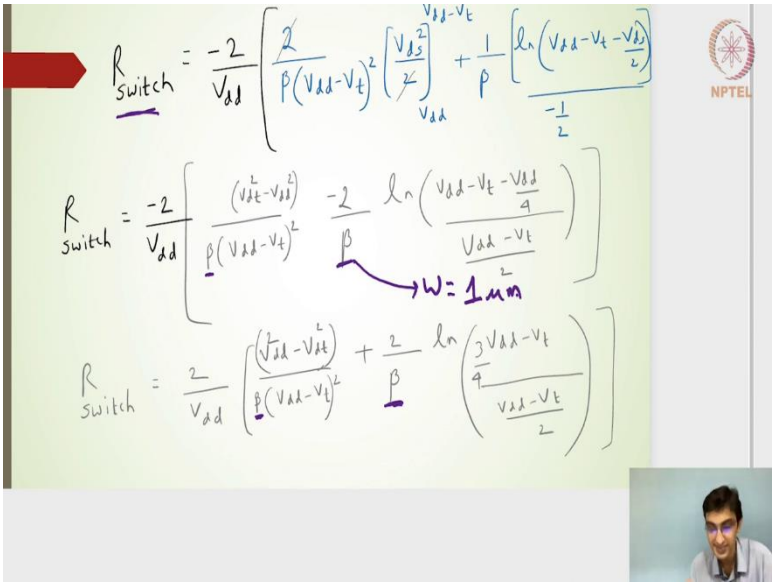

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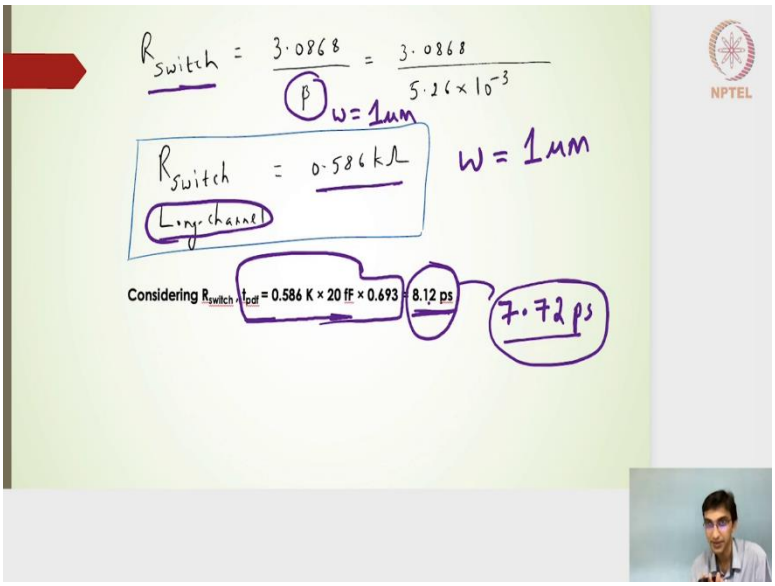


$$R_{switch} = \frac{3.0868}{\beta} = \frac{3.0868}{5.26x10^{-3}}$$

This β, width w is 1um,

$$R_{switch_{longch}} = 0.586K\Omega$$

This is my long channel switching resistance. This particular beta value and all those things this is nothing but for a w of 1 micron. I am keeping this 1 micron constant because in the NMOS transistors we have taken that current equation and then from the current equation we had to produce the voltage profile and from the voltage profile we had calculated the propagation delay falling, that propagation delay falling was for the width of 1 micron, keeping that width of 1 micron we want to benchmark whether the switching resistance makes some appropriate sense. In this particular slide what we have done is we have calculated the 0.586KΩ and if I use the Rswitching long channel resistance with that of a capacitive load of 20fF.

The propagation delay whatever the expression we had seent$_{pdf}$ = 0.586K x 20fF x 0.693 = 8.12ps, which is very very close to my long channel the transistor current based propagation delay falling was somewhere around 7.79 or 7.72 picoseconds. If I use the switching resistance of 0.586kΩ and treat it like an RC circuit my propagation delay falling for a step input it is coming close to the value of 7.72

picoseconds. No need to take the transistor current equation voltage profile and then the propagation delay falling and then finding out the value of 7.72, rather if I can find out if I have a switching resistance value take use that of 0.586xCxlog2 or 0.693 I will get this particular propagation delay falling value. Note that if the β are same for the PMOS and NMOS the propagation delay falling and rising will be equal.

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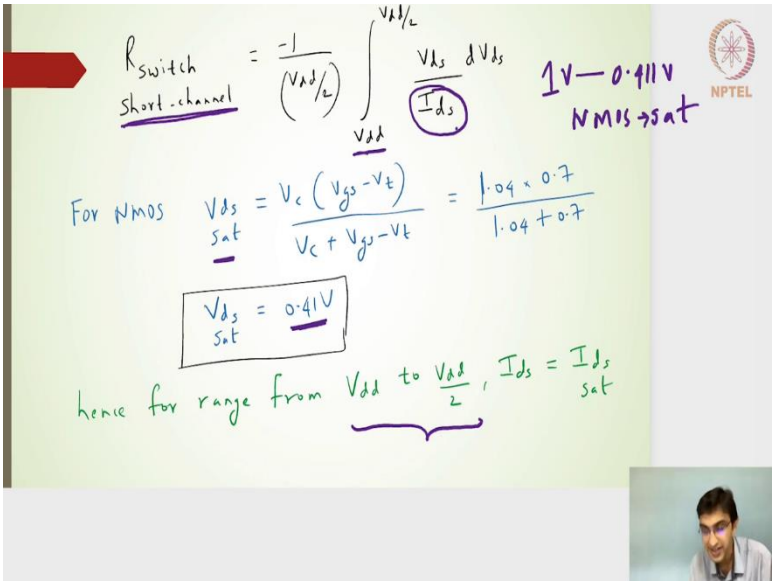


Hope that is clear, moving ahead what is the switching resistance, if I use the short channel current model. Now, remember that the propagation delay falling using the short channel current model was somewhere around 10.86 or 10.79 picoseconds.

What we need is to benchmark this, we will also calculate the switching resistance using the short channel current model and try to see that the Rswitching of the short channel multiplied by the c value and multiplied by 0.693 whether it comes closer to that particular value.

The short channel I will write the same expression of the switching resistance here it is

$$R_{switch} = \frac{-1}{\frac{V_{dd}}{2}} \int_{V_{dd}}^{V_{dd}/2} \frac{V_{ds}}{I_{ds}} dV_{ds}$$

$$\text{For NMOS, } V_{ds,sat} = \frac{V_c(V_{gs}-V_t)}{V_c+V_{gs}-V_t} = \frac{1.04x0.7}{1.04+0.7} = 0.41V$$

From 1 volts to 0.411 volts for the falling output the NMOS in the short channel will be in saturation region. That is what for the NMOS the $V_{ds}$ saturation value is 0.41 that is what we had arrived hence for the range of $V_{dd}$ to $V_{dd}/2$ we know that the $I_{ds}$ value which we have to take it is nothing but $I_{ds,sat}$

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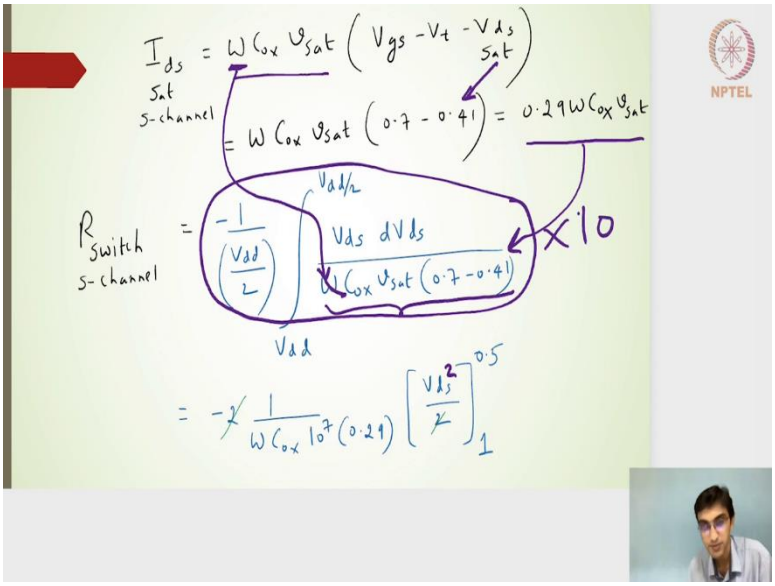


$$I_{ds,sat_{s-channel}} = WC_{ox}V_{sat}(V_{gs} - V_t - V_{ds,sat})$$

$$= WC_{ox}V_{sat}(0.7 - 0.41) = 0.29WC_{ox}V_{sat}$$

$$R_{switch_{s-channel}} = \frac{-1}{\frac{V_{dd}}{2}} \int_{V_{dd}}^{V_{dd}/2} \frac{V_{ds}}{WC_{ox}V_{sat}(0.7 - 0.41)} dV_{ds}$$

All these parameters are the constant values, I can easily take it out, what remains inside the integral is this $V_{ds}$. The solution of the integral will be,

$$= -2\frac{1}{WC_{ox}10^7(0.29)}\left[\frac{V_{ds}}{2}\right]_1^{0.5}$$

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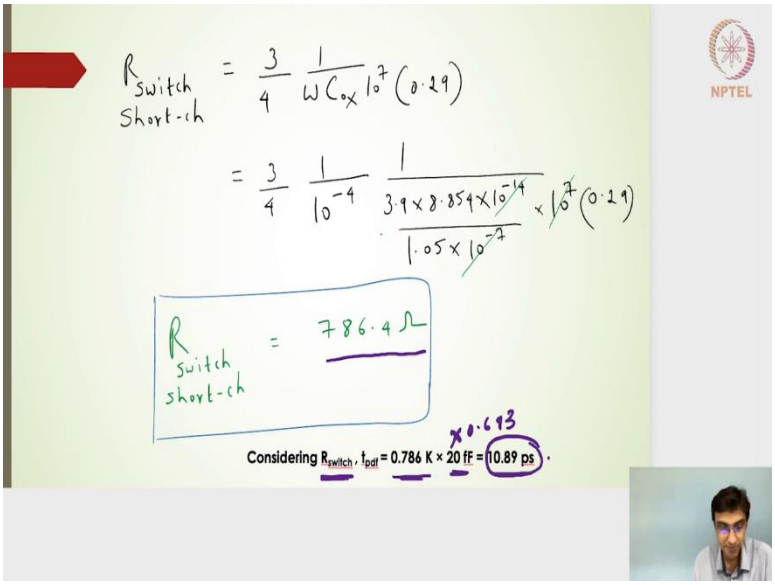


$$R_{switch_{s-channel}} = \frac{3}{4}\frac{1}{WC_{ox}10^{7}(0.29)}$$

$$= \frac{3}{4}\frac{1}{10^{-4}}\frac{1}{\frac{3.9x8.854x10^{-14}}{1.05x10^{-7}}x10^{7}(0.29)}$$

$$R_{switch_{s-channel}} = 786.4\Omega$$

For the short channel Rswitch is 786.4Ω, whereas for the Rswitching calculated or estimated R switching using the long channel current we got somewhere around 0.586kΩ. Individually, it says that the switching resistance estimated for the short channel current model is more and which is in a way it is correct. Because the current for the short channel model will be less than that of the current that has been estimated from the long channel current and if the current is less the resistance is likely to be more, that is what we have got 786.4Ω and if I use this particular switching resistance of the short channel,

$$R_{switch}, t_{pdf} = 0.786K \text{ x } 20fF = 10.89ps$$

Whereas, we have calculated using the transistor short channel current and then evaluating the output voltage expression the linearly decreasing profile and then putting the 0.5 volts, we had identified the $t_{pdf}$ using the transistor current equation as 10.79 or something like that. Here we are reaching very very close to 10.89 picoseconds which is very very close

to what we had earlier calculated. If I somehow find out the Rswitching resistance and multiply by that of the capacitive load and of course, multiplied by log2 if it is a step input, then I will likely to get the propagation delay falling for the digital transistor circuit, hope this is clear.

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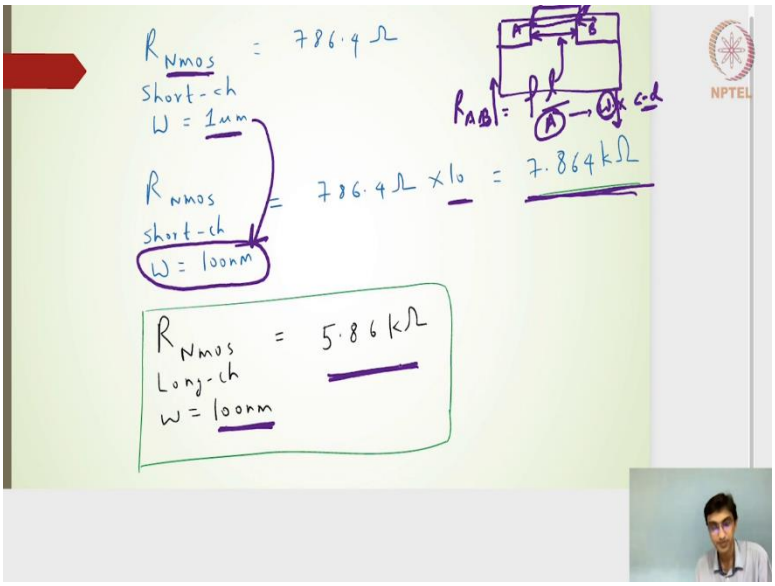


Just to summarize the short channel model the R the switching resistance for the NMOS transistor and all this while we had taken the switching resistance, we had considered the switching resistance of an NMOS transistor. Because when we apply the step input of 1volts the NMOS is on, the NMOS is operating, the NMOS is driving the output load capacitance, it is driving the discharging of the output load capacitance to 0 volts the PMOS is completely off.

The operating transistor is actually NMOS and we had used the switching resistance for the NMOS transistor we had used the current of the NMOS. Nowhere we had actually used the current of the PMOS.

$$R_{\substack{NMOS \\ short-ch \\ w=1um}} = 786.4\Omega$$

The width of the NMOS transistor if it is decreased from 1 micron to 100 nanometers its 10 times decrease, my resistance is likely to increase by 10,

$$R_{\substack{NMOS \\ short-ch \\ w=100nm}} = 786.4\Omega \text{ x } 10 = 7.864k\Omega$$

If I go back to the slide number 12, I will notice that this w was are of now this particular w is actually going into the denominator expression. If this w is 1 micron that has been changed to 100 nanometers effectively from 1 micron to 100 nanometers, effectively this whole switching resistance is likely to be x10 because w is anyways a constant which will come outside the integral.

Moving back, if it is decreased by 10 times, the resistance is going to increase by 10 times and intuitively if I look into the cross-sectional transistors what we are saying is, if this is the length and this is my gate side this particular width is increasing.

The channel cross section area if I consider this to be the terminals A and B, the $R_{AB}$ value and its cross sectional area which I can consider it to be an $R_{AB} = \rho l/A$, this particular area which is nothing w by the depth of the channel, this length is nothing but the channel length. This is this channel then area is nothing but the width multiplied by the channel depth. Which we are not considering what we are saying is, if this w decreases intuitively this $R_{AB}$ increases and that is what we are getting the switching resistance is increasing. It is increasing by 10 times if the width has decreased by 10 times.

In the long channel if I had calculated the long channel switching resistance for an NMOS transistors for 1 micron which was around 586Ω. If I use the width of 100 nanometers again the resistance is going to increase by 10 times, hope this is clear.

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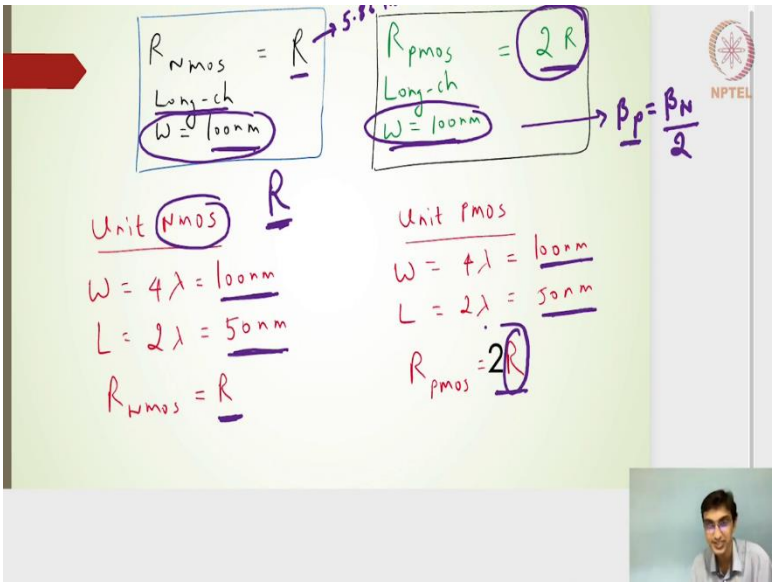


Moving forward just to summarize, $R_{NMOS}$ if I consider it to be an R long channel or whatever the short channel. Here I am taking the long channel as R which is nothing but for 100 nanometers, it is nothing but 5.86, instead of 5.86kΩ. If I actually say that this is an R value just a constant R, the PMOS long channel for the same dimensions it will be 2R and then the reason is very very simple the β if I am using the same width the β of PMOS will be half that of the β of NMOS.

If I want the β to be same, I have to make width of the PMOS to be twice that of the width of the NMOS, because the β is less, my current will be actually be less and thereby the current will be actually be less by half for the PMOS and thereby my switching resistance is going to be more, we exactly twice that off the NMOS.

What I mean by a resistance R here for an NMOS transistor is nothing but the lowest dimension NMOS transistor is going to give me a resistance of R which is nothing but 5.86kΩ. Why do I say the lowest transistor or the lowest dimensioned NMOS transistor because it is a unit NMOS, 100nm is the lowest width I can go 50nm is the lowest channel I can get in the 65nm technology node, that I will get a switching resistance for the NMOS transistor as R.

Similarly, for a unit PMOS transistor if I have the lowest PMOS transistor which is 100 nanometers and 50 nanometers of the channel length I will get a resistance of 2R, where

R is nothing but the unit NMOS resistance. I am having the PMOS switching resistance and then NMOS switching resistance trying to do a relative comparison.

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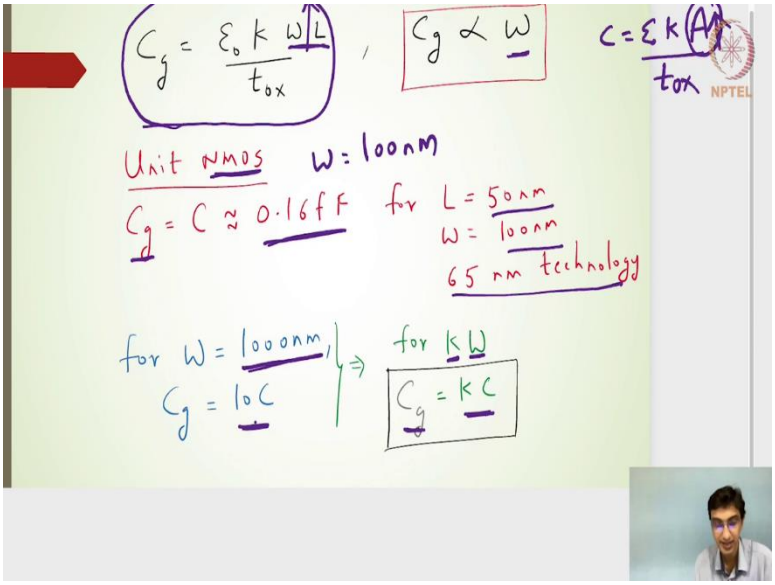


Moving ahead, what we need is basically a capacitive load, if I can also express the load capacitance in terms of a constant c, it will be much easier for me to understand, if the transistor width increases or decreases if it scales what should be the capacitive scaling effect.

$$C_g = \frac{\varepsilon_0 KWL}{t_{ox}}$$

Where $A = WL$

$$C_g \propto W$$

. If I consider a unit NMOS my w =100nm, if my w=100nm, the $C_g = 0.16fF$ for an L=50nm, w=100nm for a 65nm technology node.

For a w of 1 micron which is 1000 nanometers the w increases the area increases rather the w increases, the Cg value will also increase. The $C_g = KW$ if my dimensions, if the width increases is scales by K times, where W is the width of the unit NMOS, that means 100nm if it scales by K times, the gate capacitance also scales by K times. $C_g = 10C$ if w is increased or scales by 100 or 10 times.

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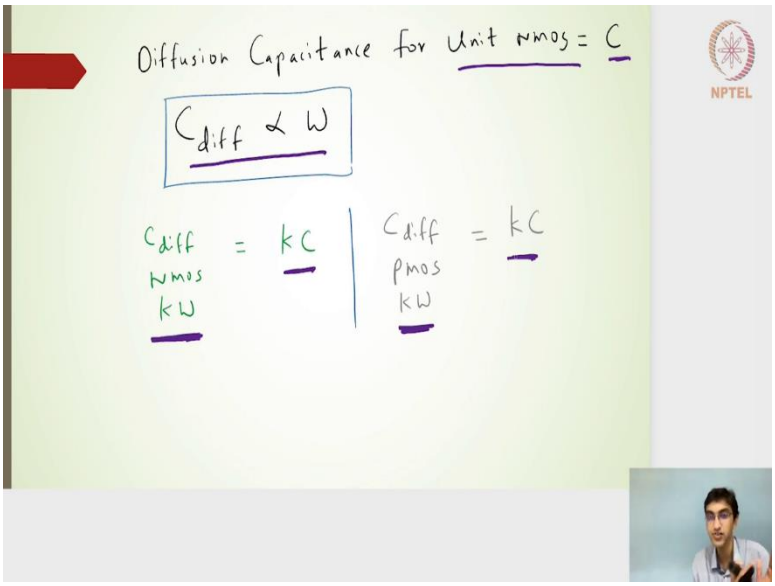


Diffusion capacitance also has a value very very close to that of the gate capacitance. If the gate capacitance is somewhere around 0.16fF the diffusion capacitance is also somewhere very very close, it turns out to be 0.14 or 0.13fF.

What we will say is that for the unit NMOS the diffusion capacitance I will consider it very very close to the C value the gate capacitance, to make our overall RC equivalent circuit very very simple to express. What we are doing is we are expressing the gate capacitance in terms of a constant variable Cdiffusion capacitance is also in terms of the constant variable C.

$$C_{diff} \propto w$$

If you see the diffusion capacitances or the depletion capacitances, if the w increases the area of the depletion capacitance also increases. The diffusion capacitance for an NMOS if it is K times more, $C_{\substack{diff \\ NMOS \\ KW}} = KC$, where C is nothing but the unit NMOS transistors gate capacitance or the diffusion capacitance value.

I can see diffusion capacitance of the PMOS if it is increases by k times, I will also get the same dimensions, the PMOS capacitance remains the same as that of the NMOS capacitances. Only the resistance for that same dimensions of the PMOS as that of the

NMOS the resistance is the switching resistance is half that of and the switching resistance is twice that of the NMOS switching resistance.

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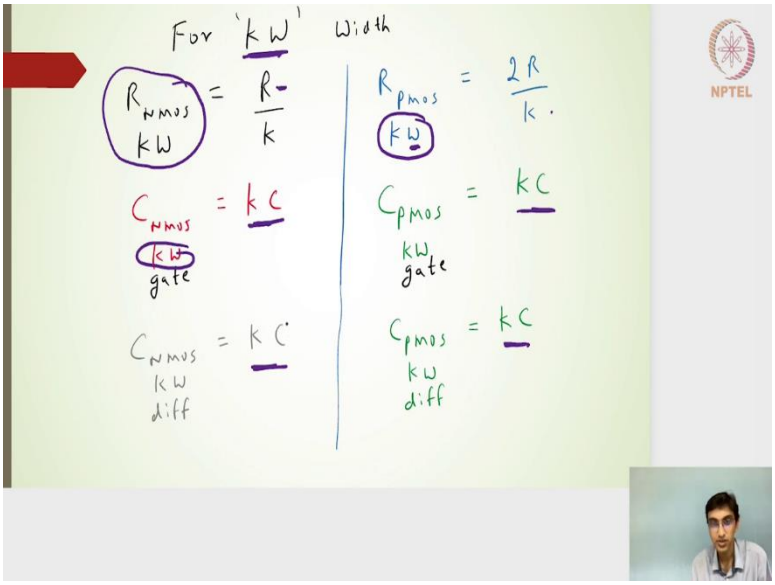


Just to summarize for the KW width NMOS switching resistance, if it increases will be nothing but the unit resistance that is for 100nm/K. For the PMOS for the W is nothing but 100 nanometers for the unit PMOS transistor it is nothing but 2R if it is scaled by k times if the width is scaled by K times it will be 2R/K.

Capacitance on the other hand for both PMOS and NMOS if it is scaled by K times the width of the transistor if it is scaled by K times the gate capacitances is nothing but KC PMOS also we will have the gate capacitance KC diffusion capacitance is also KC and the diffusion capacitance of the PMOS is also KC.

Just to summarize the switching resistance is different for PMOS and NMOS whereas, the capacitance remains the same for both of them if the width is scaled by K times. Overall, in this particular lecture what we had seen is how to evaluate the switching resistance for an NMOS using the short channel or the long channel current model.

Then we also validated, if we use that particular switching resistance and then multiplied by the capacitance load capacitance and then we get the values very very close to what we had estimated from the transistor current equations. Finally, if I want to express for a different width dimensions of the transistors we can express that in terms of R/K value as

a switching resistance or 2R/K value for the PMOS switching resistance and the or the diffusion capacitance and the gate capacitance can be expressed as KC.