Design and Analysis of VLSI Subsystems
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Lecture – 22
RC approximated delay

Hello students, welcome to this lecture on the RC approximation and then the delay estimation for the CMOS circuits. In this particular lecture we will see how do we model or approximate a transistor into an RC circuit. Before that going into that level we need to understand why is that the modeling very essential, in a sense that if you use the transistor itself in our case of an inverter a very primitive digital circuit.

What is the delay or the performance values and what kind of estimation methods we have to employs as to reach to that particular the delay parameters and to be very specific it will be the propagation delay parameters. Once we calculate that, how do we then model it appropriately into an RC circuit, that is what we are going to learn in this particular lecture.

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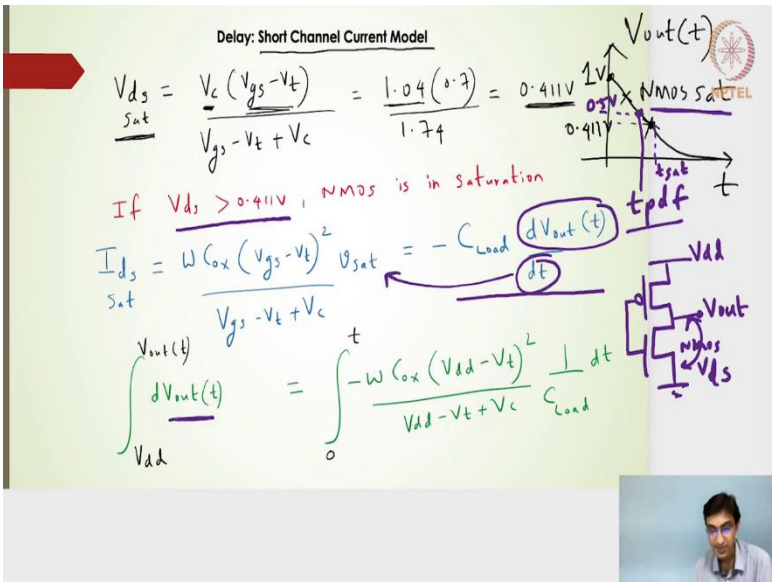

Moving ahead, we want to calculate the propagation delay especially the falling one, because we are again using the inverter where the NMOS transistor is operating in either linear or saturation region for which makes the output voltage to discharge to 0.

We are once again calculating the propagation delay falling for the same inverter circuit, but now we are using a different current model, we are using a short channel current model.

Now remember that in a short channel current model the V_{ds} saturation. V_{ds} saturation is a combination of the pinch off as well as the velocity saturated region.

What it means it is a combination, it is basically what we had said earlier it is nothing but equivalent to a parallel combination of the pinch off region and the velocity saturated region. V_{ds} saturation value for a short channel model turns out to be,

$$V_{ds_{sat}} = \frac{V_c(V_{gs} - V_t)}{V_{gs} - V_t + V_c}$$

This V_{ds} saturation value and we had seen this earlier also, the V_{ds} saturation value estimated from the short channel current model turns out to be actually less than the 0.7 volts. $V_{gs} - V_t$ for an inverter circuit where the inverter input is 1 volts of the V_{dd} value turns out to be nothing but 0.7, but V_c value it is around 1.04 as we had seen last time.

$$V_{ds_{sat}} = \frac{1.04(0.7)}{1.74} = 0.411V_{ds}$$

The 0.411 volts which is very far, I mean what it means is it is far less than that of the 0.7 volts. So, if I actually draw an axis here . If I draw a time axis here and let us say that this is my output voltage of the NMOS transistor in the inverter circuit, where the NMOS transistor is used in the inverter circuit.

While it actually drops in the long channel model we had got two profiles: a linear profile linearly decreasing profile output voltage profile I am talking about. It is a linearly decreasing profile and then exponentially decreasing profile. In this particular case, we have a some kind of a profile and then another profile this in the long channel model this point was 0.7 volts.

But, here it will be 0.411 volts starting from 1 volt. If the output node voltage is starts to 1 volts, that means the input to the inverter was 0 volts, the output was 1 volts and then the step input of 1 volt is applied at the input side that is when the output voltage will start decreasing.

When the output voltage is 1 volts we know that we will be able to analyze that the NMOS transistor will be in saturation. Whenever the output voltage is somewhere here we know

that the output voltage is above 0.411 volt, the NMOS transistor is in saturation, till it reaches 0.411 volts it is the NMOS transistor will be in saturation.

I am going to write this as NMOS is in saturation, which is in a way it is good because if I want to calculate the propagation delay falling, I do not have to go below this 0.411 volts. The propagation delay falling the voltage point to estimate the propagation delay falling is actually somewhere at 0.5.

I have to reach somewhere here and then this particular point will be the propagation delay falling, this point will be my 0.5 volts. That particular point on the voltage axis is 0.5 volts and that particular point on the time axis is actually propagation delay falling. Hope this is clear.

What it means is in the long channel current model while I was actually doing a transient analysis of the inverter circuit, we have to estimate the t saturation point and from the t saturation point we used to get the value of t_{pdf}. Here in the short channel current model, there is no need to calculate the t saturation point, because the t saturation point is way beyond the t_{pdf} point.

If I want to find out the t_{pdf} value, I can actually use this particular NMOS which is in saturation region, use that particular current equate it to the capacitor discharging current equation and then I should be able to do the integration and then find out the t_{pdf} value, that is what I have done here. Till V_{ds} from 1 volts V_{ds} or V_{out}. It is the same thing because in an inverter circuit we know that PMOS and NMOS if I draw this. This is my V_{dd} value this is my PMOS connected to the NMOS. This is my NMOS value and then this is my V_{out} which is nothing but the V_{ds} value drain and then the source.

Till V_{ds} > 0.411 volts, NMOS is in saturation. I will equate the I_{ds} saturation current equation which is nothing but,

$$I_{\substack{ds \\ sat}} = \frac{WC_{ox}(V_{gs} - V_t)^2 V_{sat}}{V_{gs} - V_t + V_c} = -C_{load}\frac{dV_{out}(t)}{dV_t}$$

If I do the integration on both the sides and take out this, dV_{out} on one side and then dt on the other side, I should be able to find the solution find the expression for V_{out}.

$$\int_{V_{dd}}^{V_{out}(t)} dV_{out}(t) = \int_{0}^{t} \frac{-WC_{ox}(V_{gs}-V_t)^2}{V_{gs}-V_t+V_c}\frac{1}{C_{load}}dt$$

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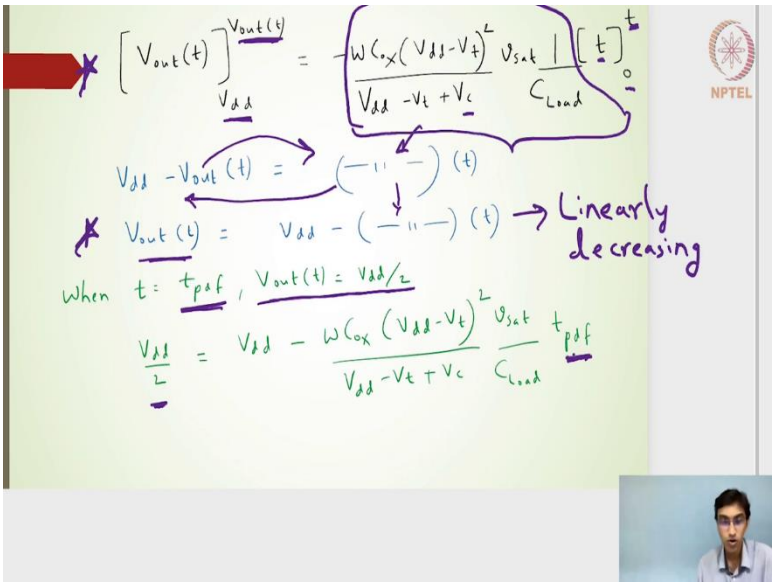

That is what I have done here.

$$[V_{out}(t)]_{V_{dd}}^{V_{out}(t)} = \frac{-WC_{ox}(V_{dd}-V_t)^2}{V_{dd}-V_t+V_c}V_{sat}\frac{1}{C_{load}}\,[t]_0^t$$

Then it reaches till the 0.411 volts. We will consider this to be a $V_{out}(t)$ for the time domain t, this is nothing but whatever is written here.

$$V_{dd}-V_{out}(t) = \frac{WC_{ox}(V_{dd}-V_t)^2}{V_{dd}-V_t+V_c}V_{sat}\frac{1}{C_{load}}(t)$$

$$V_{out}(t) = V_{dd} - \frac{WC_{ox}(V_{dd}-V_t)^2}{V_{dd}-V_t+V_c}V_{sat}\frac{1}{C_{load}}(t)$$

If I put $V_{out} = \frac{V_{dd}}{2}$ that particular time instance will be the propagation delay falling, that is what we get. If I put $V_{out} = \frac{V_{dd}}{2}$, the time instance is nothing but t_{pdf}. This particular expression or rather if I look into this particular expression V_{out} is equal to V_{dd} minus the constant values into t what it says is, it is a linearly decreasing profile with respect to the time, linearly decreasing profile, with respect to the time it is a linearly decreasing profile. There is no exponential profile here. We will need to calculate the propagation delay

falling, because the propagation delay falling is a point where the output voltage decreases to 0.5 and V_{ds} value the saturation value in the short channel current model it reaches well within that 0.5 volt.

The NMOS transistor is still in the saturation region, it changes from saturation to the linear region only at 0.411 volts, no need to get the exponential profile in the short channel current model to calculate the propagation delay falling. Hope this is clear.

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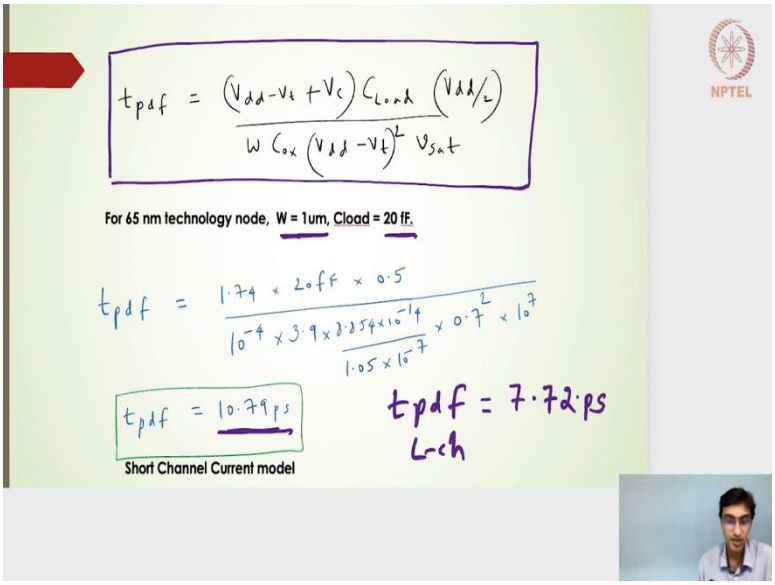

Moving forward, this is what the expression we have for the propagation delay falling for the short channel.

$$t_{pdf} = \frac{(V_{dd} - V_t + V_c)C_{load}}{WC_{ox}(V_{dd} - V_t)^2 V_{sat}}(V_{dd}/2)$$

If you are using the short channel model and taking the same parameters of w = 1µm and C_{load}=20fF.

$$t_{pdf} = \frac{1.74 \text{ x } 20\text{fF x } 0.5}{10^{-4} \text{ x } 3.9 \text{ x} \frac{8.854\text{x}10^{-14}}{1.05 \text{ x } 10^{-7}} \text{x } 0.7^2\text{x}10^7} = 10.79\text{ps}$$

We get the propagation delay falling in the short channel as 10.79ps. If you remember the propagation delay falling using the long channel model was somewhere around 7.72ps.

This one is 10.79ps and it is to some extents intuitively, what it says is the short channel current model takes little bit more amount of time for the capacitive load to discharge till 0.5 volts as compared to the long channel current, which is in a way it is intuitively correct which also signifies or reiterates that the long channel current, which is an ideal current is always gives the higher values for the same V_{gs} value or for the same V_{ds} value.

It gives a slightly higher values as compared to the short channel current model and the reasons we had seen earlier that it is due to the mobility degradation and the velocity saturation effect, where for the same V_{ds} value and the same V_{gs} value we will get the current to be lesser and because the current is lesser the discharging current.

The discharging rate with respect to time is also less and there by the capacitor takes more time to discharge from 1 volts to 0.5 volts. Hope you know this is clear.

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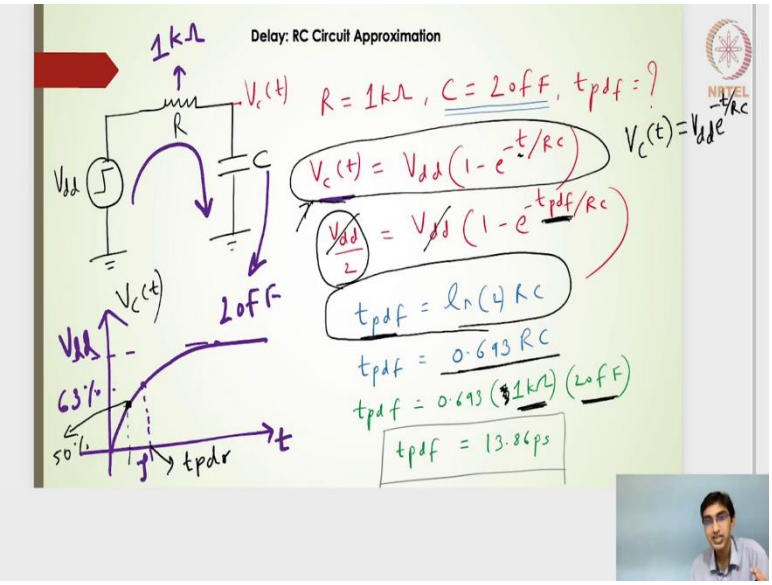

Till now what we had seen was the long channel current model and then the short channel current model and then giving the propagation delay falling of some values of 10.7. Let me go back and then see that 10.79ps.

Then the long channel current model gave us a value of somewhere around 7.72ps. What if I take just an RC circuit the C value is the same as what we had taken earlier the 20fF and this R value I am just taking a very simple value of 1KΩ and let us say that a step input of V_{dd} value is applied and then the capacitor starts charging.

Although, if I want to really estimate the propagation delay falling the capacitor should be discharging, but nevertheless, I think even if I use the same R and C values the propagation delay falling and then the propagation delay rising will be the same. Over the charging one the capacitor charging profile is nothing but,

$$V_c(t) = V_{dd}\left(1 - e^{-\frac{t}{RC}}\right)$$

Let me draw the profile and then we will see that what should be that point. If this is the particular exponential profile and this is the time constant, where it reaches to the 63% of the V_{dd} the maximum value. In this case the input voltage applied is V_{dd} and then this particular time axis we will get tau which is a time constant is the instance where the output voltage or the capacitor voltage reaches to the 63.3%, but what we need is actually the 50%. The 50% point where the capacitor voltage reaches this particular value is what we need the 50% of the capacitor voltage.

This particular point on the time axis is what we will say that this is propagation delay rising and if I use the same RC values it will be nothing but the propagation delay falling. Although in this particular equation this is the capacitor equation and the discharging profile will also be the very very similar. I will write the discharging profile once it is completely charged to V_{dd}, the discharging profile will be nothing but,

$$\frac{V_{dd}}{2} = V_{dd}\left(1 - e^{\frac{-t_{pdf}}{RC}}\right)$$

This would be the discharging profile and from the discharging profile we should be able to calculate the propagation delay falling. In this particular charging profile equation if I put the capacitor voltage as $\frac{V_{dd}}{2}$. This particular time axis will be the propagation delay rising. Although I have written is the propagation delay falling what I am assuming that taking the same R and C values it will be nothing but the propagation delay falling and the propagation delay rising will be equal.

We can take one of them, this particular parameter, if I put the values here. This V_{dd} and then this V_{dd} gets cancelled and then we will get,

$$t_{pdf} = \ln(2)\, RC$$

$$t_{pdf} = 0.693RC$$

$$t_{pdf} = 0.693\ (1K\Omega)(20fF)$$

$$t_{pdf} = 13.86ps$$

The short channel model gave us somewhere around 10 point, if I go back 10.79ps and the long channel model gave us somewhere around 7.72ps. If I take a simple RC circuit of 1KΩ and then the same capacitance of 20fF, I am getting 13.86ps.

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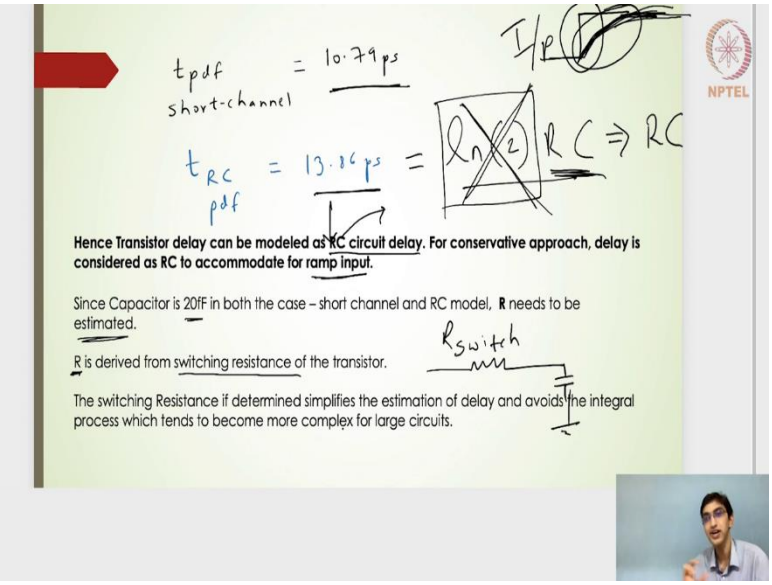

What do we conclude here? 10.79 is what I am getting from the short channel. RC circuit which giving me 13.86ps. What we are saying is if we can model a transistor, if I can model a circuit in this in the previous case it was an inverter which was actually discharging from V_{dd} to 0. If we can model that into an RC equivalent circuit.

Then if you are modeling to an RC equivalent circuit then finding out the propagation delay for an RC circuit is much much simpler then calculating it for a transistor, because in transistor I will have to write the current equations and then for getting the voltage expressions I have to do the integration of that and then find out the particular regions of the transistors and then put the value of the $V_{dd}/2$, so as to find out the propagation delay whether it is falling or rising.

Instead of that if I have an RC equivalent circuit where the c is nothing but the load capacitance. If I can find out an R value for a transistor whether it is charging or discharging. If you can find out an equivalent R circuit then it becomes much much easier for us to calculate the RC, the propagation delay falling or propagation delay rising.

The performance of the circuit, if we can make that circuit or if we can approximate that circuit into a series of RC circuits, for a larger CMOS digital circuits if we can approximate into a series of an RC circuits, then it becomes much much easier for us to calculate or estimate the performance or the delay parameters.

One more thing, this one was 13.86 we got because we had taken ln(2RC). This ln (2) component is kind of applicable when the input is a step input, when the input is going to the circuit or the inverter or the digital circuit is a step input.

This input is a step input. Generally what happens is if we have a step input given to an output of the inverter is actually cascaded to the (Refer Time: 18:50) stages and then so on and so on. In a million and billions of the inverter circuits which is used to design a system we will never have this kind of a step input applied to another circuit.

The output of the very first circuit will be in this particular case we have a ramp and then the exponential profile. This particular input profile is never a step input for the subsequently cascaded circuits. It is always some kind of a linear profile or an exponential profile which goes as an input to the next circuit. In that case to make conservative approach we take out this ln(2) the reason is very very simple, if the input is not a step input.

If it is something else, my delay the output of the circuit for which this particular input is given will be further delayed. In that circuit in that case to keep it very very simple yet a conservative approach we will remove this ln(2), that means we will get 69.3% of the RC we will remove it. We will take it the 100% of the RC value.

For an input voltage which has a ramp, the output voltage the delay estimation we will consider it to be a product of R and C, that is what I have written here. For conservative approach delay is considered to be an RC value to accommodate for the ramp input, the ramp input and not for the step input. We will not have a step input always, since the

capacitor is 20fF in both the case short channel in RC model R needs to be estimated, that is what we want we need to estimate an R.

If you look into the R value it is considered as a switching resistance of the transistor. What we are saying is, we will use the same capacitive load, we will use whatever is a capacitive load 20fF or 10fF whatever it is given. The transistor now based on its operating region we will call it, we will use the switching resistance of the transistors whether it is a PMOS or an NMOS transistors and use it to accommodate or incorporate in our delay model.

If I have a switching resistance, we will use this switching resistance and then the capacitance and then use it to either charge or discharge and then find out the propagation delay falling or rising. If the switching resistance, if determined simplifies the estimation of delay and avoids the integral process which tends to become more complex for the larger circuits.

Hopefully you have understood this it is quite clear. What we really want is from here on is finding out a switching resistance of the transistors which are used in the circuits maybe it is an inverter circuit or any other digital circuit. Find out the switching resistance and use the switching resistance along with the load whatever is a equivalent load capacitances associated with the output node voltage. Use that form a RC circuit and then estimate the propagation delay falling or rising for that particular equivalent circuit, so as to make it becomes a very simplified process.