Design and Analysis of VLSI Subsystems
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Lecture – 21
Transient analysis of CMOS Inverter

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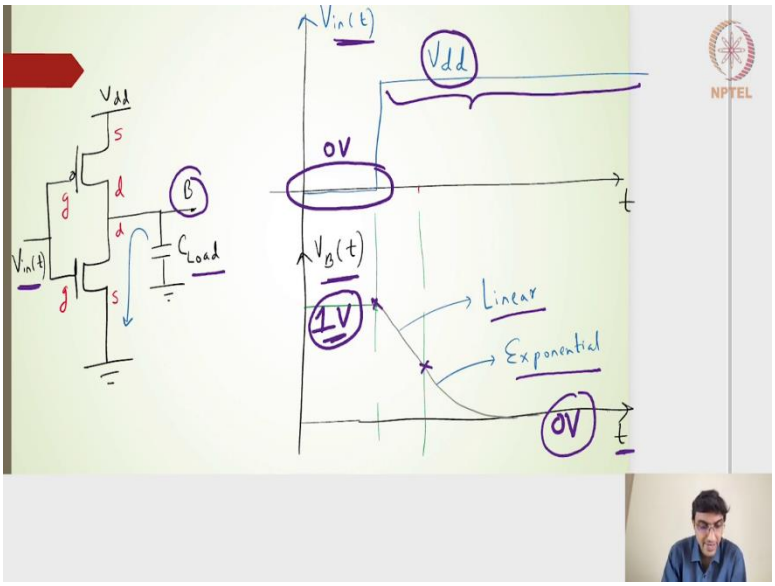

Welcome back students, this is what we have at this point of time, we have a load capacitance. This is the load capacitance and we have an inverter where the input voltage is given and we need to find out what is the output voltage profile with respect to time. Basically, we want to find out the transient analysis. What we need is, as I have drawn here the output the input voltage.

This is the input voltage and this is the output voltage V_B that is the voltage at the node B with respect to time domain and the x axis is the time domain. What we need is how is the output going to fall or how the output is going to rise. Remember that we have considered the input voltage as a step voltage. We need a step response.

The output voltage what should be the response for a given step input voltage. At this point of time I know although I have written it as a linear profile and an exponential profile do not worry about it at this point of time. We will understand what this linear profile in an exponential profile. It is very simple it is this particular profile starting from this particular

point to this particular point it is a linear line linearly decreasing line, output voltage profile and then from starting from this particular point it is an exponentially decreasing profile.

We will have to see how the capacitance discharges, how the capacitance is discharges given an input voltage here of V_{dd} how the capacitance at the output node that discharges. What in this particular profile there is one more important aspect, let me point it out.

When the input voltage is actually 0 or the digital logic 0, we know the inverter output has reached a steady state of 1 volts or a logic 1. Then as the step input is applied to V_{dd}volts to the V_{dd} value, it may be 1 volts or 5 volts whatever it is the output voltage of the inverter because the input voltage is now 1 the output should eventually reach to 0 volts.

That means, starting from 1 volts, as an initial condition it should go down to zero volts. At the steady state value it should eventually reach to 0 volts. The transition from 1 to 0 volts is our transient analysis and that is where we will try to extract the delay parameters. There is a delay here for this inverter circuit given an input voltage of 0 to 1 the change in the logic from 0 to 1 the output voltage does not change rapidly from 1 to 0.

It actually takes some time for the output voltage to change from 1 volts to 0 volts and that particular change in the duration of the time is what we will extract it or we will characterize it as the delay parameters. Hope this particular you know the intention of the inverter circuit and then extracting the delay parameters is clear, moving ahead.

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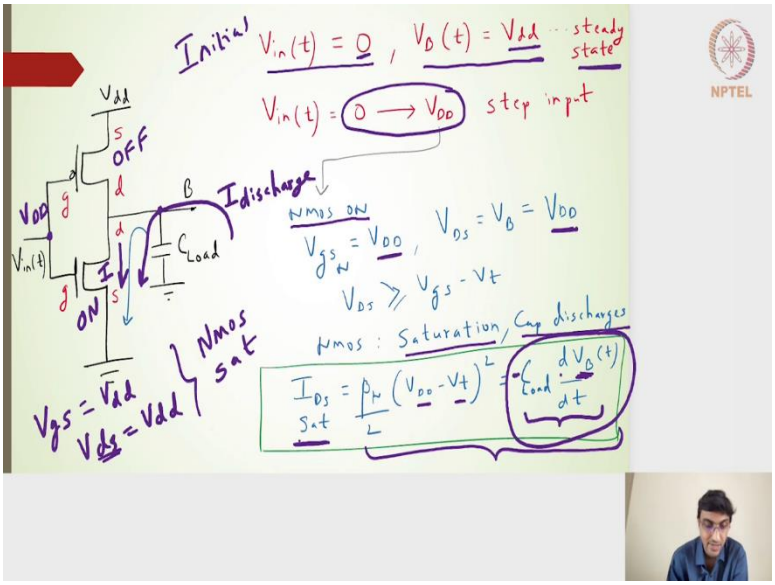

Let us begin with our discharging profile of the capacitors, our understanding of the discharging profile of the capacitor. If the input voltage is actually 0 that is the initial condition. My $V_B(t)$ the output voltage here is at V_{dd} that is at steady state for the previous condition and when the input voltage changes switches from 0 to V_{dd} that is the step input is applied I.

In that particular case, when the input voltage and at this particular gate when it is set to V_{dd} after applying that step input, V_{gs} value on the PMOS side is actually 0, there is a V_{dd} on the gate side, source side is also V_{dd}. This particular PMOS will be off. On the NMOS side this is V_{dd}, $V_{gs} = V_{dd} - 0$. This NMOS should be on because it is much much greater than Vt.

It has to be either in the linear region or the saturation region. For this particular analysis we will consider the long channel current model just to simplify the things. We will consider a long channel. In this particular lecture we will consider only the long channel right and not the short channel current model.

Moving further, NMOS is on that is what we have highlighted the $V_{gs,n} = V_{dd} - 0$, which is V_{dd}. When V_{in} voltage is 0 volts initially when it is at 0 volts, we know that the output voltage starts from V_{dd} and then it discharges to 0 volts. Initially at the time t=0 when the step input is applied, the input voltage is changing from 0 to V_{dd} the output voltage sees a V_{dd} value.

V_B is set to V_{dd}, that means the V_{ds} value is also V_{dd}. Now, I have in the time t=0, $V_{gs} = V_{dd}$, $V_{ds} = V_{dd}$ at time t=0. At time t=0 the NMOS is now operating under which condition. If $V_{ds} > V_{gs} - V_t$ then the NMOS should be in the saturation region.

It turns out that this $V_{ds} > V_{gs} - V_t$, NMOS turns out to be in operating in the saturation region. That is what I have written NMOS in the saturation region capacitor discharges with a current of the saturation current of the NMOS. The saturation current of the NMOS is nothing but Ids which is nothing but,

$$I_{ds_{sat}} = \frac{\beta_N}{2}(V_{dd} - V_t)^2$$

But the capacitance is actually discharging, that it should be the same. This is the discharging capacitance or discharging current. My ideas of the NMOS should be equal to that of the capacitor discharging current. That is what the capacitor discharging current is given like capacitance multiplied by the change in the voltage with respect to the change in the time, it is nothing but,

$$I_{ds_{sat}} = -C_{load}\frac{dV_B(t)}{d_t}$$

What it means is, if you know there is a minus sign here represents that it is a discharging profile. The overall value of this $-C_{load}\frac{dV_B(t)}{d_t}$ will be a positive value, because V_B is anyways decreasing, dV_B will give me a decreasing value or will give me a negative value and then here the negative here will neutralize it and then we will get a positive value. The current here I am looking at a positive current value hope this is clear.

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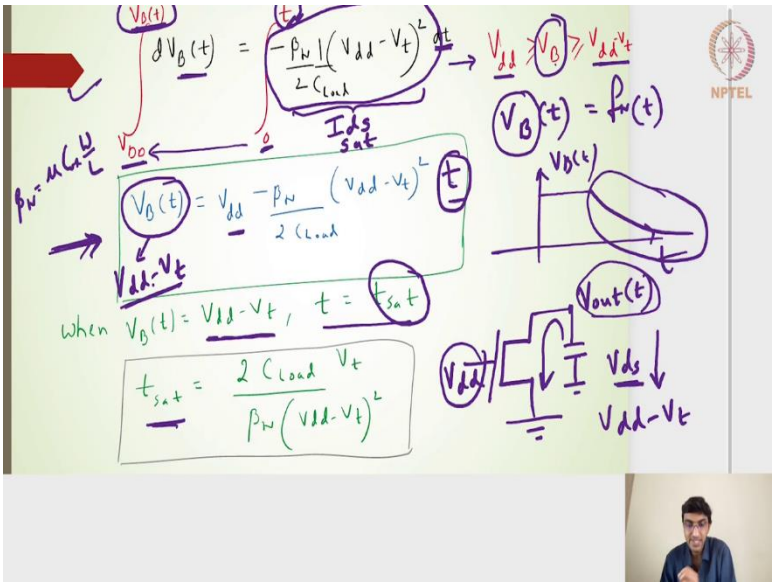

Moving ahead now, I have an equation of dV_B by dt is equal to nothing but the saturation current equation. What we really want is the value what is an or an expression for the output voltage V_B, this is what we want. We want an expression for $V_B(t)$ with respect to time. What we want is a output node voltage as a function of time, some kind of a function of time.

That I should be able to draw a profile of $V_B(t)$ and then I should be able to extract the parameters. It could be some kind of a profile earlier it was the 1 and then it will be something like this, this particular profile is what we want. In this case, we will integrate the earlier expression, let me go back a slide.

I have the saturation current and then I have this particular equation and we want a V_B expression. I will take some of the parameters I will take it into the left hand side and then try to integrate it, that I will get a expression for V_B, this is what we have done. Moving those parameters on the left hand side right hand side I will eventually get this particular parameter this particular equation.

Then, I will put an integral sign I need to understand what should be the limits. The starting limits anyways is V_{dd} for the output node voltage. Then at time t=0 that is where the output voltage is actually V_{dd}, right and have written a parameter here t.

$$\int_{V_{dd}}^{V_B(t)} dV_B(t) = \int_0^t \frac{-\beta_N}{2} \frac{1}{C_{load}} (V_{dd} - V_t)^2 dt$$

That means, that from 0 to t any particular point any particular time any particular instance of the time in the x-axis the value will be $V_B(t)$. I will start with the time t=0 that is where the output voltage is V_{dd}. Then I will have the integration done up till any particular time instance.

But knowing the NMOS characteristics knowing the NMOS transistor we know that, this particular equation, which is coming from the saturation current, this is actually coming from the I_{ds} of the NMOS of the saturation region. The saturation region is not going to stay for a long time the reason is very simple.

I have an NMOS transistor. I am drawing that and then the input is nothing but V_{dd}, the gate is nothing but V_{dd}, source is anyways grounded. The output voltage is having a capacitance it is initially charged to V_{dd}, but now it is continuously decreasing. The input voltage is fixed to V_{dd} it is a step input, the output voltage is continuously decreasing.

V_{ds} value is continuously decreasing, there will be a point where $V_{ds} < V_{dd} - V_t$. The saturation current profile is valid till this V_{ds} or $V_{out} = V_{dd} - V_t$. Below that the current of the NMOS will be in a linear operating region.

This particular equation the integral equation, this particular t value is applicable from 0 to a particular time till the NMOS is in the saturation region. Beyond that it will go to the linear region. In fact, this particular V_{dd} value you know this particular integral, $V_B(t)$ I should be able to calculate, I should be able to express $V_B(t)$ for a duration from V_{dd} to $V_{dd} - V_t$. This equation is valid till V_B is in between V_{dd} to $V_{dd} - V_t$. That is what I have stated here and I have emphasized there.

Getting from this particular equation, integral of this particular equation it is pretty simple. This particular portion on the right-hand side it is nothing but a constant value V_{dd}, V_t, β and again is nothing but if I write the $\beta_N = \mu C_{ox} W/L$. All of them are the constant parameters. C_{load} is again a constant parameter it does not vary with respect to the time, see the load capacitance is a constant with respect to the time, all these are constant.

I will have an integral of 0 to the constant multiply constant into dt, it is nothing but the constant value taken outside and then the t variable is given as,

$$V_B(t) = V_{dd} \frac{-\beta_N}{2C_{load}} (V_{dd} - V_t)^2 t$$

When $V_B(t) = V_{dd} - V_t$. This V_{dd} will come on to the right hand side and this is what the expression I will get. When this particular $V_B(t)$ expression is valid from V_{dd} to $V_{dd} - V_t$.

If I put at time t=0, I know that I will get $V_B(t) = V_{dd}$. Now, what should be the time where the saturation region of the NMOS ends and then it moves into the linear region. For that if I put $V_B(t) = V_{dd} - V_t$ the output as $V_{dd} - V_t$ then I should be able to find out the t value, where the NMOS transistor does the transition from the saturation region to the linear region, that is what I have done here. $V_B(t)$ if I substitute $V_B(t)$ the output voltage to $V_{dd} - V_t$, I will get a parameter I am calling or labeling it as the end of the saturation region as t_{sat}. This is what I will get,

$$t_{sat} = \frac{2C_{load} V_t}{\beta_N (V_{dd} - V_t)^2}$$

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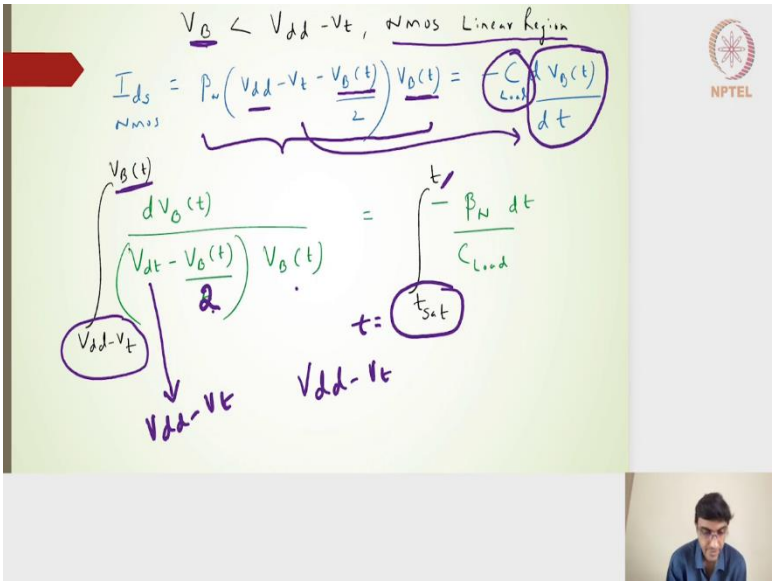

Hope this is clear at this particular point of time. Moving ahead, when the output voltage $V_B < V_{dd} - V_t$ that is when I read the NMOS linear region. My current expression is,

$$I_{\substack{ds \\ NMOS}} = \beta_N(V_{dd} - V_t - \frac{V_B(t)}{2})V_B(t)$$

The current of the NMOS transistor is now different it is not $\frac{\beta_N}{2}(V_{dd} - V_t)^2$.

Now, it actually is a function of the V_{ds} and V_{ds} is nothing but $V_B(t) - 0$. Whatever the V_{ds} value here is nothing but $V_B(t)$. My current equation of the NMOS transistor is nothing but a function of the output voltage of the inverter. That I am going to equate it to the discharging current of the capacitance, which is nothing but

$$I_{\substack{ds \\ NMOS}} = -C_{load}\frac{dV_B(t)}{dt}$$

Then if I do the similar integral, the initial value you know the integral of this if I take certain parameters on to the left-hand side and then right-hand side, I will get $dV_B(t)$ and then this particular whole expression onto the denominator side. I will get

$$\int_{V_{dd}-V_t}^{V_B(t)} \frac{dV_B(t)}{(V_{dt} - \frac{V_B(t)}{A})V_B(t)} = \int_{t_{sat}}^{t} \frac{\beta_N}{C_{load}}dt$$

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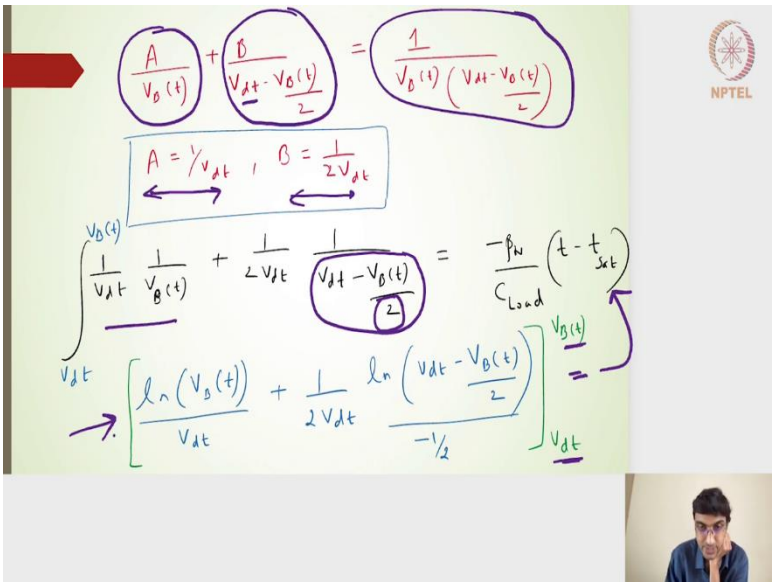

Moving further if I need to do this particular integration. Remember that if I go to the previous slide this is one. I am just trying to see a $V_{dd} - V_t$ is considered as V_{dt}, by taking partial products,

$$\frac{A}{V_B(t)} + \frac{B}{V_{dt} - \frac{V_B(t)}{2}} = \frac{1}{V_B(t)\left(V_{dt} - \frac{V_B(t)}{2}\right)}$$

What we want is basically, try to find out whether I can find out a separate fraction here and then separate fraction which will be equivalent to this right-hand side parameter. If I want to do this turns out that A and B value should be nothing but,

Where $A = \frac{1}{V_{dt}}, B = \frac{1}{2V_{dt}}$

$$\int_{V_{dt}}^{V_B(t)} \frac{1}{V_{dt}} \frac{1}{V_B(t)} + \frac{1}{2V_{dt}} \frac{1}{V_{dt} - \frac{V_B(t)}{2}} = \frac{-\beta_N}{C_{load}}(t - t_{sat})$$

This particular expression if I want to do the integration it turns out to be,

$$\left[\frac{lnV_B(t)}{V_{dt}} + \frac{1}{2V_{dt}} \frac{ln\,(V_{dt} - \frac{V_B(t)}{2})}{\frac{-1}{2}}\right]_{V_{dt}}^{V_B(t)}$$

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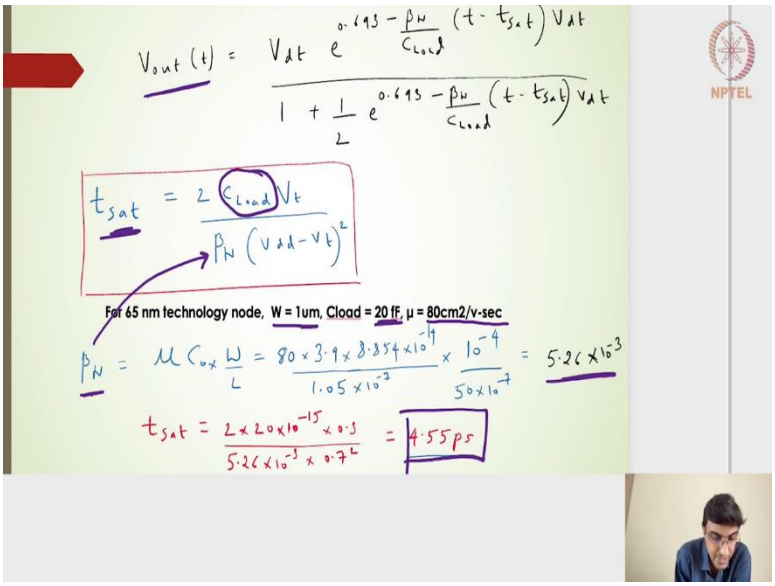

Finally, what I have done is, if you evaluate this and then if you find the solution turns out to be something like this,

$$V_{out}(t) = \frac{V_{dt} e^{0.693 - \frac{\beta_N}{C_{load}}(t - t_{sat})V_{dt}}}{1 + \frac{1}{2} e^{0.693 - \frac{\beta_N}{C_{load}}(t - t_{sat})V_{dt}}}$$

$$t_{sat} = \frac{2C_{load}V_t}{\beta_N(V_{dd} - V_t)^2}$$

For 65nm technology, $W = 1um, C_{load} = 20fF, \mu = \frac{80cm^2}{v} - sec.$

$$\beta_N = \mu C_{ox}\frac{W}{L} = \frac{80x3.9x8.854x10^{-14}}{1.05x10^{-7}} x \frac{10^{-4}}{5x10^{-7}} = 5.26x10^{-3}$$

$$t_{sat} = \frac{2x20x10^{-15}x0.3}{5.26x10^{-3}x0.7^2} = 4.55ps$$

t_{sat} value is when the output voltage starts from 1 volts reaches to 0.7 volts, up till that particular time NMOS transistor is in the saturation region.

One more point here is to understand or emphasize is the $V_{out}(t)$ here is basically an exponential profile because on the numerator side also we get an exponential profile on the denominator side also we will get an exponential profile, but it is basically a decreasing exponential profile. If I look into up till the t_{sat} value. If I go back to the previous set of slides.

This particular equation $V_B(t)$ it is nothing but $V_{dd} - V_t$ again. This is a particularly decreasing linear profile up till it reaches $V_{dd} - V_t$, after that it is an exponentially decreasing profile. The output voltage, now when the NMOS transistor is in saturation region we will get a linearly decreasing profile at the output side.

Then after that whenever the NMOS transistor is in the linear region we will get the output node voltage to be an exponentially decreasing profile. Coming back to this particular slide, where we got $t_{sat} = 4.55ps$ what should be the t_{pdf} value.

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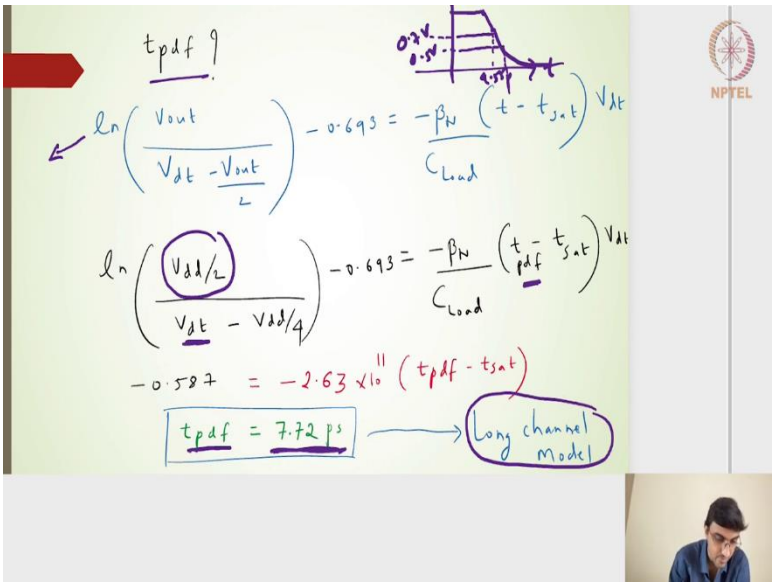

Now, t_{sat} will give me only 0.7 volts, this t_{pdf} value, if I consider the output voltage profile with respect to time it will start linearly and then till 0.7. This is a linear profile and this is where we have got the t_{sat} value as 4.55 picoseconds and then there will be an exponential profile.

This is the point of 0.5 volts, what we need to find out is an additional duration from 0.7 to 0.5 volts, where the output voltage reaches the 0.5 volts. This additional duration plus 4.55 will give me the overall propagation delay.

If I do this, I have an expression now, I have putting that particular expression as,

$$ln\left(\frac{V_{out}}{V_{dt}-\frac{V_{out}}{2}}\right)-0.693=\frac{-\beta_N}{C_{load}}(t-t_{sat})V_{dt}$$

This expression is coming from our the previous slide where we had the log the previous to previous slide. Where we had, this is the expression. I mean using this particular expression I am trying to find out the t_{pdf}, this is the slide we are in. Putting this V_{out} as $V_{dd}/2$, because that is where the propagation delay falling definition falls. This is where the output voltage reaches to the 50 percent of the maximum output voltage.

The maximum output voltage is anyways V_{dd} values, the 50 percent of that will be $\mathrm{V_{dd}}/2$.

$$\ln\left(\frac{\mathrm{V_{dd}}/2}{\mathrm{V_{dt}}-\frac{\mathrm{V_{dd}}}{4}}\right)-0.693=\frac{-\beta_{\mathrm{N}}}{\mathrm{C_{load}}}(\mathrm{t_{pdf}}-\mathrm{t_{sat}})\mathrm{V_{dt}}$$

$$-0.587=-2.63\mathrm{x}10^{11}\left(\mathrm{t_{pdf}}-\mathrm{t_{sat}}\right)$$

$$\mathrm{t_{pdf}}=7.72\mathrm{ps}$$

On this particular side it will be nothing but this will be the propagation delay falling minus of the tsat value. I will finally, get evaluate the tpdf as 7.72 picoseconds, according to the long channel model.

The propagation delay how we have expressed this is first we got the linear expression linearly following output voltage profile and then an exponential profile. Putting this in the exponential profile whatever the expression is if I put $\mathrm{V_{out}}$ is equal to $\mathrm{V_{dd}}/2$, I should be able to find out what is the time is nothing but $\mathrm{t_{pdf}}$.

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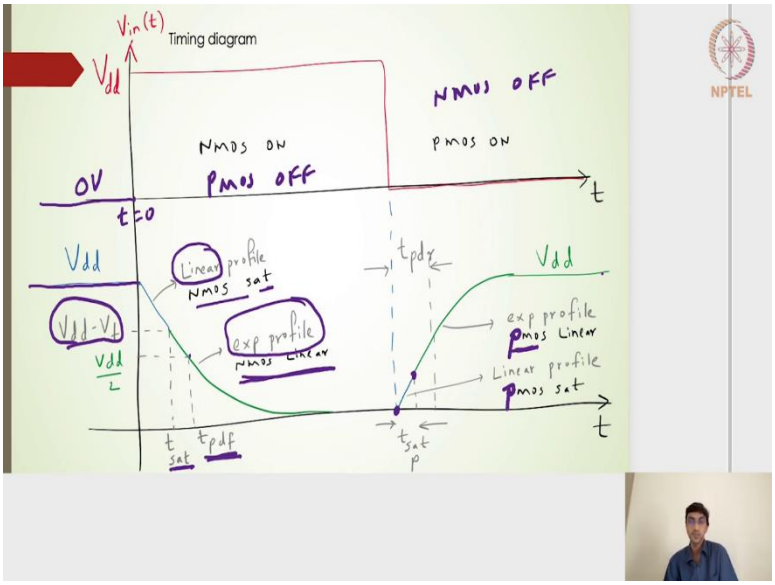

Looking at that overall timing diagram, coming back to what I meant about the linear profile. This is the linear profile, if I use a step input of at the input side 1 volt. That means, that before time t is equal to 0, the input was 0 and then at time t is equal to 0, we have the input to be V_{dd}, I will get the output voltage starting from V_{dd}, because at input to be 0 the output has reached a steady state of V_{dd} value.

Then till $V_{dd} - V_t$this is this particular value it will be in the NMOS will be in saturation region. I will use the saturation current, but finally the output voltage will be a linearly decreasing profile, after that it will have the NMOS region will be linear region.

We will get the current, we will use the linear region current, but the output profile will be an exponential profile exponentially decreasing profile and this particular point is our propagation delay falling till it reaches $V_{dd} - V_t$, we have this t_{sat} point. Similarly, on the PMOS side if we have the betas to be same what we will get is a very symmetrical profile.

Although it will start from the output voltage will start from 0 and then reaches to V_t value, up till that particular value we will have a linear profile, this will be the PMOS, the PMOS will be in saturation. When we have the input to be 0, the NMOS will be off and the PMOS to be on. Here in this case what we had was when NMOS was on for a step response for a step input PMOS will be off and when PMOS is on, that means when for the step input to go back to 0 PMOS will be on, but NMOS will be off.

This particular symmetrical profile for the output to charge back. This one was the output was discharging from V_{dd} to 0. Now, when the input voltage is 0 the output now charges back to V_{dd}. I will have the initially the PMOS to be in saturation region we will get the linearly increasing profile.

After that we will get an exponentially increasing profile when the PMOS region is in linear. So, sorry for that in the slide I have made a mistake this should be PMOS and not NMOS. Then we will get a profile till it charges to V_{dd}value. Hope this is clear at this particular point of time.