Design and Analysis of VLSI Subsystems
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Lecture - 02
Introduction to NMOS

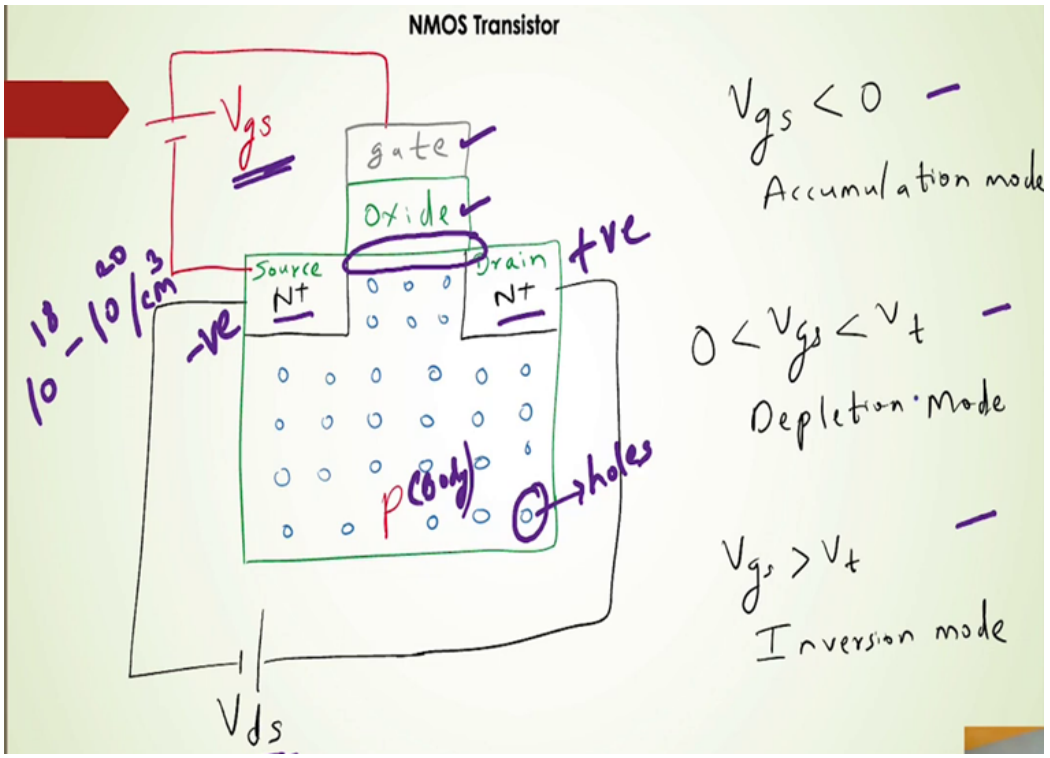

Figure 2.1: NMOS transistor cross sectional structure

Figure 2.1 show the cross-sectional structure of NMOS transistor consist of a gate, oxide and p-type body. Whereas for PMOS transistor an n-type body is used. In p-type body the majority carriers are holes, these holes are boron or gallium external dopants material and minority carriers are electrons. The minority carriers are generated randomly due to the thermal energy available at room temperature. Again, as the pure Si-crystal also possesses a few electrons and holes, therefore, the p-type Si-crystal will have a large number of holes (majority carriers) and a small number of electrons (minority carriers).

The n^+ dopants are formed with the process of implantation towards the surface corner of the p-type body structure. Doping concentration of this n^+ dopants is around 10^{18} to 10^{20} per cm^3. The n^+ dopants as the larger concentration and it's doped with phosphorous or arsenic material. Thus, a small corner wells of n^+ is diffused on this particular cross-sectional area of

the p-type silicon material. These wells are named as source and drain terminals. The source terminal sources the majority carriers and drain terminal drains away the majority carriers. As source generates the majority carriers and these majority carriers are collected at the drain side. But there does not exist a channel (or no path for majority carriers to move from source to drain end) connection between the source and drain side. An electric field or potential difference is applied at the drain to source side, even then there is no direct channel for the majority carriers to move to drain end. But there will be a very minimal path for the current to flow. Thereby, electric field does not have much force to attract the majority carriers from source side to the drain side.

The electric field which is created by the potential difference of V_{ds} is a lateral electric field. Initially an electric field of gate to source voltage V_{gs} is applied, but this electric field is a vertical electric field. Depending upon the magnitude and polarity of gate bias, there are 3 different modes of operations that is accumulation mode, depletion mode and inversion mode.

In the accumulation mode, when $V_{gs} < 0$, that is a negative potential difference is applied between the gate and source terminal as shown in figure 2.2. Due to negative potential at gate terminal, the majority carriers (holes) present at p-type body are accumulated towards the semiconductor oxide interface. This is known as accumulation mode. In this mode of operation, a channel is not formed from source to drain. Thereby the electrons cannot flow.

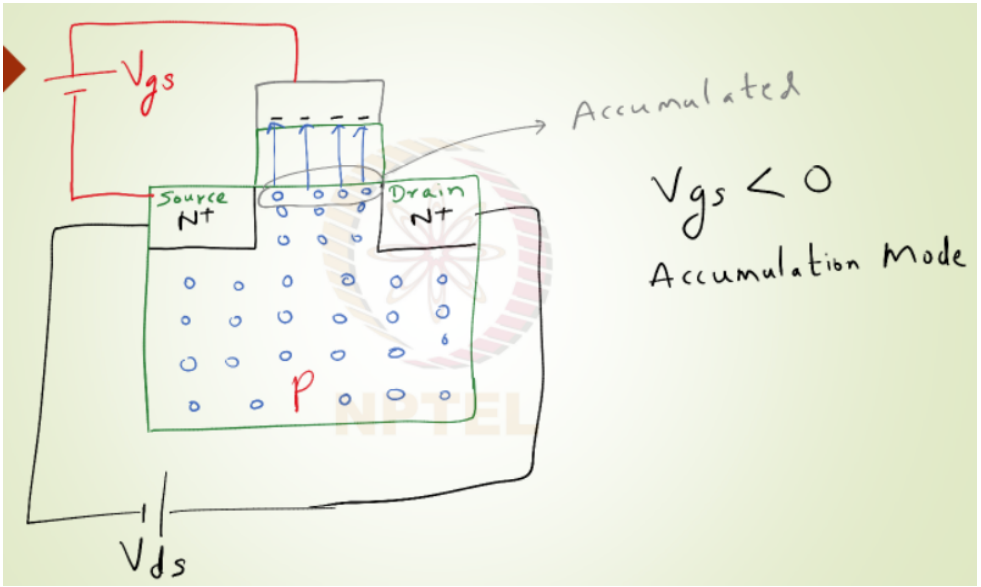

Figure 2.2: NMOS structure – Accumulation Mode

In the depletion mode, when $V_t > V_{gs} > 0$, where V_t is called as the threshold voltage as shown in figure 2.3. The majority carriers (holes) in the body are repelled from the region directly beneath the gate, resulting in a depletion region forming below the gate. Whereas the minority carriers (electrons) in p-type body are attracted near the oxide interface. But a small positive voltage is not sufficient enough for the minority carriers to attract at the oxide interface. This is called as depletion mode.

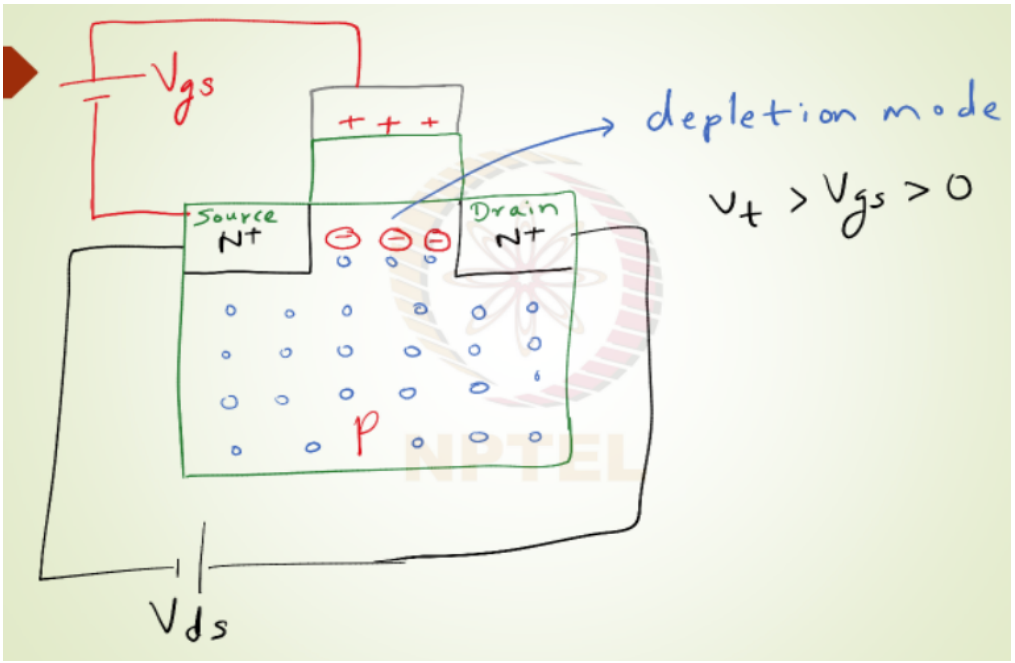

Figure 2.3: NMOS structure – Depletion Mode

The last mode of operation is inversion, when $V_{gs} > V_t$ as shown in figure 2.4. The positive potential at the gate side is going to attract this minority carriers of the p type and forms the electric field and this makes the channel intact. This particular channel forms a path connecting the source to the drain and allows the majority carriers of the source through this path to enter into the drain side. The minority carriers forming the conducting path and this path allows the free electrons. Free electrons from the source side move to the drain side and thereby the direction of current is from drain to the source I_{ds}. This conductive path of electrons in the p-type body is called the inversion layer.

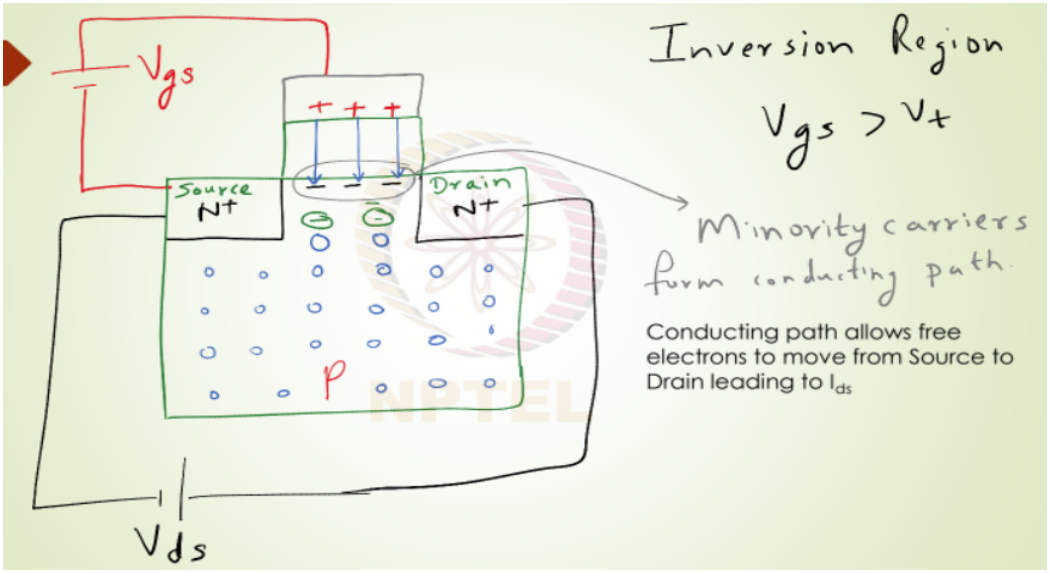

Figure 2.4: NMOS structure – Inversion Mode