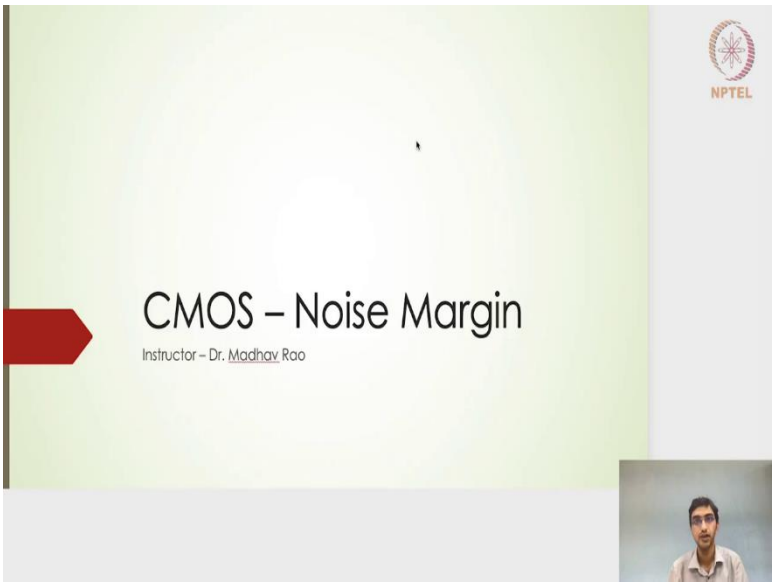
Design and Analysis of VLSI Subsystems
Dr. Madhav Rao
Department of Electronics and Communication Engineering
International Institute of Information Technology, Bangalore

Lecture – 18
Noise margin characteristics of inverter

(Refer Slide Time: 00:15)



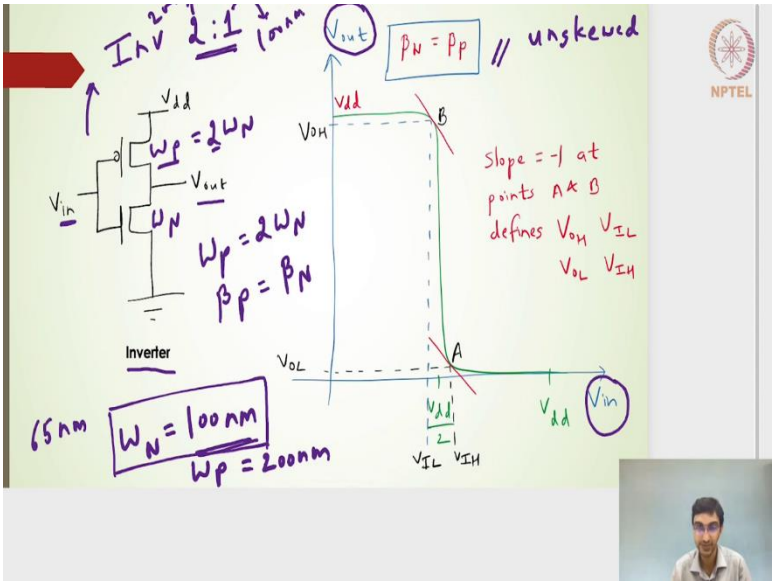
Welcome to this particular lecture, but we will be looking at the Noise margin. Noise margin as such is very important for the CMOS and for the digital and analog circuits. The reason is once we can characterize the noise margin, once we can calibrate the noise margin we should be able to put our input within that particular noise margin, so that we will get the discrete output.

Noise margin as such is a characterized or a calibrated, you know allowable range for the input to get a discrete output. In a sense it is that particular range where we can allow some kind of a mistakes or we can allow some kind of a noise signal, but yet to get a discrete output. In this particular lecture what we will see is how do we evaluate or how do we characterize the noise margin from a given circuit.

What we will do is from a given circuit? We will try to find out the transfer characteristics and then from the transfer characteristics we should be able to determine the noise margin characteristics for that particular circuit. We will take a very simple example what we have been doing, we have been using the inverter as a primitive digital circuit and we had

already gone over the transfer characteristics and from there we should be able to characterize the noise margin.

(Refer Slide Time: 01:57)



This is what we have a very primitive circuit. Let me take out my pointer this one and this is what we have been using the inverter as our very first level of the digital circuit, given an input we should be able to find the output. What we had seen is the transfer characteristics. We are kind of very familiar with the transfer characteristics. Transfer characteristics once again trying to reiterate it is nothing but the output voltage versus the input voltage how does it behave. So far you know and $V_{dd}/2$ turns out to be our threshold voltage for the inverter, that means, that anything lower than $V_{dd}/2$ I should be able to get the output voltage higher and anything lower than $V_{dd}/2$ I should be able to get the voltage the output voltage lower.

This is what the transfer characteristics we have defined and in this particular transfer characteristics the PMOS and NMOS, the width of the PMOS and then the width of the NMOS. What we have taken is the width of the PMOS is equal to twice that of the width of the NMOS and according to the long channel current model it should be able to get the betas of the PMOS to be same as that of the NMOS and thereby what I have said is the betas are same, that means this is an unskewed inverter.

That is what I am writing here it is an unskewed inverter because this is the inverter circuit and that is the reason why we get the threshold voltage to be $V_{dd}/2$ when we apply the

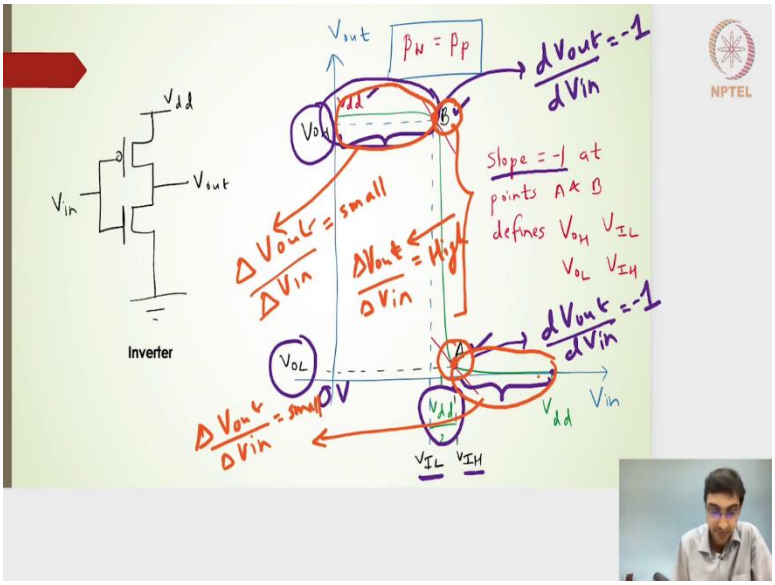
real voltage of Vdd and on the other side we apply a real voltage of 0. The threshold voltage for an unskewed inverter will be $V_{dd}/2$.

In another case what we also say it is the twice that of the NMOS generally what we say is if I am going to make a lowest size transistor in whatever technology node. In this case I am going to use let us say 65nm technology node. The lowest size NMOS transistor, of course will have a channel length of 50nm the width will be the lowest width what we can design is for 100nm.

We are taking the 4:2 ratio of the width and then the length. This turns out to be 100nm this will be the lowest width of the NMOS transistor that we can design. To get the unskewed inverter now the lowest width of the PMOS turns out to be nothing but 200nm. In this particular case what we can also say is I mean the way to represent the lowest size the width dimensioned the inverter could also be 2:1 because the PMOS width is twice that of the NMOS width.

We can also represent this inverter whenever we are writing we can also say that this is nothing but 2:1 inverter, what it represents is the PMOS width is twice that of the NMOS width and then because it is the lowest the primitive inverter. The size could be 200nm and then this is nothing but 100nm. In the textbooks and most of the times you will see 2:1 inverter what it really means is nothing but the width of the PMOS is 200, the width of the NMOS is 100nm. The channel length is for both of them is 50nm. When we are looking at the transfer characteristics of the inverter we get certain points like the $V_{dd}/2$.

(Refer Slide Time: 06:15)



$V_{dd}/2$ which is nothing but our threshold voltage and then of course, we have this V_{dd} points and then this particular point which is nothing but the 0 voltage. This is something we had already seen in the transfer characteristics of the inverter in addition to that I have added 2 more points A and B here. B and A and I have said that this is the slope is -1 at this 2 particular points.

Basically, these two points are the points on the transfer characteristics profile of the inverter, where the slope at this particular point is -1. The slope in fact represents the change in the output voltage with respect to the change in the input voltage is minus 1 and then that is same for both here. Again, the change in the output voltage to the change in the input voltage at this particular point is -1.

What it really means in this particular profile and then in this particular region of the transfer characteristics if the slope is -1 those points will be our A and B and there will always be a unique point in these two particular regions. In this particular region if I really want to find out the slope is -1 I will get a unique point B and of course in this particular region if I find out the point where the slope is -1 I will get a unique point that will be point A.

Now, these points A and B will actually define certain 4 new parameters which will help us to characterize the noise margin. Now these 4 parameters are called the output voltage low V_{OL} represents the output voltage and L represents the low level of output voltage V_{OH}

represents the output voltage high H represents the high and the corresponding parameters on the input side. Input voltage low and input voltage high hope this is clear.

Now, coming back to the slope of -1. If I look into this particular region above the point B this particular region I am talking about let me pick up a new color and then this particular region I am talking about and then this particular region I am talking about.

In this particular region the change in the output voltage with respect to the change in the input voltage. As the input voltage keeps on increasing the output voltage changes very very minimal, it turns out to be very very small.

Similarly, here in this particular region the change in the output voltage with respect to the change in the input voltage is also very very small or low. In this particular region of the transition region what we call it as a transition region which is coming from those intersection points of the NMOS and PMOS saturation current, this particular region where we get the output voltage and the input voltage.

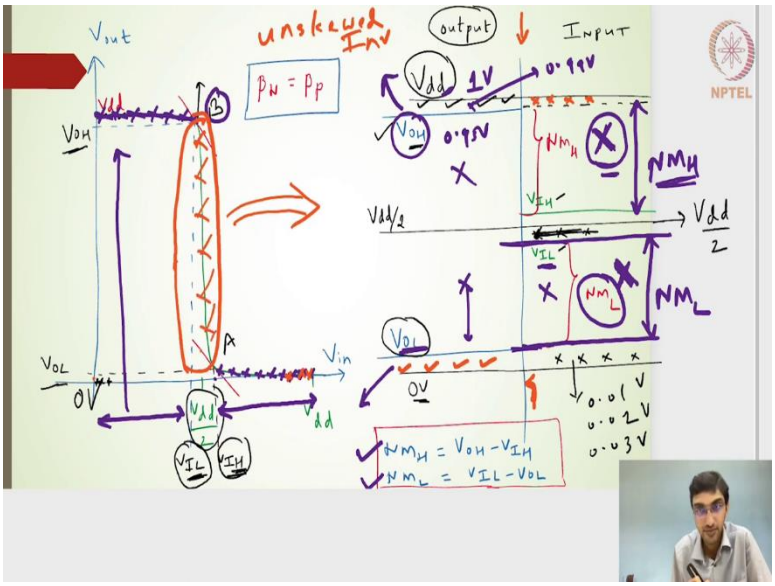
If very small change in the input voltage, I will get a very large change in the output voltage, I am going to write it as very high. The noise margin especially the parameters V_{OH}, V_{OL}, V_{IH} and V_{IL} is actually defined between these two points A and B where the slope is going from small to high and then again from high to low we will get the corresponding points B and A right.

If I choose the point B it is actually the slope for this particular transfer characteristics changes from small to high and we want to capture the point B where the slope is actually minus 1, it is not small enough and it is not high enough it is actually -1.

Similarly point A here, that particular point where the slope of the transfer characteristics changes from high to low and point A is actually the slope of -1 where it is not high enough and it not small enough and that is how it has been defined. The points A and B are defined as the slope of -1 which will be able to characterize the noise margin.

That is how the definition of the noise margin has come or rather I will say that the definition of those the output voltage level high low and input voltage level high and low that has been derived from or deduced from. Where the slope is actually minus 1 because on either side the slope is very very small or the slope is very very high.

(Refer Slide Time: 11:27)



Coming back to this particular transfer characteristics. We have this particular transfer characteristics of the inverter where it is the betas are same, that means it is an unskewed inverter. It is an unskewed inverter and that looking at the transfer characteristics I can easily state that this is an inverter digital circuit and then that is what the transfer characteristics represents.

On the right-hand side, we have the output and input voltage levels drawn, from the transfer characteristics what we really want is actually this particular output and input voltage level characteristics. From the voltage level characteristics then I can actually define the noise margin. The output and input voltages what I have done is, I have divided into two segments.

This is my division line I have just drawn a line here this particular blue line. This particular line is what I have I am considering and I have drawn because it is a voltage level. I have drawn a 0 volts level and then I have drawn a V_{dd} level. That is what the output and input level I have drawn the 0 volts level from the output region and input region and V_{dd} level on the output and input region from those slope of -1.

This is point B and this is point A we got 4 parameters 2 on the output parameters and then 2 on the input parameters. The V_{OH} which is very very close to V_{dd}. That is what I have drawn V_{OH} on the output region and then V_{OL} on the output region that is very very close

to the 0 volts. This is the 0 volts line and that is why it is very very closer to the 0 volts line. I have completed the output region levels.

What are the 4 output region levels V_{dd} 0 and in between V_{OH} and V_{OL}. On the input side I have anyways drawn V_{dd} level I have anyways drawn 0 voltage level I need the 2 of the input low and input high parameters. This one I will draw it which is very very close to this $V_{dd}/2$.

I am going to draw a $V_{dd}/2$ lines, this is my $V_{dd}/2$ line and it is because it is an unskewed inverter it is actually falls very very symmetrically. Symmetrical in the sense V_{IL} and V_{IH} points are actually symmetrically placed on either side of $V_{dd}/2$. This is my V_{IH} and this is my V_{IL}.

Looking at this particular output and input region or input and output voltage levels what we can say is if my input voltage I am going to extend this line on the input side the V_{OL} and then V_{OL} and V_{OH} line if my input is somewhere here I am pretty sure that my output will be here.

I have drawn 4 crosses. I will also make a equivalent number of tick marks there. What it means is if my input voltage level is very very close to 0 volts, that means, there may be a point of 0.01 or 0.02 or whatever you know 0.03 volts which is less than this V_{OL} value.

It is very very clear that somewhere here at the input side if I get these points I am pretty sure that the output voltage will be very very close to V_{dd}. That is what the transfer characteristic says the output levels is very very close to V_{dd} and that is what from the transfer characteristics we get. This x points is actually mapping to the output side, the tick mark points which is very very close to the V_{dd}.

Similarly, at the input side if I put a different color, let me see at the input side if I get my input points very very close to the V_{dd}, that means that is very very close to the V_{OH} level then I am pretty sure that the output will be very very close to the 0 volts. Looking at the transfer characteristics if the input points are somewhere here very very close to the V_{dd} then I will get my output values to be very very to be 0, somewhere this particular point it states that the output voltage is actually 0.

The transfer characteristics and then the input and output voltage region says that by default if my input levels to the inverter is very very close to 0 volts my output will be almost V_{dd} values and if the input levels is very very close to the V_{dd} values the output will be anyway 0. That is by default. What if, now the question is what if I have some points somewhere here at the input side if it is somewhere here what should be my output voltage.

Now, the noise margin low is defined as V_{OL} and this particular region of V_{IL} and V_{OL}, that means this particular region and then this particular region where we have defined our V_{IL} and V_{OL}. This particular region is called the noise margin low and then similarly this particular region is called the noise margin high. Noise margin low because it is basically on the lower side of the input and noise margin high it is on the higher side of the input.

If my points is actually falling in this particular region. Noise margin low because of this transfer characteristics any point here is likely to give me this is basically this point noise margin low is nothing but V_{IL} and below V_{IL}.

This is the region where I will actually get my output, now this particular region where I will actually get the output somewhere here. V_{IL} is actually defined by point B. Any input in this particular region is likely to give me the output point somewhere here which is actually very very greater than V_{OH}, that means this is very very closer to V_{dd}.

Similarly, if my input points is actually somewhere in between in this noise margin high region, that means that is actually defined by V_{IH}, this particular region. My actually output values lie somewhere here which is actually closer to very very close to 0 volts. What it means is the noise margin high and noise margin low it is the allowable input range where my input signals can still lie somewhere here.

But still I will get an output a definite and a discrete output somewhere in this particular region based on the whether the input signal is in the noise margin high or the input signal is in the noise margin low. It is an allowable input range for which I will get an output voltage still a satisfied digital or a discrete output voltage, now output voltage can be either Vdd volts or rather I can say it as 1 volts or if $V_{OH} = 0.95$.

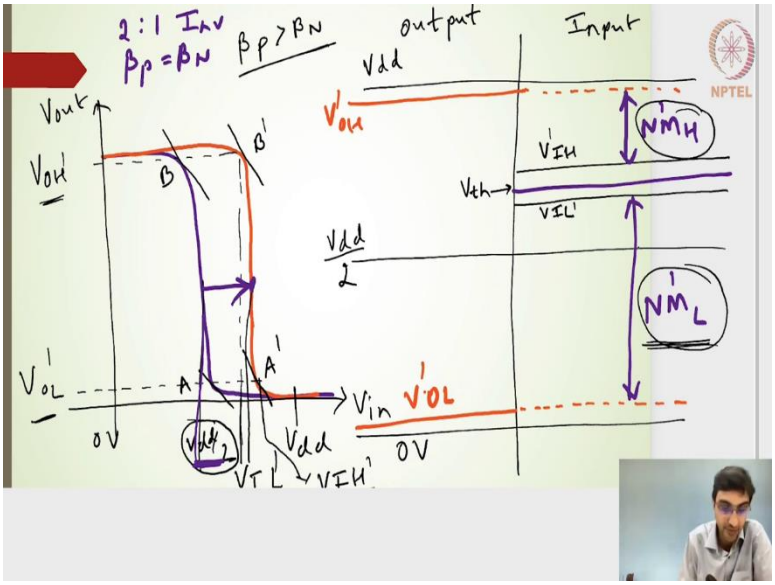
I can get an output voltage somewhere close to 0.99 or 0.98 or 0.97, but it is still very very close to 1 volts and if I have some input range here it does not give me a point somewhere

here and if my input range is somewhere here it does not give me a point somewhere here. It actually gives me a point very very close to the 0 volts.

That is the importance of the noise margins especially for the digital circuits and this is very very useful in terms of designing a mixed signal circuit where we have a digital component coming from the analog component. The analog component is fed to a digital component and then in that sense if the analog signal gives me somewhere here I still should be able to get a digital output. That is the reason why this noise margin is of importance.

The noise margin high as I had said earlier it is nothing but the difference between the V_{OH} and V_{IH} and a noise margin low is nothing but V_{IL} and the difference between this particular line and this particular line which is nothing but $V_{IL} - V_{OL}$. This is an empty slide. What it means is I am likely to draw something here I am going to draw something here.

(Refer Slide Time: 21:32)



What we had seen is for a 2:1 inverter that means, that my $\beta_p = \beta_N$ for an unskewed inverter we had the transfer characteristics and I am going to draw the transfer characteristics which is nothing but like this and transfer characteristics is nothing but V_{out} and then V_{in} and then let me say that this is my V_{dd} value and then this is my 0 volts value and somewhere here this is my $V_{dd}/2$.

If I change my $\beta_p > \beta_N$. In that sense my width of the PMOS is much much higher than that of the NMOS it is not only 2 times this is the width of the NMOS, but it is much much higher. That I will get a skewed inverter now. With the skewed inverter as we know the transfer characteristics is likely to change the transfer characteristics is going to be shifted towards the right and then this is what I am going to get.

If I further write this particular value is will be my threshold voltage and it will not be $V_{dd}/2$ it will be something else and then if I want to draw my B and A points where the slope is minus 1 that is also likely to change. Let me draw this on this particular point. This is my point B and then this is my point A for the skewed inverter and then similarly this will be my point B dash and this will be my point A dash. A dash and B dash are the slope, are those points which defines the V_{OL} V_{IH} V_{OH} and V_{IL}.

If I look into this B dash parameters B dash parameters which will give me the new points which will give me output high dash and this particular line which will give me V'_{IL}. Similarly, points A here will is likely to give me V'_{OL} and this particular point line I am going to draw it as V'_{IH}.

Earlier we had V_{OH} V_{OL} V_{IL} and $\mathrm{V_{IH}}$. If I go back to the previous slide we had this $\mathrm{V_{IL}}$ $\mathrm{V_{IH}}$ we have $\mathrm{V_{OH}}$ and $\mathrm{V_{OL}}$. Now, going further with the skewed inverter we now have all those parameters with the $\mathrm{V'_{OH}}$ $\mathrm{V'_{OL}}$ $\mathrm{V'_{IH}}$ $\mathrm{V'_{IL}}$, these are different points alright.

If I draw my input output region. I am going to draw this input and output region and then I am going to draw the $\mathrm{V_{dd}}$ line. This is my input and this is my output hope you are able to see this and I am going to draw my input and output region with $\mathrm{V_{dd}}$ line and then with 0 voltage line.

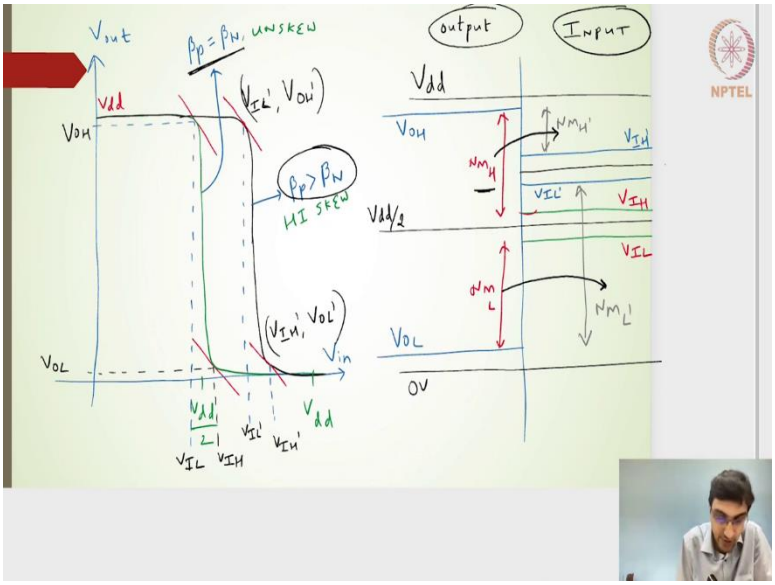
Earlier my threshold voltage when it was an unskewed inverter $\beta_{\mathrm{p}} = \beta_{\mathrm{N}}$ and my threshold voltage was $\mathrm{V_{dd}}/2$ This is my $\mathrm{V_{dd}}/2$ line, now the threshold voltage has been moved to some other value. This is my new threshold voltage and I have drawn it above $\mathrm{V_{dd}}/2$ because from this particular region we know that it is $\mathrm{V_{dd}}/2$ is this unskewed line this particular region and then this particular region this has been shifted it right.

It has been shifted. What it means is my threshold region, that threshold input side or threshold voltage is above $\mathrm{V_{dd}}/2$ and that is why I have drawn this above $\mathrm{V_{dd}}/2$. My $\mathrm{V'_{IL}}$ and $\mathrm{V'_{IH}}$ has also been shifted right and it should be on either side of this threshold voltage.

This is my threshold voltage V_{th} is this and this will be my V'_{IH} and then this will be my V'_{IL} and to further complete on the output side I have this V'_{OH} and on the output side low side I will have V'_{OL}. This is my extending line and if I complete this the noise margin, now is this noise margin higher and then a dash because it is for the skewed inverter and then similarly here noise margin low and I will say that dash because it is for the skewed inverter and not for the unskewed inverter.

The noise margin high and noise margin low has changed. The noise margin low apparently has increased and noise margin high has apparently decreased.

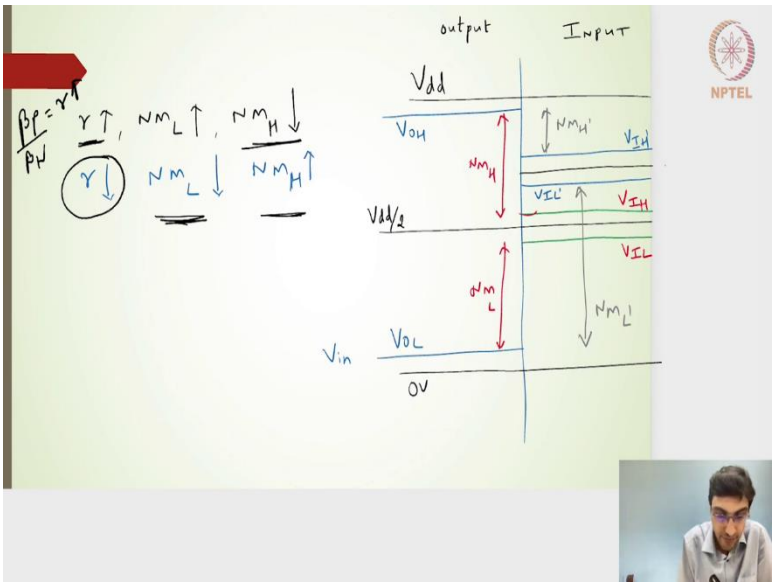
(Refer Slide Time: 27:35)



If I go further this is what is for the 2 transfer characteristics when the $\beta_p = \beta_N$ and skewed one and then the other one is $\beta_p > \beta_N$ which we had seen in the last slide. I have put both the slides and both the input and output regions together and because if you look it at once it may be a little bit overwhelming and that is why I have drawn that previous slide.

But this slide is nothing but if you look into this output and input regions it is nothing but two of these lines, two of the transfer characteristics parameters rather the noise margin parameters which we have put it together. Looking at it noise margin high has been decreased and noise margin low has been increased with respect to an unskewed inverter. What it signifies is as I actually skew.

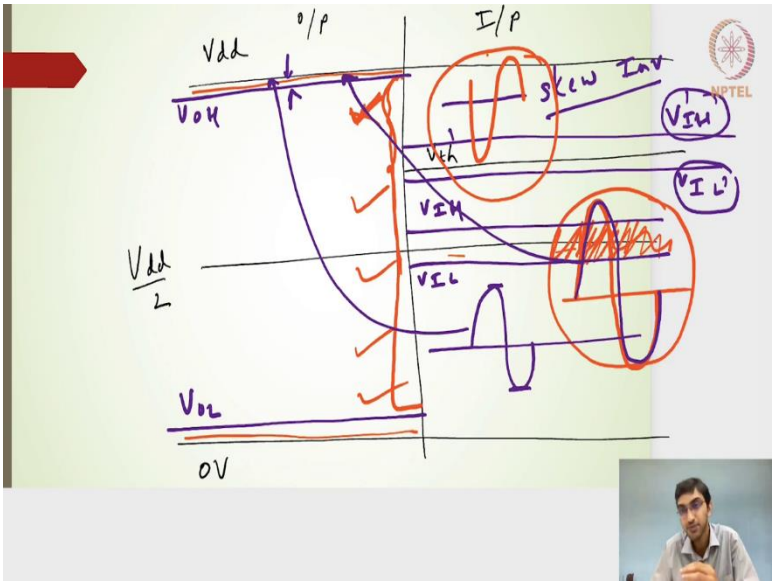
(Refer Slide Time: 28:35)



If I increase the skewing ratio, that means that my β_p/β_N is that is this skewing ratio and if it increases the noise margin on the lower side is going to increase the noise margin on the higher side is going to decrease. Similarly, it will have a very symmetrical effect if the skewing ratio is decreased, the noise margin lower side will decrease and noise margin higher side will increase.

Now, what is the advantage of this? The advantage here is if I know let us say, I pick up an unskewed inverter and then in the unskewed inverter, let me go back to the unskewed inverter if I can find out or rather let me draw. Let me draw a new design, that is what I have done I have got a new slide.

(Refer Slide Time: 29:42)



I am going to draw the input output characteristics of an unskewed inverter, that means that it is going to lie on V_{dd} this is my output and then this is my input and this is my 0 voltage line, this is exactly symmetrical $V_{dd}/2$. I will pick up another pointer showing that this is my V_{IH} and then this is my V_{IL}.

I am going to write it as V_{IL} and then V_{IH} and then this is going to be my V_{OH} and then this is going to be my V_{OL}. Tomorrow if I have a signal like this which falls in this particular region then I am pretty sure that I am going to get an output somewhere here in this particular region of V_{dd} and V_{OH} for the inverter, which is good. So, if I have any kind of a noise signal whatever frequency it is, but its amplitude is limited within this particular region that is perfectly fine.

But let us say that if I have a noise signal, which is crossing this transition region like this, this particular region the transition region gives me any points at this particular output range. If I go back to my transfer characteristics, I have taken the slide number 3. Any point any input voltages within this particular transition region, I can actually get any output values in this particular region.

Going back to where we were. What it means is if I have some kind of a points here in this particular region I will actually get, I will not be able to get a defined output level, I may get a point somewhere here, I may get some point here, I may get some point here, I might

get some point here or somewhere here, it is not a defined one right. I will not get a defined range somewhere in between here it could lie between V_{OH} and V_{OL}.

Which is not good for the circuit, we have not taken or accommodated this particular noise which we have not characterized it or calibrated properly to give a valid output signal. What it means is if I get this particular input signal then I will have to change or I will have to design my circuit such that my threshold range is here. This will be my V_{th} and the symmetrically I will write V'_{th} and then V'_{IL} and then the corresponding V'_{IH}.

I will have to change my dimensions or the width of the PMOS such a way that I will get this Vth dash value and then corresponding V'_{IL} value and V'_{IH} value high enough such that this particular input signal level is accommodated. If I can accommodate that then I know that any input signal here in this particular region should give me a definite point somewhere in the output range. I need to skew my inverter.

Similarly, if I have more input signal at the higher side here. Let me pick up another color more input signal at the higher side then I should have a skewed inverter of course but on the lower side.

I will probably use a low skew inverter to accommodate this particular changes, that really depends on the input characterization. In the input characterization in the sense if we know that the input signal that has been applied to the inverter has more noise signal at the lower side then I can easily make the high skew inverter.

But if we see that there are more noise signal that has been applied to the input side on the higher side that means, that along this particular regions then we can make it a low skew inverter. That is the advantage of skewing and that has been highly been used in the digital circuit design as well as in the mixed signal circuit design.

Hope you have understood this. What we started was an unskewed inverter draw the we anyways understand the transfer characteristics and then from the transfer characteristics we were able to design the noise margin. The noise margin is nothing, but allowable range for which we will get a definite output signal closer to V_{dd} or closer to 0 volts for an inverter and you know if there is an input signal which is falling on the lower side and if we want to accommodate it we can actually change the width of the PMOS or the NMOS

transistors and then make it appropriately such that the noise margin is being accommodating the input noise signal.