Design and Analysis of VLSI Subsystems
Dr. Madhav Rao
Department of Electronics and Communication Engineering
International Institute of Information Technology, Bangalore

Lecture – 17
Bad CMOS Buffer – Part 2

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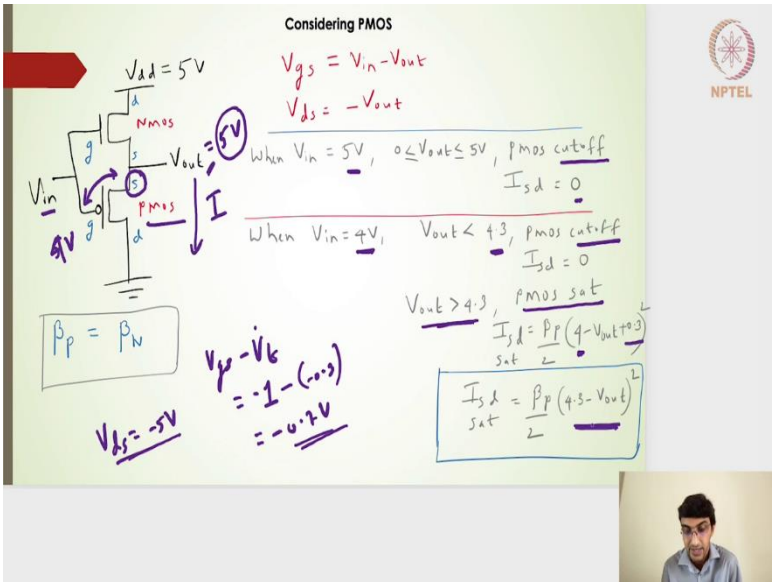

In this particular case, let us look into the PMOS transistor, because I think the PMOS transistor is there in the pull-down circuit. Where it is kind of connected to the closer to the ground rail. Whereas, NMOS transistor is connected closer to the Vdd rail. If I want to write the V_{gs} values, what we really want is this particular PMOS current to be written in the form of the V_{in} and V_{out} expression, rather than writing it in the form of V_{gs} and the V_{sd} or V_{ds}.

Let me try to find out what is the V_{gs} value for the PMOS transistor and what is the V_{sd} value or V_{ds} value for the PMOS transistor in terms of V_{in} and V_{out} voltage. V_{gs} is equal to nothing but for the PMOS transistor is nothing but

$$V_{gs}=V_{in} - V_{out}$$

$$V_{ds} = -V_{out}$$

Now, let us take an example very very similar to how we have done for the NMOS transistor. Let us take an example by picking the input voltages and then see for the different ranges of output voltages what is the current of the PMOS, very very similar to how we have evaluated for the NMOS transistor and derived or deduced the IV profile. Let us pick up an input voltage of 5 volts. If input voltage is 5 volts, we know that the output voltage has to be between 5 to 0 volts. If the input voltage is 5 volts here.

$V_g = 5V$ and output voltage is likely to be between 0 to 5 volts. It is likely to have a voltage less than that of 5 volts. In that case V_{gs} turns out to be positive, that means the PMOS transistor will always been cut off and that is why the I_{sd} current will be 0. If V_{gs} is 5 volts, on the other side the output voltages will always be between 0 to 5 volts.

The V_{gs} range or the V_{gs} value will be actually be the maximum value will be 5 volts and then the minimum value will be 0 volts, which will always be less than, it is always positive value for a PMOS transistor. Hence it will be cut off and then the current will be 0. Let us pick up an input voltage of 4 volts now, if it is 4 volts, if I change this 5 to 4 volts, V_{out} voltage has to be between 0 to 5 volts.

If it is less than 4 volts, we know that the V_{gs} will be positive and then the current will be 0, the PMOS transistor will be in cut off. If V_{out} voltages is 4.3 volts, if $V_{out} < 4.3V$, V_{gs} turns out to be $> -0.3V$.

That means that the PMOS transistor will be in cut off. Anything, less than 4.3 volts, PMOS will be in cut off, the $I_{sd} = 0$. Whenever this particular terminal, s terminal if it is less than or equal to 4.3. We will get the current to be 0, because the PMOS transistor does not satisfy the V_t voltage, that means, the PMOS transistor will always be in the cut off and hence the current will be 0.

If the output voltage is greater than 4.3, that means that the V_{gs} value will now be going more and more negative. If the output voltage is going beyond 4.3 to 5 volts, in that case the V_{gs} value becomes more and more negative. That means it crosses the negative threshold voltage that is required for the PMOS transistor and thereby there will be a flow of current, but we have to make sure that whether the PMOS will be linear or the saturation current.

In that case let us say that $V_{out} = 5V$. V_{gs} will be more negative than the threshold voltage, $V_t = -0.3V$, $V_{gs} = -1V$, $V_{sd} = 5V$ or whatever $V_{ds} = -5V$. The -5 volts is much much negative than that of the -1 volts that is coming from V_{gs} and $V_{gs} - V_t = -1 - (-0.3) = -0.7$ volts, but $V_{ds} = -5V$, it is much and much negative than that of -0.7V. The PMOS transistor should be in the saturation region, that is what we have stated here.

If it is greater than 4.3 volts, I have taken an example of 5 volts here. If it is greater than 4.3 volts, PMOS transistor will always be in the saturation region. The current we will have to use the saturation current, which is nothing but β_p. For β_p represents

$$I_{sd,sat} = \frac{\beta_p}{2}(V_{gs} - V_{out} + 0.3)^2$$

Where $V_{in} = 4V$,

$$I_{sd,sat} = \frac{\beta_p}{2}(4.3 - V_{out})^2$$

What we have seen is when the input voltage is 5 volts, the PMOS transistor is completely cut off; very very similar to that of the NMOS transistor when the input voltages were 0, then NMOS was not completely cut off. When the input voltage is 4 volts here for the PMOS transistor will either be in saturation or in cut off.

Output voltage if it is less than 4.3, it will be in cut off, anything greater than 4.3, it will be in saturation region and then the value will be $\frac{\beta_p}{2}(4.3 - V_{out})^2$. If I look into $V_{in} = 1V$ for the NMOS transistor, we will get the similar conditions of NMOS being in saturation and NMOS being in cut off.

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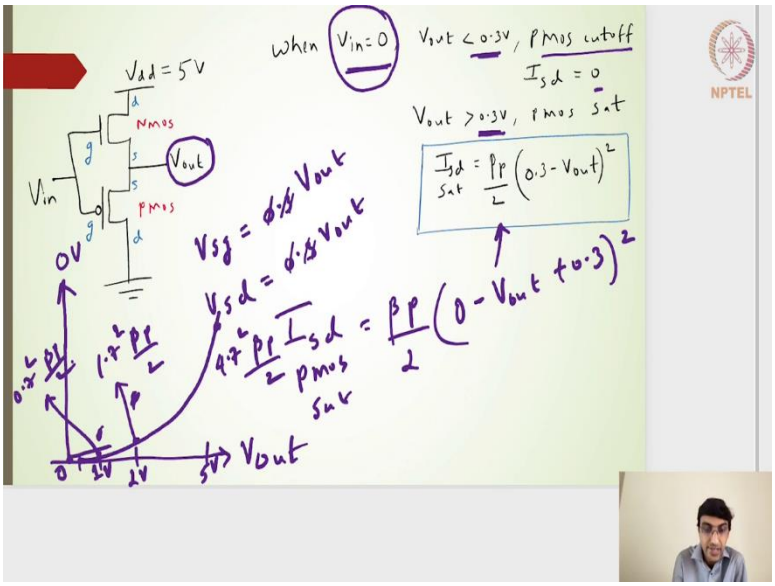

Proceeding further, when $V_{in} = 0V$, I am taking the extreme case for the PMOS transistor. We started with the PMOS transistor, we started with the input voltage of 5 volts, then 4 volts, 3, 2 and 1 and 0. I am taking the extreme case of 0 volts, I am not taking 3, 2 and 1 volts, because the expressions will be very very similar. I am taking one last extreme case of the input of 0 volts and if this is 0 volts here at the input side.

The output voltage if it is less than 0.3, the PMOS transistor will be in cut off. It is less than 0.3, it will be in cut off, anything higher than 0.3, there will be a non-zero current. PMOS will be in cut off for the output voltage less than 0.3 and $I_{sd} = 0$. For a $V_{out} > 0.3V$, that is another condition, if it is $V_{out} > 0.3V$, we have to know that whether it is in the saturation or linear region.

In this case if the output is greater than 0.3 and this is 0; my V_{sg} or whatever $V_{gs} = -0.3V$, V_{sg} is 0.3 and my V_{sd} will also be 0.3 volts, in fact it will be same. I am going to write it as if it is greater than 0.3, then it is V_{out}. $V_{sd} > V_{sd} - V_d$ and that is why the PMOS transistor will be in saturation.

My saturation current equation will be nothing but, if I write the saturation current equation for the PMOS, which is in saturation of course, will be nothing but,

$$I_{sdp,sat} = \frac{\beta_p}{2}(0 - V_{out} + 0.3)^2$$

Turns out to be nothing but whatever I have stated here,

$$I_{sd,sat} = \frac{\beta_p}{2}(0.3 - V_{out})^2$$

What we really want now is the profile of using this particular expressions for different input voltages we have now got the current profile which varies with respect to the output voltage. What we want is again the output voltage for the PMOS transistors.

If I pick this input voltage of 0 volts here, V_{out} if it is 0 what is the value? because V_{out} voltage if it is 0, the current in the PMOS transistor is cut off and the current will be 0.

If $V_{out} = 1V$; what should be the value? If $V_{out} = 1V$, I will have to put in this particular saturation current equation $\frac{\beta_p}{2}(0.3 - 1)^2$. I will get some value here, which is nothing, but $\frac{\beta_p}{2}(0.7)^2$.

Similarly for 2 volts, for 2 volts it will be nothing but $\frac{\beta_p}{2}(0.3 - 2)^2$, I will get $\frac{\beta_p}{2}(1.7)^2$ and similarly, if I take 5 volts here, it will be 4.7. I will get something like this, it is a parabolic profile, below 0.3, something like this. This two points I am going to erase it, this particular point will be my $\frac{\beta_p}{2}(4.7)^2$, this point will be for 2 volts it will be $\frac{\beta_p}{2}(1.7)^2$, this point will be very very close to $\frac{\beta_p}{2}(0.7)^2$.

What we have got now is the current versus output profile for one specific input voltage, I should be able to draw it for a different input voltages.

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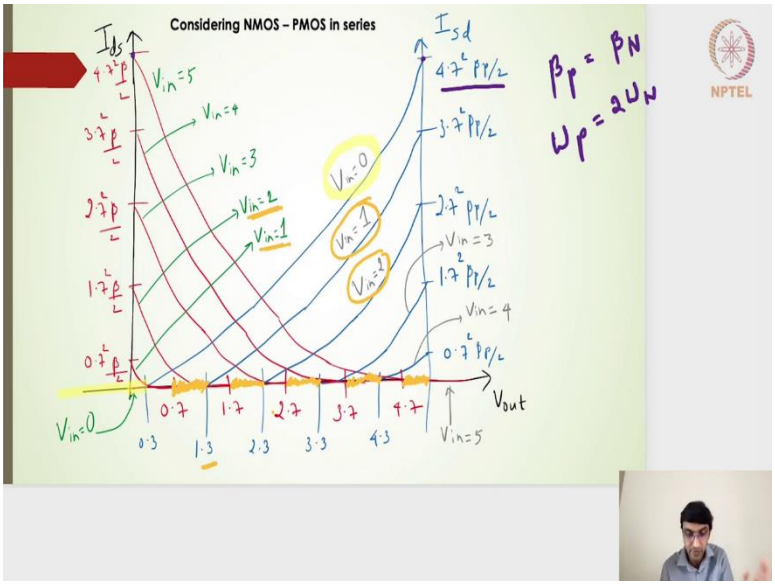

That is what we have drawn here. The current profile with respect to the output voltage for a different input voltages. In the previous slide I had shown the V_{in} voltages of 0 volts, similarly for input voltage of 1 volts, 2 volts, 3 volts, 4 volts, it is nothing but a parabolic profile, again a decreasing profile just for visualizing or writing the maximum current values on both the sides on the NMOS and then the PMOS transistors, I have drawn two parallel y axis, one for the NMOS current and another for the PMOS current with the maximum values. The maximum values are nothing but $(4.7)^2 \frac{\beta_p}{2}$ for the PMOS and $(4.7)^2 \frac{\beta_p}{2}$ for the NMOS, but for the different voltages of course.

For the input voltage of 5 volts, NMOS is giving me a current of $(4.7)^2 \frac{\beta_n}{2}$and for the PMOS I am getting $(4.7)^2 \frac{\beta_p}{2}$ for the PMOS transistor, but for input voltages of 0. Now what we have got is the current profile of the PMOS and NMOS and assuming that in this case also $\beta_p = \beta_n$, that means although the mobility of the holes is half that of the mobility of the electrons, what we have done is the width of the PMOS, we have taken it twice that of the width of the NMOS.

As to satisfy this the β has to be equal. In that case my current magnitude values, the highest values and then the lowest values will be same for the PMOS and NMOS transistors and we have got the current because both of the transistors will be in series the current will be same.

Now, this particular profile wherever they are intersecting, we should be able to find the solution. If I pick $V_{in} = 0$ here, this is my profile which starts from $(4.7)^2 \frac{\beta_p}{2}$ and then it goes to 0 at 0.3 volts and $V_{in} = 0$ for the NMOS is nothing, but this particular straight line. My intersection point is nothing but this particular points will be my intersection points, 0 to 0.3, because we are beyond the 0.3 both of them, starting from 0.3 volts, it will have a series of intersection points.

Similarly, for an $V_{in} = 1V_{in}$, it starts from $(3.7)^2 \frac{\beta_p}{2}$ and then goes till 1.3, this is what I have written here on the NMOS side if I want to pick up the $V_{in} = 1$ here. This is the input of 1 profile, which is nothing but starts from $(0.7)^2 \frac{\beta_n}{2}$ and then goes to 0 at 0.7.

The intersecting points in this case will be nothing but 0.7 to 1.3 volts, that is where I will get the intersection of the series of the intersecting points for the input voltages of 1 volts, where the current of both NMOS and PMOS are matching. Similarly for input voltage of 2 volts, again it will start from $(2.7)^2 \frac{\beta_p}{2}$ and then at 2.3 volts, so it will go to 0. And similarly for input voltages of 2 volts that is on the NMOS side, I will get it starting from 1.7 volts, this becomes my intersection points again and then similarly for $V_{in} = 3V$, it will start from 2.7 and then go till the 3.3 is the intersection points and then for $V_{in} = 4V$, I will get 3.7 to 4.3 values and then finally, for input voltages of whatever 5 volts, I will get 4.7 and this one. Now, what is happening is for the different input voltages, I am get I am actually getting a series of intersection points.

If I pick $V_{in} = 2V$, I am actually getting intersection points from 1.7 to 2.3 volts. The output voltage is now a series of this output voltage solution points. If I give an $V_{in} = 2V$ for this particular new circuit design, the output voltages could be 1.7 to 2.3, a difference of 0.6 volts. The intersection point or the output voltage can lie in between this 0.6 volts, starting from 1.7 to 2.3 volts. Hope this is clear.

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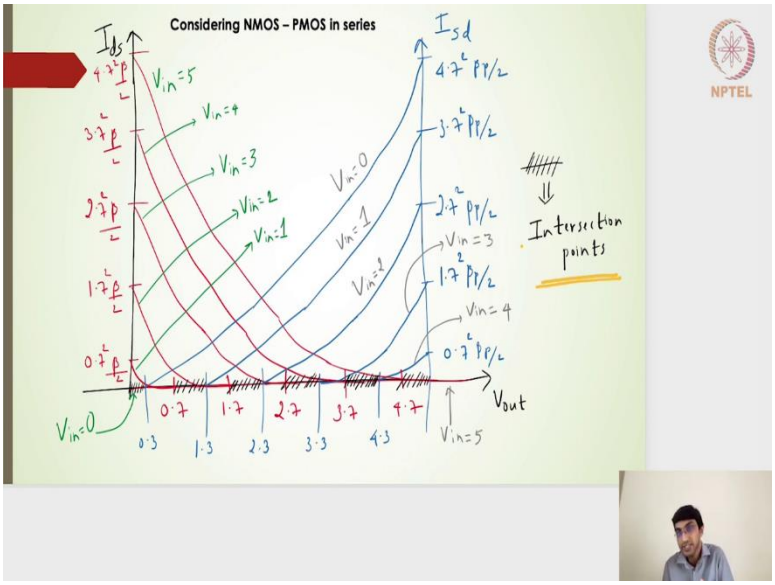

This is what we will get mathematically or graphically. This is what I have highlighted again the intersection points here. The same as nothing, but what I have shown in the earlier slide is the intersection points 0 to 0.3, 0.7 to 1.3, 1.7 to 2.3, 2.7 to 3.3, 3.7 to 4.3, and 4.7 to 5 volts. This is the series of the intersection points.

Remember that in your inverter design although we had got the currents to be the same for the PMOS and NMOS points, we used to get only one intersection points, apart from the $V_{dd}/2$ as an input voltage. Only when both the PMOS and NMOS transistors are in saturation, we will get a series of intersection points. In all other cases we got only one unique intersection points and thereby we got a unique output voltage.

For a specific input voltage we got a unique output voltage, except at the transition region. In this particular case, we are not like that, we are not getting like that. For every input voltages we are getting a series of intersection points, that too it is a theoretical or a graphical analysis.

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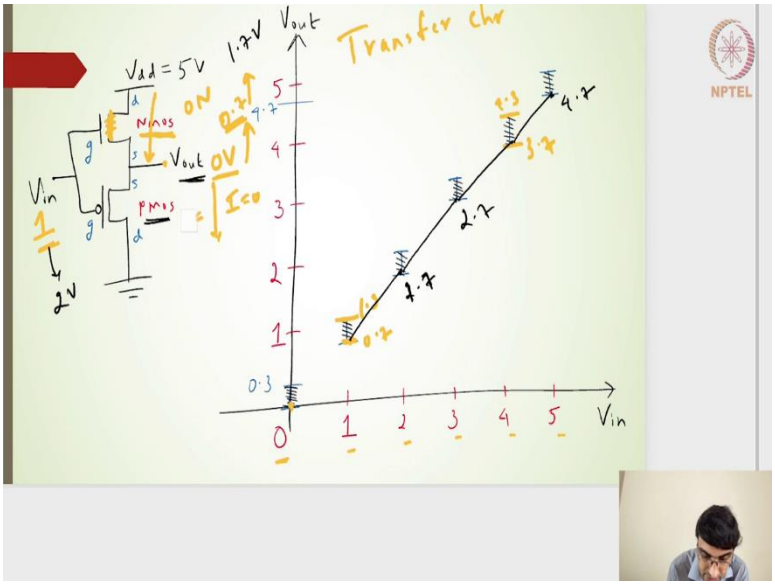

Let us see what it means. If I actually draw a transfer characteristic output voltages with respect to the input voltages. For a specific input voltage in the sense 0 volts or 1 volts or 2 volts 3 volts 4 volts and 5 volts what are those intersection points or what is that output voltage.

The output voltage is lying between 0 to 3 volts, for 1 volts of input voltage the output voltage is anywhere between 0.7 to 1.3, for 2 volts it is somewhere between 1.7 to 2.3 and then for 3 volts it is 2.7 to 3.3 and then so on. That is what we have got, this is the transfer characteristics. If I pick 1 volts as an input voltage, is it really possible for the circuit to reach to reach a point in between this two extreme steps?

Let me say that for 1 volts, the lowest point here is 0.7 volts at the output side and 1.3 volts. If I really want to see whether it is possible, if I apply one volts here at the input side, whether the output voltages can actually reach somewhere around 0.8 or 0.9 or 1 or 1.1 or 1.2 and similarly, if I pick 4 volts can it actually really can be in between any of these two points, 4 volts it will be 3.7 in the lower side and 4.3 on the higher side.

Anywhere between 3.7 and 4.3 can the output voltage be at the steady state value of let us say 3.8 or 3.9 or 4 or 4.1 to 4.2 and so on. Coming back to this particular point, let us say the input voltage is 1 volts and let us say that the output voltage is actually 0. Let us start with a very simple case the output voltage is 0, the input voltage is 1 volts.

I have a V_{gs} value on the PMOS side is positive 1 volt and the V_{gs} value on the NMOS side is positive 1 volt. The PMOS will be off and NMOS will be on, it means that it is not in the cut off. The NMOS will be in not in cut off, whereas the PMOS will be in cut off.

The current for the PMOS will be 0 and the current for the NMOS will have some kind of a current here on the NMOS side. What it implies is, although both the series currents are should be same; but what we are saying is the NMOS there will be some current and then the PMOS there will not be any current. What it really means is this particular output voltage there will be some current before reaching the steady state value.

What we have said is the PMOS and NMOS steady state current should be in series, the steady state current should be equal. But let us say that input voltages was something else and then we have switched on the power supply and then I will get this 1 volts and thereby I will get some kind of a transient current, before reaching the output volt, before reaching the steady state output voltage. The initial conditions are output voltage is 0, input is 1 and that is why NMOS is on and PMOS is off. Thereby now I will start getting the NMOS current, which will ensure that the output voltage is gradually increasing from 0 to some value.

In that case if $V_{in} = 1V$ and output voltages is increasing from 0 volts, it increases to let us say 0.1 volts, no problem V_{gs} is still 0.9. It increases to 0.5 no problem, V_{gs} will still be 0.5, if it increases to 0.7, output voltage from 0 volts it increased to 0.7 volts, after that my V_{gs} this particular channel.

The $V_{gs} = 0V$, $V_{gs} = 0.3V$, if the output voltage starts increasing beyond 0.7 volts, the V_{gs} value will be less than 0.3 and thereby the channel here that is formed for constantly charging the output node voltage will not be there. The output node voltage can reach effectively till 0.7.

The output voltage started from 0 volts and it can reach to 0.7. Let me pick another pen color. Let us say that the input voltage has increased to 2 volts, output voltage will increase and it will increase till 1.7 volts, beyond which the channel will be cut off again, the channel will not be there and thereby it will be limited to 1.7 volts.

From 0.7 it can go till 2.7 volts or rather 1.7 volts, from 1.7 volts it can go till 2.7 volts, similarly it can charge till 3.7, it can charge till 4.7. Similarly, very very symmetrically on

the NMOS side what we have seen of the charging of the output node voltage from 0 volts to 0.7 to 1.7 to 2.7 to 3.7 and finally, reaching 4.7.

On the discharging side whenever the PMOS is on, that means that let us say that the output voltage has reached 4.7 volts.

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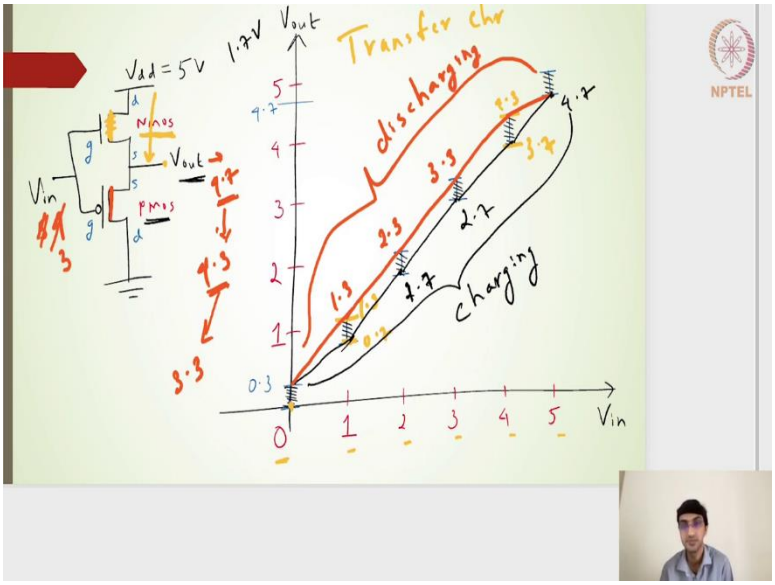

Let us say that the output voltage is 4.7 volts and let us say that the input voltage is 5 volts. In that case my V_{gs} value is 0.3, whether it is possible for the output voltage to decrease, that cannot, it will have a channel and it starts. The V_{gs} value is there and it becomes positive, the PMOS will always be off.

Let me take $V_{in} = 4V$, $V_{gs} = -0.7V$. The PMOS the channel is there, the output voltage can actually drop down, because this PMOS transistor is on, it is discharging to the ground and thereby 4.7 volts whatever is the charge has been applied there will be discharging it here through the PMOS transistors and finally it can get dropped till 4.3 volts.

Because beyond that the PMOS that whatever the channel was there, which was facilitating the discharge path from 4.7 to 4.3, beyond that it will not possible, because the channel would not be there.

From 4.7 it can actually go to 4.3 and then if I decrease this input voltage to 3 volts. the V s will be much much negative. It can drop till 3.3 volts, beyond which the channel will not

be formed and then thereby it can go to 3.3, it can go to 2.3, it can go to 1.3, and finally, it can go till the 0.3.

This is what we will have 3.3, 2.3, 1.3 and then finally 0.3 of voltage as a steady state value. Once again when the input voltages is applied as 1 volts. I will use a different ink and it will charge back to 0.7. This is what we will have the transfer characteristics. This particular region whatever I have drawn it in the black line is for the charging profile.

While the output voltage is actually moving up from 0.3 it can reach till for 4.7 and the discharging profile, while it is getting pulled down by the PMOS transistor. This particular region of the red is nothing but our discharging, the voltage is dropping down.

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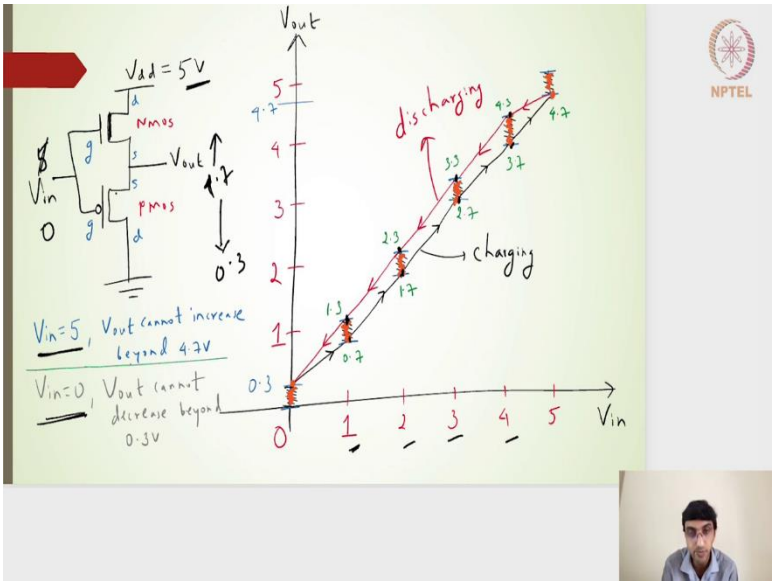

That is what I have drawn here, the discharging profile and then the charging profile and then I have written down the points of 1.3, 2.3, 3.3, 4.3 and all those values, but it cannot take the intermediate values between 0.7 and 1.3.

In fact, it cannot take any values here, the output voltage actually cannot take any of these values here, although theoretically or graphically we have got those points, but when it is in a circuit, we it satisfies only one point. It satisfies only one point here, while it is charging, it satisfies only one point here, one point here 2.7, 3.7, 4.7 and while it is coming back or discharging only one point is satisfied.

Although we got the series of intersection points, only 2 for a input voltages of 1, 2 and 3 and 4 only these extreme cases are satisfied. Only the 2 points which are on the extreme case are satisfied, while it is going up only one case is satisfied, only one intersection point is satisfied, while coming down only one intersection point is getting satisfied. Now again same thing when the $V_{in} = 5V$, let us say that when $V_{in} = 5V$ here, V_{out} cannot increase beyond.

It cannot go beyond 4.7, 4.7 the reason is very simple, the moment it goes beyond 4.7, this particular channel will not be there. There is no channel for the output voltage to get connected to the $V_{dd} = 5V$ and thereby there is no channel for the output voltage to get charged or to get pulled up towards 5 volts, it will get restricted to 4.7.

Similarly, when $V_{in} = 0V$ it can go till 0.3 volts, beyond which the PMOS channel will not be there and the PMOS will not be able to pull it beyond 0.3 volts.