Design and Analysis of VLSI Subsystems
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Lecture – 16
Bad CMOS Buffer - Part 1

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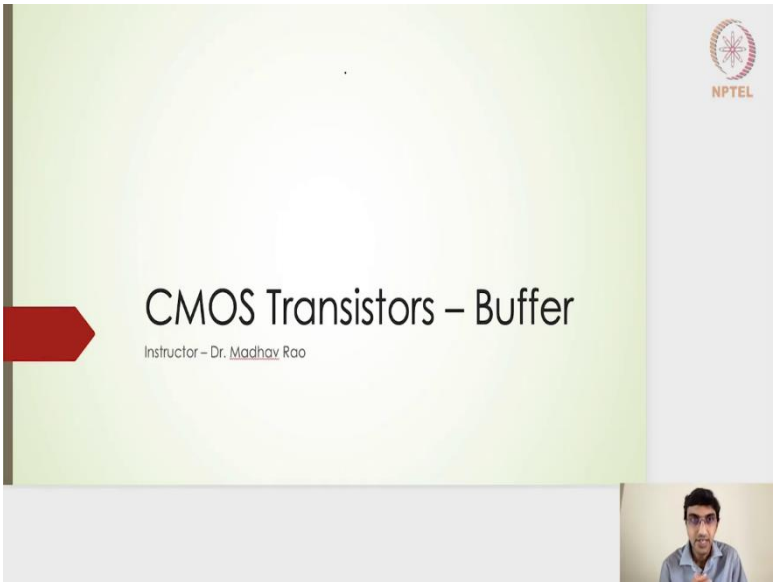

Let us begin this particular lecture on the Buffer design. One of the designs which we will not normally use, but I think it is very important to understand why we generally do not use this particular buffer design.

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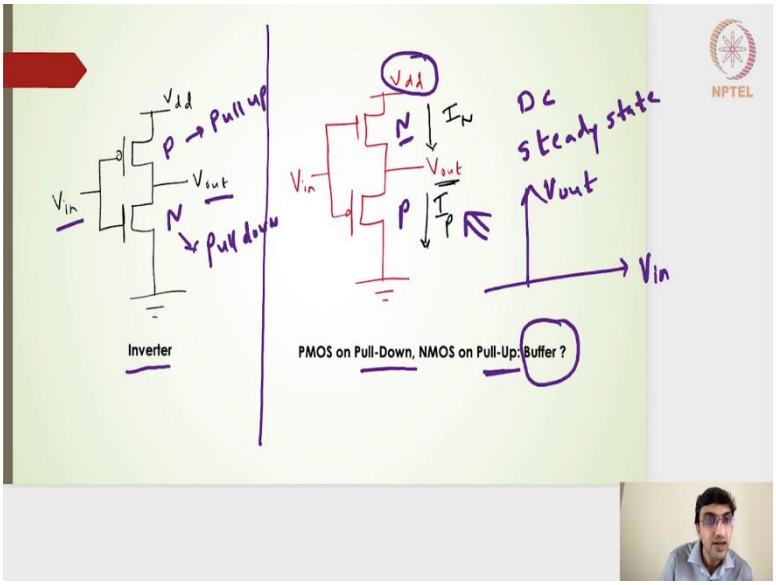

Going into the next slide. This is what we have this particular region is the inverter and this one is the new design which we are talking about. Let me pick up a pointer and then start emphasizing on the different points. This is our inverter design. This is what we had seen the inverter design and we know that the PMOS transistor and then the NMOS transistor are connected in series and thereby we were able to visualize the V_{out} steady state voltage for a given steady state input voltage.

Similarly, what if I have this kind of the transistors configuration like, the NMOS is here and then the PMOS is here. If I look into the left-hand side and then the right-hand side, you will notice that the PMOS and the NMOS transistors are completely swapped in their positions. The NMOS is now closer to the Vdd rail and then the PMOS is now closer to the ground rail also, but the input is very very similar to what we had seen for an inverter design.

What we had seen for the inverter design is the PMOS transistors was closer to the V_{dd} rail and we call it as a pull up circuit. NMOS transistor was closer to the ground rail and then this is pull down circuit. In this particular new configuration circuit, new circuit where we have exactly the positions of the NMOS and PMOS to be altered or to be swapped. We have the NMOS on the pull up side and PMOS on the pull down side and then I have written here a question mark on the buffer. We will see what should be the output characteristics whenever we apply the input voltage and again, we are looking into the DC characteristics. The DC steady

state characteristics at the output side when a given an particular input voltage, this is the V_{dd} value. This is the V_{dd} rail we have used, the input voltage actually ranges from 0 to V_{dd} volts.

And for our inverter example we have taken a V_{dd} of 5 volts. Here also we will apply the same V_{dd} of 5 volts and input voltage are ranging from 0 to 5 volts. In the steps of whatever you know what in the inverter we had used the steps of 1 volts. What it means is if the input voltage is 0 volts what should be the output voltage.

If the input voltage is 1 volt what should be the output voltage. If the input voltage is 2, 3, 4, 5 what should be the respective output voltages and then for the inverter we had drawn the DC transfer characteristics and then similarly what we want is for this particular circuit, for this particular buffer circuit, this particular configured circuit we need a steady state transfer characteristics V_{out} versus the V_{in}, this is what we want eventually.

For an input voltage now, what should be the output voltage for this particular circuit. Moving forward let us try to analyze how do get this particular transfer characteristic. What we really need is the current versus the voltage characteristics. Especially, if you can find out the current versus the output voltage and then the intersection point should be able to map it into this particular V_{out} versus V_{in} characteristics.

If I actually look into this, let me pick up in different pointer. This particular current and then this particular current, so I am going to write this current as an NMOS current and as a PMOS current. Again, these two transistors are in series. So, the NMOS current and then the PMOS current should be equal.

Wherever the currents are intersecting even in this particular configured circuit, I should have that as a solution point for the V_{out} voltage, which will give me the V_{out} voltage for a specific input voltage. Those particular V_{out} voltage I am going to draw it in the V_{out} versus the V_{in} characteristics that will be my transfer characteristics for this particular new circuit.

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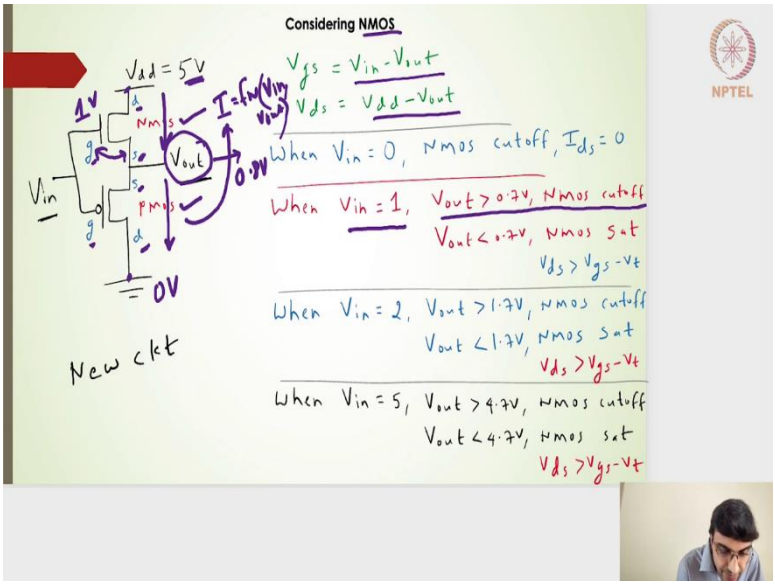

Moving ahead pick up the next slide. This is what the new circuit is. I am going to write this as saying that this is my new circuit. NMOS is on the pull up side and then PMOS is on the pull down side and I am going to label this NMOS and the PMOS terminals. The V_{dd} let us pick again at 5 volts and V_{in} voltage will range from 0 to 5 volts. V_{out} voltage as we had seen in the inverter also should range between 0 to 5 volts.

The rail is 5 volts, this is the rail is 0 volts here. The rail of V_{dd} is 5 volts, the rail of ground is 0 volts. The V_{out} voltage should either be between the 5 to 0 volts. It could be any value between 5 to 0 or any analog values also like 3.3 or 4.3 or 5.3 or 3.7 or 4.7 or 2.7 or 1.7 or 0.7 and so on. It should be any values between 5 to 0 volts. Input voltage again we will be restricted to not go beyond 5 volts and not go below 0 volts.

It should be between 0 to 5 volts, because my rail I have defined it as 5 volts. It is assuming some point kind of the technology node a V_{dd} of 5 volts has been chosen. The V_{in} and V_{out} should be lie between 0 to 5 volts. Now, if that is the case, if I pick the NMOS, what should be the labeling of the terminals across this NMOS transistor.

Which one should be drain which one should be source and which one should be gate. Gate is anyways very very intuitive. The input that has been applied onto this particular terminal will be the gate terminal and similarly for the PMOS also this will be the gate terminal. Choosing the drain and the source, now remember for the NMOS transistor the drain is always the terminal which has a higher potential than that of the other terminal is source terminal.

In this case the V_{dd} is given to this particular terminal and that is set to 5 volts. V_{out} can reach to 5 volts, but it can reach to 5 volts, but it should be always be in between 5 to 0 volts. That means that this terminal is likely to be on a lesser potential than that of another terminal.

In that case, the V_{dd} terminal, whichever V_{dd} rail, whichever terminal it is fixed to, that will be the drain, this is what the drain is for the NMOS. The other terminal the V_{out} terminal which ranges from 0 to 5 volts is likely to have a lower potential, it is likely to reach to a lower potential than that of the other terminal and that is of the reason why this is chosen as source.

On the PMOS side, this particular PMOS transistor again we have to choose the terminals the source and the drain. Remember that for the PMOS, the source terminal has to be at a higher potential than that of the drain. The drain of one terminal this is connected to the that the ground rail, that means, that this particular potential will always be 0 volts, will always be 0 volts similar to what we had seen here. That means, the other terminal which is connected to the V_{out} potential node is likely to be between 0 to 5 volt. It is likely to be having a higher potential than that of the 0 volts, that is why this particular terminal is chosen as the source node and then this one is chosen as the drain.

Now, once we have the source a drain and then the gate terminals annotated in our transistor, it becomes much simpler for us to analyze what should be the current and what should be how do we estimate the current right, estimate the current and which current we are talking? about this particular current and then we are talking about this particular current on the PMOS side.

We can actually estimate the current by writing the current equation in terms of V_{gs} or V_{ds} in terms of V_{gs} or V_{ds} for the PMOS and NMOS respectively. That is why the terminals labeling are very important, even it was important for our inverter design and it is kind of important even for this particular new circuit configuration. If I start writing down in fact even for an inverter transfer characteristic.

We finally, draw the IV characteristics in terms of the input voltage for a specific input voltage, the profile of the current with respect to the output voltage. If both for the NMOS as well as for the PMOS. Similarly, here also what you are intending to do was write down the current equation of the NMOS and PMOS as a function of input as a function of output voltage. Same here for the PMOS also a current equation in terms of the input and output variables instead of V_{gs} and V_{ds} variables.

To begin with what we have done is we have considered the NMOS transistors. Only the NMOS transistors are considered here and then we will go with the PMOS transistors and then we will see how to put the profile of the NMOS and then the PMOS current with respect to the output voltage in one particular coordinate system. So that I will be able to get the intersection points, those intersection point will give us the V_{out} voltage for the specific input voltages.

To begin with if I want to write the current equations in terms of the input and output voltages, let me try to find out what is the V_{gs} in terms of V_{in} and V_{out}. V_{gs} for an NMOS is this one, where g is connected to the input and s is nothing but output. V_{gs1} input is nothing but $V_{in} - V_{out}$, and V_{ds} for the NMOS transistor is nothing but V_{dd} which is nothing but $5 - V_{out}$, this is what the $V_{dd} - V_{out}$ turns out to be. Now, what we have to do is we have to draw the profile. Let me pick a input voltage of 0 volts. If the input voltage is 0 volts here when the input voltage is 0 volts V_{gs}, V_{out} has to be between 5 to 0 volts. It is kind of a positive value V_{gs} turns out to be negative, that means, NMOS transistor will be in cut off. Ids will be 0. When the input voltage is 0 volts, V_{gs} turns out to be negative and thereby the current will be 0, because the NMOS transistor is cut off.

When $V_{in} = 1$ 1 volts, V_{out} again has to be between 0 to 5 volts and let us say that V_{out} voltage is between 0 to 5 volts I do not know what current it will give. If V_g which is nothing but 1 volts here and let us say that the V_{out} is 0.8 volts for some reason it has gone to 0.8 volts.

V_{in} is 1 volts, V_{out} is 0.8. V_{gs} value turns out to be 0.2 volts alright. The NMOS will be in cut off. In fact, the NMOS will be in cutoff for any values of V_{out} above 0.7 volts. Any values above the V_{out} goes above 0.7 volts it will be in cut off and that is what I have written V_{out} any above 0.7 volts NMOS will be in cut off and any values below 0.7 volts. I will have the NMOS giving the current. Let me try to see whether I can erase some of these diagrams. On resuming, we were at new to the NMOS and then the PMOS transistors and let us say that what we wanted to say is if this is 1 volts and V_{out} is let us say it is 0.5 volts alright.