Design and Analysis of VLSI Subsystems
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Lecture - 15
Transmission Gate

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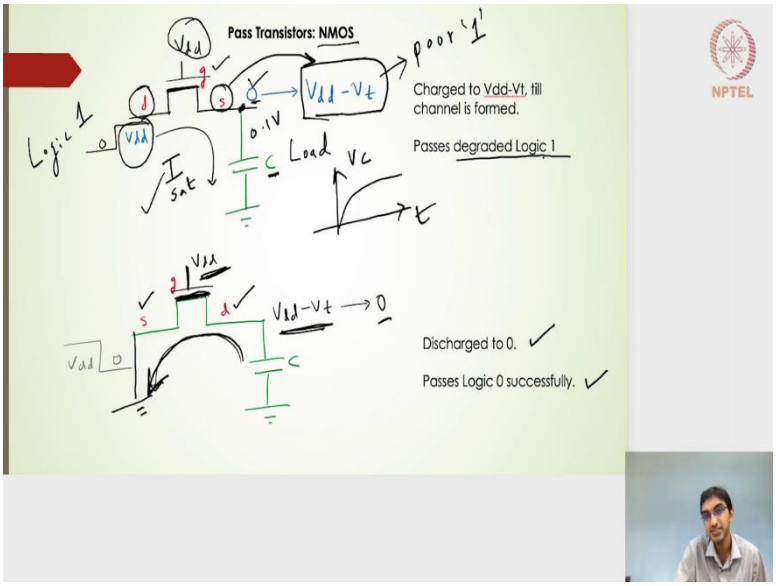

In this particular lecture, what we will talk about is more on the pass transistors and then the transmission gates. I have drawn a pass transistor here. In this particular case, it is a pass transistor means a single transistor, and I have considered the NMOS as the pass transistor here and then we need to understand the working of this particular NMOS transistors. The pass transistors can also be designed using the PMOS transistors and that is something we will see in the future slides.

Let us begin with this NMOS transistor. I have drawn the NMOS transistor here. The input is provided with a V_{dd} power supply here. The V_{dd} is this particular V_{dd}. The drain and source are there and let us say that for the drain the V_{dd} is being applied, a power supply is there.

I have switched on the power supply and that is why earlier if it was wired at this particular terminal of the transistor was directly connected to the power supply and then if it was switched, so that is why you will see this kind of a step input right 0 to V_{dd}.

I have switched on the power supply and this particular terminal receives a power supply of Vdd and let us say that on the other side of the terminal we have arranged a capacitor. A load capacitor is there. This is nothing but a load capacitance is been added.

Even if there is no load capacitance, the source and then the body or rather whatever the source or the drain with respect to the body, that is the terminal with respect to the body will always have the junction capacitance. Irrespective of the load capacitance, there will always be a junction or a depletion capacitance or a parasitic capacitance, which we had seen in the previous lectures. I have drawn this particular capacitance and on this particular terminal, we have switched on the power supply. This is anyways V_{dd} is applied to the gate, because it's an NMOS transistor, we know the gate terminal here, this is the gate terminal g. We do not know which terminal is this, whether it is a drain or source, although I have written it as d and s, let us try to validate whether it is actually drain.

To begin with the capacitor is not charged at all. The capacitor carries a voltage of 0, it has a voltage of 0 here. On the other side of the terminal, it has a potential of V_{dd}. For an NMOS, the drain should be at a higher potential than the source and that is why we have this side covered as drain and then this side covered or called as source. Now I have this particular terminals, and then the power supply is also labeled in these particular transistors, we should be able to state, which operating region the transistor is operating, whether it is a linear, cutoff or saturation region.

If I have this particular V_{gs} value which is nothing but $V_{dd} - 0$, because initially it says 0 volts. So, initially $V_{gs} = V_{dd}$. Initially the transistor will be in the saturation region. Is that correct?

The V_{gs} value is V_{dd}, the V_{ds} value is also V_{dd}, because initially it is 0 volts. Initially the current will be flowing from V_{dd} and it will be charging the capacitor. The charging capacitor or the charging current for the capacitor is the saturation current, I am going to say that this is nothing but saturation.

This particular source potential while the capacitor keeps on charging, it is going to have an increase in the voltage, across this particular node it is going to have an exponential profile, capacitor charges and then it should have an exponential profile of the voltage for the capacitor with respect to the time so the capacitor charges. And let us say that after some time, it will reach to a 0.1 volts.

V_{ds} value is still $V_{dd} - 0.1$, V_{gs} value is still $V_{dd} - 0.1$. So, it will still we in the saturation region. So, it continues to this charge the capacitor via the saturation current and it will reach to a value of $V_{dd} - V_t$. So, the capacitor charges still $V_{dd} - V_t$.

After that once the source potential reaches, once the source potential reaches $V_{dd} - V_t$, V_{gs} turns out to be less than V_t. So, once it is it goes beyond , so let us say that V_{dd} is 1 volts, V_t is 0.3 volts. So, until 0.7 volts it is charging the capacitor. So, this particular configuration is charging the capacitor.

But once it goes beyond 0.7, let us say 0.71, V_{gs} turns out to be less than 0.3. So, there is no channel that is formed here. So, the channel is not there for the current to drive from the drain to source and then charge the capacitance. So, the capacitance can charge still $V_{dd} - V_t$. So, if I have a V_{dd} here, it can charge till $V_{dd} - V_t$. So, the charge to $V_{dd} - V_t$ till the channel is formed.

What it implies is if I have a pass transistor and if I want to supply the logic from one end and then see the other end voltage if I pass a logic here, so a logic 1 on one terminal which is nothing but V_{dd}, on the other side I will get $V_{dd} - V_t$, $V_{dd} - V_t$ is called as a poor logic 1.

Poor logic 1 because it is actually closer to $V_{dd} - V_t$ is actually closer to V_{dd}, far away from logic 0 and that is why it is called as it is passing logic 1, but it is passing a degraded logic 1 or a poor logic 1. This is about passing the logic 1. NMOS transistor passes a degraded logic 1.

Now, let us see what happens if I want to pass a logic 0. Passing a logic 0 means this particular power supply which is there which I had switched on in this particular case I am going to switch it off, so that it connects to the ground, there is 0 volts here. Thus this particular terminal I am going to connect it to the ground, whereas this capacitor is now completely charged to $V_{dd} - V_t$ that is the maximum it can go.

And we will see that whether this particular capacitor discharges to 0 volts because on the other terminal it is now connected to the ground. The capacitor now starts discharging. It starts discharging using the channel here, the channel becomes the path for the current to flow from one terminal to the another terminal of the NMOS transistor.

Now, we have to label this. The label in the sense the gate, source and drain which of these terminals are the drain and the source terminal, the gate is very easy to identify. It is gate and

this particular terminal is the gate terminal and we know that it is connected to the V_{dd}. We do not know which one is the source or the drain here.

This particular terminal is $V_{dd} - V_t$, this particular terminal is connected to the ground which is nothing but 0 volts. Whichever terminal has a higher potential we will call it as the drain terminal. Similarly in this particular case the first case we also labeled or defined the drain terminal for the terminal whichever one is higher.

Whichever potential is higher V_{dd} or 0 we will call it as the drain terminal. This drain terminal is nothing but $V_{dd} - V_t$ because it is greater than the 0 potential. This becomes a drain and then this becomes the source.

In this case, if V_{gs} is there, V_{gs} will always be $V_{dd} - 0$ because this is anyways grounded. V_{gs} will always be 0 here. In this case, V_{gs} was changing continuously as the capacitor was charging. V_{gs} was starting value of the V_{gs} was V_{dd} and then a capacitor voltage increases, the V_{gs} value started decreasing and until it reached $V_{dd} - V_t$ above beyond the V_{gs} value. V_{gs} value turned out to be less than V_t and thereby the channel was disconnected.

Here the V_{gs} value is always $V_{dd} - 0$, so it is greater than V_t value. There will always be a channel here in this particular transistor. Thereby the capacitor can always have a path. It ensures that there is always a path for the discharging. So, it starts from $V_{dd} - V_t$ and then discharges completely to 0, that is what I have written here discharge to 0 and it is also passes the logic 0 successfully. It does not stop in between.

It does not stop in the middle as it reaches to the 0 volts and that is why if I apply on this particular terminal 0 voltage it passes the 0 successfully, whereas for an NMOS transistor it passes a degraded logic 1, because it is limited till $V_{dd} - V_t$.

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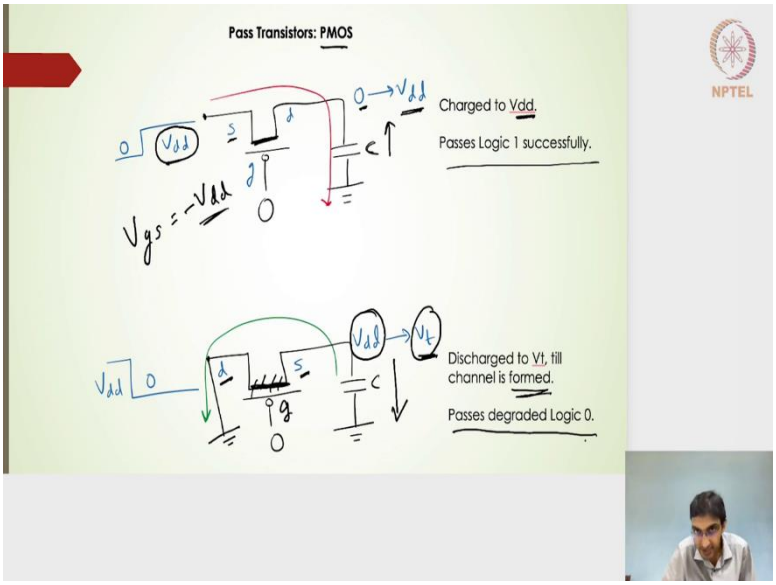

Going forward let us take a look at the PMOS transistor as a pass transistor again. If I look into this, the PMOS transistor again the same thing the gate is connected to the 0 volts because I want the gate to be at a negative potential than that of the source. V_{gs} value turns out to be negative for the PMOS. I am putting it 0 on both the cases, 0 volts of the gate represents why here it is a gate. 0 volts of the gate represents that the PMOS transistor has a gate potential of 0.

Other two terminals again if I have connected a power supply and switch on the power supply. I will get a step response V_{dd}. I am having a V_{dd} potential connected to the one terminal. For a PMOS transistor, we know that the terminal which has a higher potential that should be the source in an NMOS drain should have a higher potential than that of the source, whereas in the PMOS the source should have a higher potential than that of the drain.

Whichever one has a higher potential that will be the source. In this case, the power supply is connected to the terminal and that is why we call it as the source. Because, on the other side, even if the physical capacitance is connected, the capacitor initially will be at 0 volts. This particular terminal potential will be less than that of the other terminal potential. This will be considered as source and the other one is considered as drain.

V_{gs} value for this PMOS transistor is nothing but always $-V_{dd}$ always, because the other terminal we have the capacitor connected and the capacitor is charging it does not disturb the V_{gs} value. The V_{gs} value is always $-V_{dd}$, which is much much less than that of $-V_t$ or -0.3V.

Thereby the PMOS transistor has a path constantly available for it to charge the capacitor. The capacitor even if it starts from 0 volts, it will actually charge till V_{dd}. For the PMOS pass transistor, it charges to V_{dd} and it passes the logic 1 successfully.

On the other side, if I have it grounded, if the power supply is now switched off, I will have this particular terminal connected to the ground. Now, let us say that a capacitor is charged to V_{dd}. Whichever terminal of this particular PMOS transistor has a higher potential that particular terminal will be labeled as source, the other terminal will be labeled as drain.

This will be the source and then this will be the drain, this is V_{dd} let us say that this particular capacitor starts with V_{dd}. This will be the source and then the other one which is connected to the ground will be the drain. V_{gs} value as the capacitor discharges, that means, the potential across the capacitor is going to decrease. Initially it starts from V_{gs} value, V_{gs} value as $-V_{dd}$. But as the capacitor discharges, this V_{gs} value is going to decrease. In fact, it is going to become closer and closer, it was more negative $-V_{dd}$ and it is coming closer and closer to the 0 volts, it starts discharging and it discharges till it hits the V_t value. The movement V_{gs} becomes $-V_t$ beyond that it the channel which is formed here, the channel that is formed in the PMOS transistor will not exist anymore, it will discharge till V_t.

The discharging of this particular PMOS transistor is held or its limited to V_t till the channel is formed beyond that the channel does not exist, there is no discharging path. The PMOS transistor passes a degraded logic 0, whereas the NMOS transistor passes successful logic 0. The PMOS transistor passes the successful logic 1, whereas the NMOS transistor passes an incomplete or a degraded logic 1. Hope this is clear.

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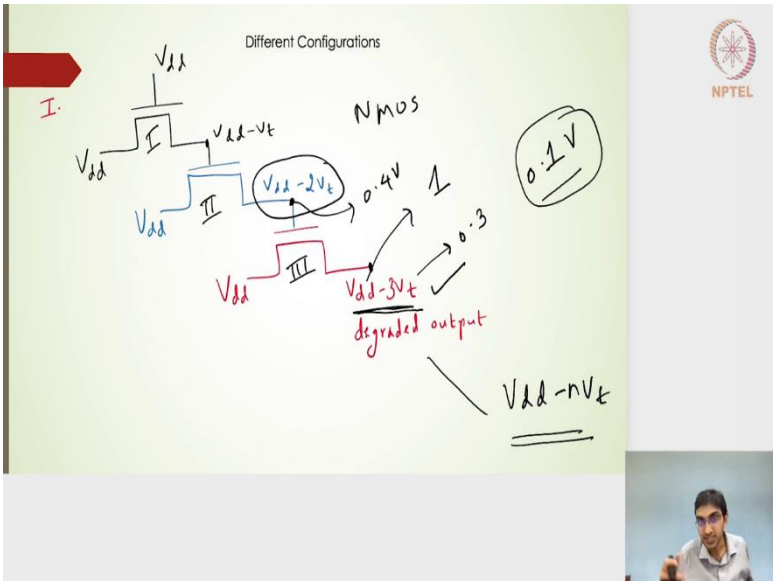

I have drawn two different configurations here. One where we have a stacked transistors and the output of this particular first transistor is connected as a gate to the next transistor. The next transistor output is connected to the third transistor. In this particular configurations I have three transistors and then we have the supply of V_{dd}.

What should be the output of the third transistor? if this is V_{dd} and then the gate is V_{dd} and it is an NMOS transistor, it is an NMOS configuration here. We know that the output will be charging till it reaches $V_{dd} - V_t$. Beyond that this channel or this transistor will go into the cutoff.

It will go till $V_{dd} - V_t$. If this is $V_{dd} - V_t$ and this is V_{dd}, it is going to charge this particular node, it is going to charge till $V_{dd} - V_t$. It is going to charge till $V_{dd} - 2V_t$. Similarly, for the third transistor, it will go till the $V_{dd} - 3V_t$.

For the n transistors, it will be nothing but $V_{dd} - nV_t$, provided it does not go below that of the V_t value. This will be the $V_{dd} - nV_t$ as a general expression. If I consider V_{dd} to be 1 volts and then V_t to be 0.3, it will be 1 minus of 3 into 0.3, so it will be 0.1 volts which is not true, because this one will have 0.4 volts.

To begin with this one will start from 0 to 0.1, this will be $V_{dd} - 3V_t$ that is correct and then if I have the fourth transistor, so this will be 0.1 volts which is very very less than that of the V_t. The fourth transistor will always be in the cutoff region.

If there is a capacitor, there is no path connecting in the fourth transistor, that particular channel does not exist for the fourth transistor. The output of the fourth transistor will always be the 0 volts, and then the fifth transistor will also be in 0 volts. Hope this is clear.

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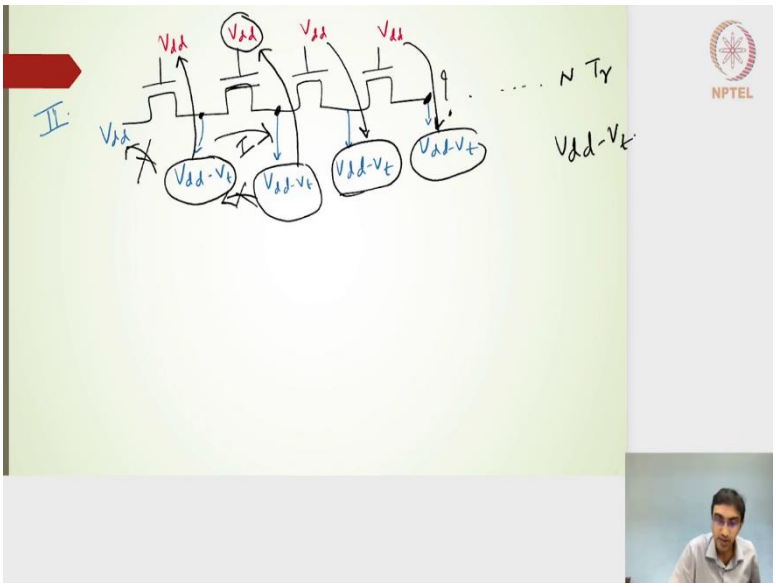

Second configuration where we have again a cascaded one, I call it as a stacked 1 and then this one is called as a cascaded 1. The reason is nothing but the output is connected to the input of the pass transistor and again the output of the second transistor is connected as an input to the third transistor and so on. Finally after four transistors cascaded four transistors configuration what should be the output here?

If I am supplying V_{dd} here and the gate of all our transistors in the cascaded configuration is V_{dd}, what should be the output here? The output is nothing but it will reach till $V_{dd} - V_t$ beyond which it cannot go because this particular transistor will be in cut off, it will drive till $V_{dd} - V_t$. The next transistor again it will drive till it is going to pass this particular transistor to charge the capacitor at this particular node, this is the current.

But their charging the voltage profile of this particular charging, it will reach till $V_{dd} - V_t$, the reason is beyond that the V_{gs} value of this second transistor will be less than V_t and then the channel here will be broken. Thereby it will charge till $V_{dd} - V_t$. Note that this $V_{dd} - V_t$ has nothing to do with this particular voltage.

This delimiting factor is nothing but coming from the gate voltage, whatever is the gate supplied voltage it is actually derived from the gate supplied voltage. Again, this $V_{dd} - V_t$ is actually derived from this particular gate voltage and then this $V_{dd} - V_t$ is also derived from this particular gate voltage of V_{dd}.

Beyond which the transistor will be in cut off. Therefore, the maximum output voltage will be $V_{dd} - V_t$ here. In fact, if I keep on going for the N transistors, the output of the Nth transistor will also be $V_{dd} - V_t$. Hope this is clear.

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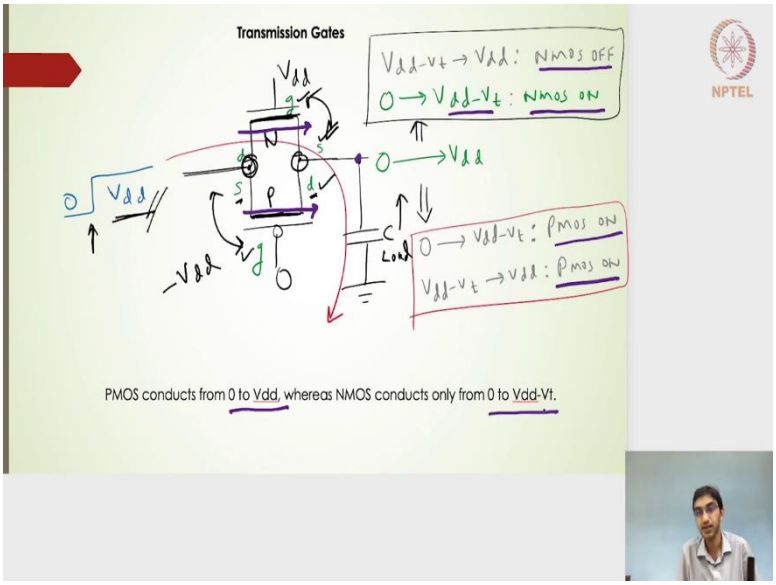

Moving ahead now let us take a look at the transmission gates. Alright, earlier we had seen the series the inverter which is nothing but a series of the PMOS and NMOS transistors. Here instead of having a series of PMOS and NMOS transistors, what we have is a parallel combination of PMOS and NMOS transistors. I have a PMOS transistor this one the bubbled gate shows that is a PMOS transistor and the unbubbled gate is an NMOS transistor.

The gate of both this transistor is very very clear. I am going to write this gate as g, and then this gate as d. On one side the gate is supplied with the V_{dd} on another side the gate is supplied by 0 volts. The moment the gate is supplied by V_{dd} or the gate is supplied by 0 volts on the PMOS side, we know that this transmission gate should drive some current unless the V_{gs} value turns out to be less than V_t on either side.

You know V_{gs} value is less than V_t for NMOS and V_{gs} value is less negative than that of -0.3 then we can say that it is in cut off region. We have connected the two terminals the two diffusion nodes here and then we have also connected the diffusion nodes of the NMOS and PMOS transistors.

Basically, we have tied both the diffusions and then fed it into a power supply again its a step response the reason is I have switched on the power supply. I will get from 0 volts now at this particular instance it is switched on. I will get the V_{dd} power supply. The moment it is the V_{dd} power supply and I need to have the labeling of the terminals.

That I can write, I can find out or I can estimate the current and then I can estimate the charging profile of the capacitor. On the other side there is a capacitor here it could be the load capacitor connected to the ground. If this is V_{dd} for an NMOS transistor whichever one earlier this capacitor, formally this load capacitor is connected at this particular terminal, the load capacitance initially it is completely discharged, the potential here is 0 volts.

On the other side of the terminal, it is the V_{dd}. Whichever potential or whichever terminal has a higher potential that should be the drain the other one should be nothing but the source for the NMOS transistor. For the PMOS transistor it is the opposite, whichever terminal has a potential has a higher potential than the other one that should be called as a source and the other one should be called as a drain.

Now I have this particular configuration of NMOS and PMOS where the same tide node is having a different terminal. The NMOS has a drain here whereas, this particular tide node has the source represented for the PMOS and similarly on the opposite side NMOS has the source here and then the PMOS has a drain here that is perfectly fine. That is perfectly fine because the channels here are formed by this gate to source of the NMOS, the channels of the PMOS are formed by gate to source of the PMOS.

What we are interested is whether that there is a channel path for this capacitor to charge or discharge. In this case it is charging because the power supply is V_{dd}. I have switched on the power supply, now for the NMOS is the V_{gs} value. So, this is the V_{gs} value. The capacitor while it is charging through this particular path, the voltage is going to increase. Increasing the source voltage for the NMOS is going to reduce this V_{gs} value for the NMOS, it can reach, it can increase till it reaches $V_{dd} - V_t$.

As we know that the NMOS transistor is going to pass a degraded logic 1, whereas the PMOS is going to pass a logic 1 successfully, because this V_{gs} value is independent of the capacitor charging effect here which is completely on the other terminal. The V_{gs} here for the PMOS is nothing but minus of V_{dd} alright. It will always have this path for charging.

Now, I have one path. Let me draw using a different pointer. I have one particular path here and another path here. I have two paths for charging the capacitor. The charging rate will be higher. It will take less time for the capacitor to charge when we compare this particular transmission gates, when we compare with that of the only single PMOS transistors because the paths are now two. It is also charging from this particular NMOS path, it is also charging from this PMOS path to.

At the output side or this particular side the capacitor charges and then reaches to $V_{dd} - V_t$ after which the NMOS will be off, NMOS goes into the cutoff after $V_{dd} - V_t$ only PMOS transistor will be on. The channel of the PMOS will be there to charge the output from $V_{dd} - V_t$ to V_{dd}.

From 0 to $V_{dd} - V_t$, NMOS will be on, so 0 to $V_{dd} - V_t$, PMOS will be on. Beyond that from $V_{dd} - V_t$ to V_{dd} only PMOS will be on NMOS will be off. The PMOS conducts or consists of a channel or has the channel path for charging the capacitor from 0 to V_{dd}, whereas the NMOS conduct only for only from 0 to $V_{dd} - V_t$.

The NMOS transistor and the PMOS transistor is going to conduct is going to charge the capacitor really fast from 0 to $V_{dd} - V_t$, beyond which $V_{dd} - V_t$ to V_{dd} only PMOS transistor is available NMOS transistor will be cut off. However, the transmission gate now because both the transistors are in parallel are stacked in parallel and both the channels are available for the capacitor to charge, it actually passes logic 1 successfully. If you remember NMOS transistor was passing the degraded logic, but the transmission gates makes use of the PMOS transistor which is passing the successful logic 1 alright.

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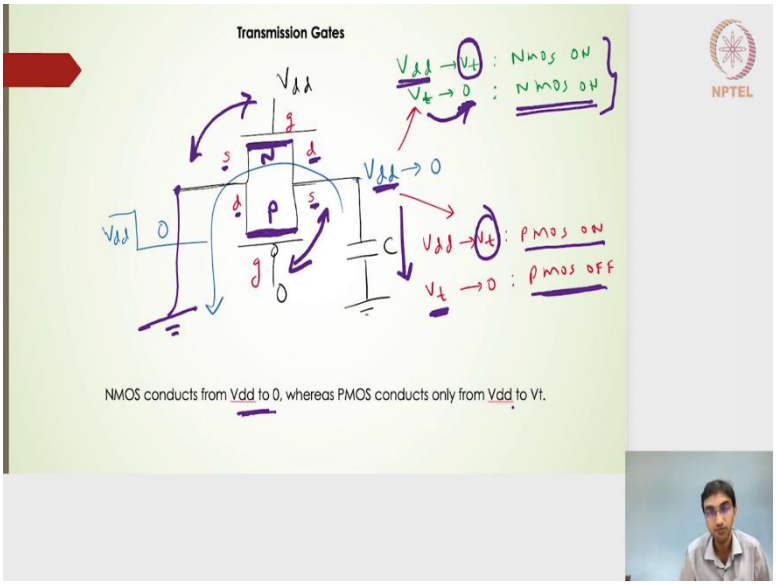

Let us have a look at the transmission gate for the logic 0 passing. On this particular terminal, if I switch off the power supply, I will get again a 0 voltage here. This particular terminal is now connected to the ground and let us say that the capacitor is completely charged to V_{dd}. For an NMOS whichever potential is higher that will be considered as drain, that is why I have written drain here and then the source here.

V_{gs} will always be V_{dd}. This channel which has been formed does not have any effect for the NMOS transistors. The capacitor sees a path here and then it discharges, because this part is only dependent on this V_{gs} value and not on the capacitor discharging profile, not on the capacitor voltage which is continuously decreasing because of its discharging path. At any point of this discharging, this particular path does not have any effect. The path is always there for the discharging of the capacitor on the NMOS side.

On the PMOS side whichever one potential is higher on the PMOS side, whichever potential is higher on these two terminals that will be called as the source terminal. Initially it is a V_{dd}, it will be called as s, the other one which is connected to the ground is called as the drain.

The V_{gs} value now as the capacitor discharges, there will be a path initially till the capacitor voltage decreases to V_t till that time there will be a path beyond that the PMOS will not have a path because the V_{gs} value now will be less negative than that of -0.3.

What we have is exactly a symmetrically opposite situation as that of for the logic 1 which we had seen earlier. The NMOS path is available from V_{dd} to ground to 0 volts. So, from logic 1 to logic 0, the NMOS path is available, whereas PMOS is available initially right from $V_{dd} - V_t$. Beyond V_t, PMOS is off.

Similarly, to the last one where there will be a discharging path, both the paths are available the PMOS and NMOS, and thereby the discharging rate will be higher the time taken for the capacitor to discharge till the V_{dd} to V_t will be really faster because both the transistors are on V_{dd} to V_t, beyond V_t only NMOS transistor is on.

Beyond V_t, on the NMOS transistor will be the path made by the NMOS transistor will be made available the PMOS will be off. The NMOS conducts from V_{dd} to 0, whereas the PMOS conducts only from $V_{dd} - V_t$.