Design and Analysis of VLSI Subsystems
Dr. Madhav Rao
Department of Electronics and Communication Engineering
Indian Institute of Technology, Bangalore

Lecture - 12
Skewed Inverter

Hello students, so welcome to this particular lecture on the Skewed Inverter. So, till now we had seen an inverter characteristic, the CMOS inverter which is made up of the PMOS and NMOS transistors, where the β of the PMOS and NMOS were same. Thereby we were able to evaluate the current intersection points, which was then put it into the transfer characteristics.

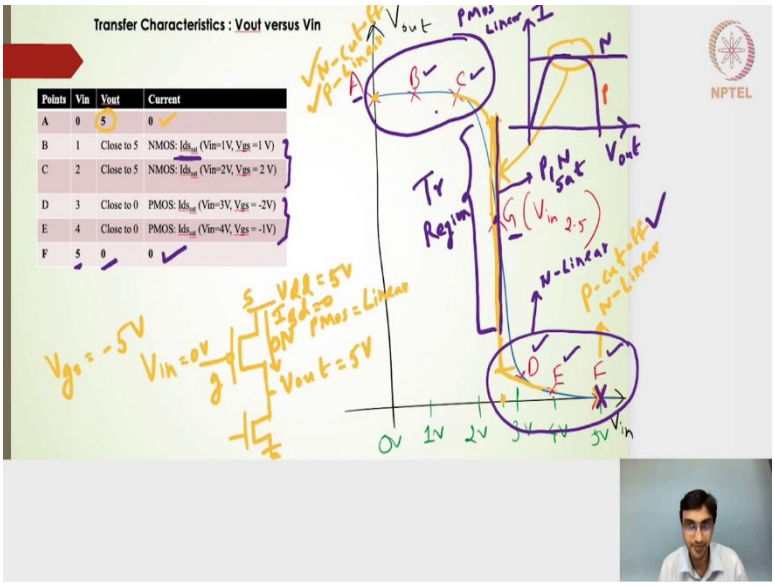
So, if you remember the intersection points came from the current and the voltage characteristics of the PMOS, intersecting at that of the current and the voltage characteristics of the NMOS. So, for the given input voltage along the output voltage line the current points which were intersecting.

So, those became the solution points for the CMOS inverter, which is made up of PMOS and NMOS transistors. So, those intersection points gave us the input voltage. I mean given the input voltage gave us those intersection points, gave us the current as well as the output voltage values. Those particular points were then put it into the transfer characteristics, which is made up of V_{out} in the y-axis and V_{in} input voltage in the x-axis and then thereby the transfer characteristics was drawn for the CMOS inverter. So, this is what we had seen in the last lecture.

Today in this particular lecture we will go over slightly modifying, if you have a modified inverter; modified inverter in a sense, if the width of the PMOS or NMOS is different than that of the other transistors, then the β if it is not same. What is likely to happen to the transfer characteristics. That is why, if the β are not same that is called as a skewed inverter. If the β are same then it is called as an unskewed inverter.

The unskewed inverter is what we had seen in the last lecture and today we are going to look into the skewed inverter where the β will not be the same.

(Refer Slide Time: 02:28)



Moving ahead, just a revision of what we had done in the last lecture is the transfer characteristics of the Vout versus the Vin is drawn, these were the intersection points. A, B, C and then D, E and F where the intersection points which we had clearly drawn. Where the current of the PMOS and the current of the NMOS were actually intersecting and then those points we labeled it as A, B, C, D, E. From those particular points we got two values, one is the current value and then the output node values.

Voltage values for a particular input voltage and we have chosen six input voltages: one is 0 volts, second is 1 volts, 2 volts, 3 volts, 4 volts and the 5 volts and thereby we get this six intersection points. The 7th one which is a G point, here is the intersection points for the input voltage of 2.5 volts, when the β are same. For a 2.5 volts, we realize that the G point is actually not a single point, it is actually a series of points because of the saturation currents. If I want to draw the PMOS, so, this is my PMOS for the current versus the V_{out} of the inverter and for the NMOS this is the value, this is the particular profile. So, this is the PMOS profile. So, let me draw this is PMOS and this is NMOS. So, this intersection points, the series of intersection points is what is giving me this particular profile. In fact, I have drawn it little bit kind of a slope line, it should not be a slope line it should be a straight line, straight line along the point G.

The transfer characteristics should actually look something like this. So, that is the intersection series of intersection point. I have picked one point of G, where the input

voltage is 2.5, where we will get the output node voltage a series of values. This is called as a transition region. So, just to summarize the points A, B, C and D, F what we are saying is now the point A here so, if you remember the point A in the previous slides of the previous lecture you will notice that the point A was on the extreme side of the IV characteristics.

The extreme side of the IV characteristics represents the point A was actually touching the x-axis line. The point A was when NMOS transistor was in cut off. I am going to write it as NMOS was in cut off and the PMOS we had it in linear region. The intersection of those two current lines give me the point A, similarly point F.

This particular point is exactly the opposite, where I had F point was actually lying on that 0 voltage point in the IV characteristics profile. This F point is, where the PMOS is in cut off and NMOS was in linear region. Let us come back to point A, PMOS is in linear region and NMOS is in cut off is what we are claiming.

NMOS is in cut off, now let us try to evaluate or validate whether our claim is correct. NMOS should be in cut off for point A. The point A is a point, where the input voltage was 0, that means the NMOS V_{gs} value was 0 and thereby it is validated that the NMOS will be in cut off. PMOS although its line looks like a linear region. In fact, if the V_{in} is 0, V_{gs} turns out to be -5 volts is that correct?

Let me draw the PMOS and if V_{in} is actually 0 volts, s is nothing but V_{dd}. So, this is nothing but, we had considered 5 volts here and this is my output voltage. So, let us forget about the NMOS time being, we have validated NMOS should be in cut off for input is equal to 0, for PMOS I am claiming that it is in linear region, but let me have a look at it V_{gs}, this is g for the PMOS this is s for the PMOS.

V_{gs} turns out to be -5 volts, that means V_{sg} is +5 volts much much above than the V_t of 0.3 volts or rather much much negative than that of the -0.3 volts. Thereby this PMOS transistor will be ON. Whenever it is V_{gs} or with respect to V_{sd}, if it is V_{sd} is much much greater than the mod of V_{tp} which is 0.3 volts, then we say that the PMOS is ON. It means that it should be in either linear region or the saturation region right.

At point A, the output voltage node, what I have stated here in the table it is 5 volts and these 5 volts is actually coming from the intersection points, which we have seen in the previous lecture.

The point A which was actually on that particular x-axis line at that particular V_{dd} point and we got the V_{out} to be 5 volts. Although the PMOS region is in linear, this particular PMOS I am writing it as to be on transistor, which is also in linear region. The output voltage is 5 volts, V_{dd} is 5 volts, the current here that is flowing from the source to drain should be 0, I_{sd} should be 0. Because, both the potentials or terminals have a potential of 5 volts. So, both the terminals have the same potential.

The current V_{ds} or V_{sd} for the PMOS is actually 0, so the linear region current whatever we have the expression, if I put V_{sd} to be 0, I will get the current to be 0. So, our claim of PMOS to be in linear region is validated, although the current value is 0 and this is what is shown in this particular table.

Similarly for this particular point F, for point F we say that our claim is NMOS is in linear and PMOS is in cut off. PMOS is in cut off because V_{in} is 5 volts. If V_{in} is 5 volts V_{sg} or V_{gs} is 0. So, it is not above 0.3 volts or not beyond -0.3 volts in whatever terms you take whether it is V_{sd} or V_{gs}.

The PMOS is in cut off, that is validated. NMOS is in linear regions, the V_{in} is 5 volts. So, V_{gs} for the NMOS is greater than 0.3 volts and thereby the NMOS will be above the cutoff region. So, it will be either in linear region or the saturation region.

Again, if I pick this V_{out} voltage, it is 0 volt. So, the output voltage is now 0 volts, the other terminal of the NMOS is also ground. The V_{ds} potential difference between the drain and source of the NMOS transistor is the same or rather the potential difference is 0. The current that is flowing in the NMOS transistor will now be 0. That is what we are getting here.

For the other points for the points B and C, if you remember the B and C points was actually closer to the 5 volts. B and C points were on the right side of the IV characteristics and the D and E points were actually on the left side of the IV transfer characteristics right. The B and C points were on the right side, what it implies is the B and C points where the

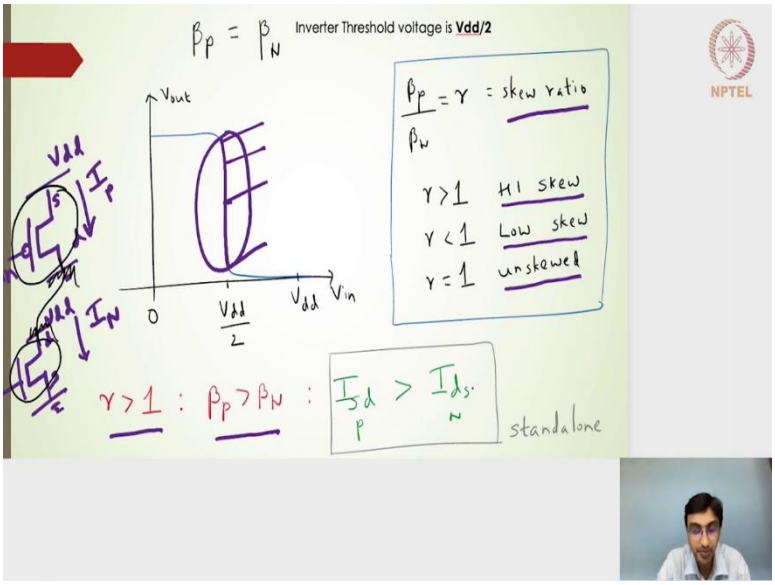
intersection points coming from the linear region of the PMOS and the saturation region of the NMOS.

The saturation region of the NMOS, that is why I have written the current of saturation of the NMOS equated it to that of the linear region of the PMOS current, for both B and C. Similarly for D and E, for an unskewed inverter means when the β are same. The D and E are symmetrically on the opposite side as that of B and C and D and E which is closer to the 0 volts now.

What we can say is the D and E is those points are arrived from when the PMOS is in saturation region and NMOS is in linear region. Those two currents, one in the saturation and another one in the linear region, if we can find out the solution, then we will get the points D and E for those particular values of the input voltage. So, this particular profile or this particular region above the transition region. This is I will call it as the transition region. Above the transition region, this is where we will have the PMOS to be in linear region. And then this one, this particular region below the transition region, the points D, E, F is when the NMOS will be in linear region.

During the transition region, the transition region can be characterized as the intersection points in the IV characteristics, where both the transistors are in saturation region. In this particular region it is both the PMOS and the NMOS are in saturation region. So, I am going to write it as P and N as saturation region. Hope this is clear. This is the transfer characteristics of the unskewed inverter.

(Refer Slide Time: 13:42)



Let me proceed further. If I have $\beta_p = \beta_N$, it is an unskewed inverter we have this particular transfer characteristics. This transfer characteristics is more appropriate because this becomes a very very straight line. The point G whatever I had drawn previously which is actually nothing but for an input voltage of 2.5 volts, it will give me the series of this points.

There is no one particular G point, it should give me a series of the output values for a particular input voltage value. If I apply an input voltage of 2.5 volts, I might get this particular value as the output voltage or I might get this one as the output node voltage.

Now, what happens if you know the β are different? That is what is the crux of this particular lecture. What we are going to do is, establish a different label called as skewing ratio. The skewing ratio is nothing but the ratios of the β, the β of the PMOS and the β of the NMOS, remember that the β are nothing but a function of the width, the PMOS width and then the NMOS width. Although the skewing ratio is nothing but the ratios of the β of the PMOS and NMOS which are used to construct the inverter. We can have a skewing ratio for different combinational circuits for a different standard gate also, that we will see look into the in some of the future lectures. But at this point of time the β of the inverter. The β of the PMOS transistor and the β of the NMOS transistor, the ratio of that which is used for drawing or designing the inverter is called as the skewing ratio.

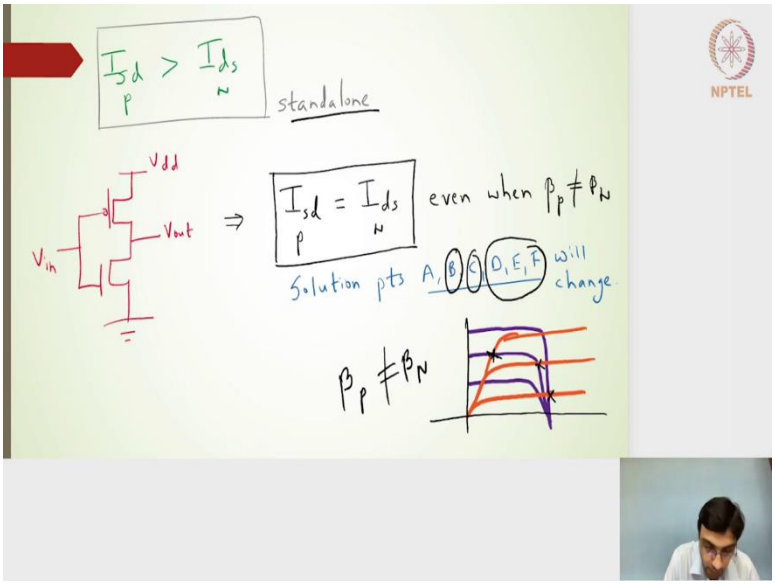
If $r = 1$ it is called that is an unskewed ratio; that means that the β are same and that is why it is called as an unskewed inverter. If $r < 1$, that means PMOS β is less than that of the NMOS β and that is called as a low skew. If $r > 1$, if the skewing ratio is greater than 1, that means that the $\beta_p > \beta_N$, that is called as the high skew ratio.

If $r > 1$, it is called as an high skew that is what is mentioned here, that means that the $\beta_p > \beta_N$standalone. If it is not an inverter, if I have a standalone PMOS transistor, let me draw a standalone PMOS transistor. PMOS with a bubble and then let me say, that this is input, this is my source and this is I will just ground it, instead of connecting it to the NMOS transistor, because it is a standalone transistor. Similarly, I will draw an NMOS, which is nothing but V_{in} again a V_{dd} here and then a ground of course, this will be drained for the NMOS and then this will be a source for the NMOS.

If I have this β_p to be more than β_N. The current here, what I am drawing from the PMOS, the current of the PMOS will be greater than the current of the NMOS. So, that is what I have stated here right, but if I actually put these two transistors together. So, let me pick up another colored pointer. If I have these two transistors and then this particular transistor, so, if I disconnect this ground and V_{dd} and then connect it here; the currents of these two transistors, which are in series should be same. Although the β are different, if I connect it in series, I will get the same current.

So, that is why I have written, if I have a β to be different and as a standalone transistor, the current what we are expecting from the PMOS and what we are expecting from the NMOS, the PMOS current is likely to be greater. If I apply the same voltage same V_{gs} value in fact and then the same V_{ds} is given, then I am expecting a more current from the PMOS.

(Refer Slide Time: 18:28)

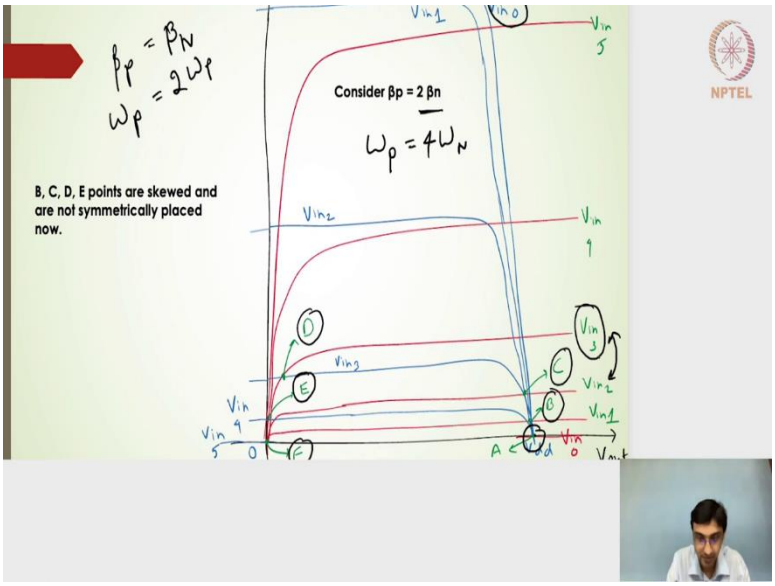


Again, just to reiterate that the same expression. I have written, the PMOS current is likely to be more in a standalone transistors. That is what I have written, but when you are connected in series to form the inverter, we have to satisfy the Kirchhoff's current law. This particular value or the currents being same has to satisfy.

Even when the β are different, standalone the currents will be different, but when they are put together in an inverter the currents will be equal. We will get of course, very similar to what we had seen in the last lecture. We will get the intersection points, if we apply the input voltage of 0, we will get the intersection point of A, if we apply the input voltage of 1 we will get the intersection point as B, If we apply the input voltage of 2 volts, we will get the intersection point as C, if we apply the input voltage of whatever 3 volts, 4 volts and 5 volts we will get the intersection points as D, E and F. Of course, those intersection points, that position of those points in the IV characteristics means what we have seen in the last lecture, let me draw a different one.

The PMOS current and if I draw the NMOS current something like this, so this intersection points, here and somewhere here. This particular points might be different now, because it is a skewed inverter. The β are changed. The β are not equal, those intersection points where we had the β to be same. Those positions of the intersection points will be different now. So, hope you are able to understand.

(Refer Slide Time: 20:35)



I have drawn this particular profile, when the β_p is actually twice that of the β_p and one way to do this is, if it is twice or rather if $\beta_p = \beta_N$, whatever we had seen in the last lecture. We wanted to make this PMOS width to be twice that of the NMOS width. If I want to make the $\beta_p = 2\beta_N$, I will make my PMOS width to be 4 times the NMOS width. And that is where we will get the β_p to be equal to that of twice that of the β_p and if I draw the IV characteristics now.

For this particular V_{in} of 0 line, for the PMOS IV characteristics, but this particular linear region is sufficient enough and it will actually proceed. So, if I pick the blue color. So, if I you know somewhere here i will draw. Coming back to my black pointer for V_{in} of 1, I get this particular blue line, for V_{in} of 2, I get this particular blue line, for V_{in} of 3, I will get this particular blue line and then V_{in} of 4 and V_{in} of 5. Following V_{in} of 5, the PMOS will be in cut off. So, the line or the IV characteristics line will be nothing but the x-axis line.

Similarly, the input voltage, the IV characteristics of the NMOS transistors, for V_{in} of 0 is this particular x-axis line, V_{in} of 1 we have this particular line. V_{in} of 2 I have this particular line, V_{in} of 3 is this particular line, V_{in} of 4 is this particular line and then V_{in} of 5 is this particular current line.

Notice that, earlier for an unskewed inverter, V_{in} of 0 the saturation current of V input of 0 was matching with the saturation current of the Vinput of 5. Similarly the saturation current of Vinput of 1 was matching with that of the saturation current of V input of 4, what it really means is the saturation current is nothing but the highest current or the constant value.

Those levels, the constant values of the V_{in} of 1 in the PMOS and the V_{in} of 4 of the NMOS are actually matching. V_{in} of 1 is actually nothing but V_{gs} or V_{sg} of PMOS to be 4 volts and V_{in} of 4 for NMOS is nothing but 4 volts. So, if I have the V_{sg} or V_{gs} to be same and β to be same then I am likely to get the same current.

But now because the β are different the saturation currents, now the maximum level of the currents for the PMOS and for the NMOS are different and that is why we will get the levels to be different. In that particular case, I will still be able to get the intersection points of B, C or rather A, B, C, D, E, F.

It is still the same in a graphical analysis for the same input voltage of 0, wherever the current of the PMOS intersects with that of the current of the NMOS we will get this particular point A. Similarly, for input voltage of 1, wherever the PMOS current is intersecting with that of the NMOS current we will get this particular point B.

Similarly point C for the input voltage of 2, a point D for the intersection point D for the input voltage of 3, point E and point F for the input voltage of 4 and 5 volts respectively. It is very very similar to what we had seen for an unskewed inverter, but if you look into this closely the points B and C for an unskewed inverter was symmetrically placed, was symmetrically a mirror image of those positions in the IV characteristics.

Whereas, in this particular case, because of the skewness of the β, the current magnitude of the current is slightly skewed now of the PMOS and NMOS in the IV characteristics. Thereby the positions of the B, C does not match to the positions, does not match to the positions of the E and D. What I mean by the positions means, the levels of B and C does not match with the levels of E and D. E and D are slightly above than that of the B and C. For the β to be higher, the D and E points right are slightly higher, not only higher, they are slightly away from the 0 volts, then when it was in the unskewed inverter C and B points.

In this particular case, when the β is more twice that of the β_N, the β PMOS is higher than that of the β of NMOS. The C and B points are now actually closer much much closer to the 5 volts. E and D points are now slightly moving away from the 0 volts.

So, this is something, once you should be able to draw it for the unskewed inverter and then skew inverter you should be able to notice this and appreciate it. Hope you know this is understood, so, moving ahead. One more point here I wanted to emphasize is in an unskewed inverter, the point G if I applied in an unskewed inverter when V_{dd} was 5 volts. If I apply input voltage of 2.5 volts, I should be able to get the series of the intersection points. As a series of intersection points, which means that the PMOS saturation current is intersecting with that of the NMOS saturation current and then those particular intersecting series points where is nothing but, our transition line in the transfer characteristics.

In this particular case, when it is now skewed, the standalone PMOS current will be higher than that of the standalone NMOS current. In fact the standalone PMOS current the PMOS current the standalone PMOS current in the saturation region if I look only into the saturation region it will be high right.

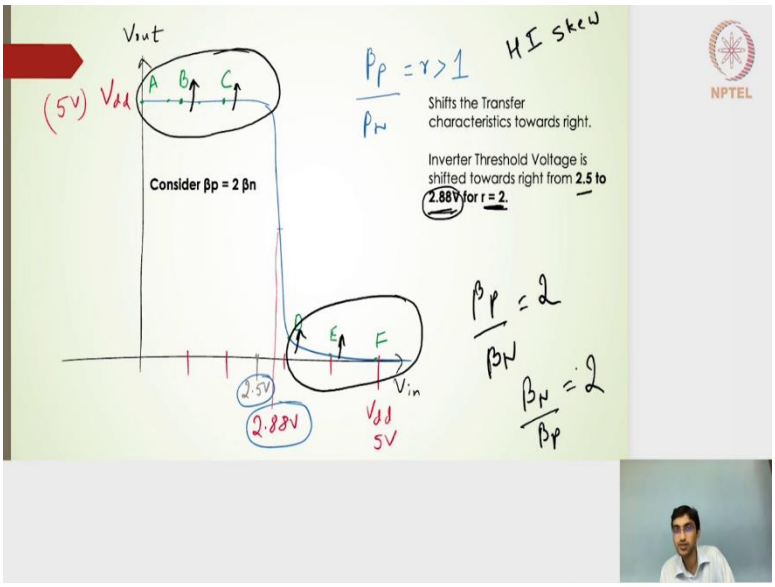
So, what it means is for an input voltage right, which is less than or rather for the input voltage you know for the input voltage to be higher than 2.5 volts for an input voltage above 2.5 volts or somewhere between 2 and 3 or closer to the 3 volts. I should be able to draw a line of the current line of the PMOS, the current line of the NMOS and at that particular point we should be able to establish a series of the intersection points in the saturation region.

If I draw actually in this particular skewed inverter of $\beta_p = 2\ \beta_N$ and if I draw the 2.5 volts input voltage on the PMOS current line and then the NMOS current line. I will actually not get the intersection point, I mean in fact I will get only one intersection points and not a series of the intersection points.

In fact, that particular intersection points if I draw, V_{in} of 2.5 volts that particular intersection points will be the point where the PMOS will be in the linear region and NMOS will be in the saturation region. In fact, the 2.5 point will actually be shifted somewhere along this particular side, where it is the intersection point is closer to the 5 volts, because it is skewed now, the threshold or the transition region does not fall in the input voltage of 2.5 volts.

If I want to derive the series of the intersection points, it will be the input voltage which is closer to the 3 volts and higher than 2.5 volts. We will look into it, what exactly will be that particular input voltage, where we will get the series of the intersection points.

(Refer Slide Time: 29:32)



In the last slide we had got the points of A, B, C, D, E, F. Reflecting those points into the output versus the input profile, this is what I will get A, B, C and then I will get D, E, F. Remember that A, B, C is now much much closer to the 5 volt. It is in fact, if I look into this particular transfer characteristics of an unskewed inverter this point B has slightly moved above its position, when it was in the unskewed inverter.

It is slightly moved above, but yet it should be lower than the 5 volts. Similarly, C point slightly moved above, D and E points are now closer or rather it should be away from the 0 volts. Again, so this particular D point and E point away from the 0 volt. It is slightly moved above its own position when it was an unskewed inverter alright.

What it really means is, if it is a high skew inverter, which is nothing but the ratios, the skewing ratio is greater than 1. Then the transfer characteristics is actually shifted towards the right and the inverter threshold voltage because I have done some calculation which we will see later. It actually moves from 2.5 volts to 2.88 volts.

So, do not worry about this particular value you should be able to calculate it as in the future slides, we will derive that particular expression, but for time being, let us assume

that this value is correct 2.88 volts. For the skewing ratio of 2, then this particular transfer characteristics around the 2.5 volts which has been shifted to 2.88 volts.

The more regions are there in this particular transfer characteristics of the output versus the input. For the more value of the input voltage, the output stays at 5 volts or closer to 5 volts and for the less points of the input it stays at 0 volts or closer to 0 volts.

The β_p if it is more than β_N, in this case it is 2, β_p is more than β_N what is doing is, it is pulling most of the input voltage to the 5 volts, because β_p which is more dominant. The PMOS is more dominant. So, it is going to pull away most of the points closer to the 5 volts, most of the input voltage closer to the 5 volts and the less number of input voltage, the NMOS is able to pull it closer to the 0 volts.

Similarly, if $\beta_N > \beta_p$, then β_N or the NMOS is more dominant. So, it is going to pull most of the input voltages closer to these 0 volts. PMOS is a weak transistor in that particular case. It will have less number, it will be able to push less number of input voltage to the 5 volts.