Design and Analysis of VLSI Subsystems
Dr. Madhav Rao
Department of Electronics and Communication Engineering
Indian Institute of Technology, Bangalore

Lecture - 11
Transfer characteristics of Inverter

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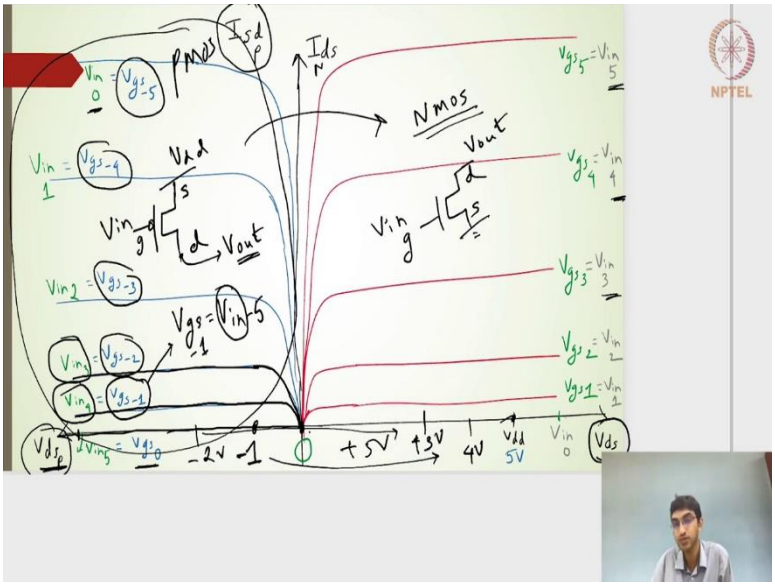

In the last lecture we had seen the NMOS. As an inverter, the NMOS and the PMOS transistors in series and if you want to find out the solutions graphically, you know the way we wanted to do graphically is to avoid understanding of whether it is in saturation region or linear region.

So, if we do not have that kind of an information, at this point of time what we will do is we will draw the graphical analysis. Where we will draw the profiles of you know the current versus the voltage profiles of the NMOS transistor. Then try to draw the PMOS transistors current and the output voltage profile and wherever those current profiles are intersecting those will be our solution points.

The V_{ds} is nothing but the V_{out} and then this V_{ds} is nothing but the V_{ds} of the NMOS. we had drawn this particular NMOS profile assuming that the NMOS is a standalone transistor. So, it is not connected to the PMOS where one side of the NMOS, you know if I draw this it is nothing but the gate which is connected with the V_{input} voltage and then

this one is nothing but the source, this one is nothing but the drain and the drain is connected to the output node V_{out} and the source is connected to the ground. And that is what we have drawn the profiles of the NMOS transistor which is the current versus the V_{ds} profile.

Similarly, if I want to draw for the PMOS transistors, on one side we have gate and on this side we have it the drain of the PMOS and then on this side we have the source of the PMOS, where the source is actually connected to the V_{dd} rail and the drain is actually connected to the V_{out} of the inverter. If I make this particular you know pick those particular PMOS transistor, specific PMOS transistor in the inverter and make it as a standalone PMOS transistor, where it is connected to the V_{dd} rail, where the input is fed to the gate of the PMOS transistor and this is the output node and if I do the transfer characteristics with respect to the V_{in} V_{out} and then V_{dd}. To begin with for a standalone PMOS transistor, which is connected to the Vdd and then connected to the terminals V_g s and d. So, this is what I get.

So, the blue lines with respect to the V_{ds} of the PMOS, this is my current profile. The I_{sd} is a positive value for the PMOS, the source to drain is a positive value. Similar how I get the drain to source of the NMOS is positive. The I_{sd} is the current which is a positive value with respect to the V_{ds} of the PMOS. Remember that the source is always at higher potential than that of the drain.

So, if I am writing this V_{ds} of the PMOS, that means, the x-axis is actually negative. So, as I go negative and negative for the V_{ds} of the PMOS, my current will be higher.

In fact, for the PMOS it is very very replica of the NMOS. If I write the V_{ds} of the PMOS because V_{ds} turns out to be negative. So, it will be a mirror image of this particular red lines which is nothing but, representing the NMOS current, the blue lines represents the PMOS current.

So, as it is going the V_{ds} value is going more and more negative, it is going to start from the linear region and then go to the saturation region. So, for a specific value of V_{gs} of 0 volts, for a specific value of V_{sg} of 1 volts, V_{sg} of 2 volts, V_{sg} of 3 volts, V_{sg} of 4 volts and V_{sg} of 5 volts.

See remember that I have stated it as V_{sd}, although I have written it as V_{gs}. So, if V_{sd} is actually 0, the V_{gs} is also 0. What it means is, if V_{sd} is 0, if it is less than $|V_t|$ of PMOS which is 0.3 volts then the current will be 0. So, that is why, for a V_{sd} of 0 the current is nothing but the same line as my x-axis and if the V_{sd} is 1 that means, V_{gs} is minus 1 volts, I will get this particular profile linear region and then it goes to the saturation.

If V_{gs} is minus 2 that means, V_{sg} is plus 2. Then, I will start with the linear region and then, it proceeds to the saturation region. Similarly for a higher values of V_{sd} of 3, 4 and 5 that means, for a negative value of V_{gs} of minus 3, minus 4 and minus 5, I will get more currents. So, the more linear region and then saturation, more linear region saturation and linear region and saturation, hope this is clear. So, the notations I have just slightly changed it and you will know the reason why I have slightly changed it. If my V_{gs}, if my V_{gs} is minus 1 volts. So, V_{gs} is actually, if I can rewrite it here, V_{gs} is nothing but $V_{in} - V_{dd}$ which I have taken it as 5 volts. If V_{gs} is minus 1 volts here, so the input voltage will be nothing but positive 4 volts. So, I have rewritten this expression as V_{in} of 4 volts this is my current profile.

Similarly, if V_{gs} is minus 2 volts, input is 3 volts, so my profile of the current is nothing but this. If input is 2 volts; that means the V_{gs} is -3 or V_{sd} is +3, I will get this particular profile and then similarly V_{in} of 1 represents of -4 volts that is what my profile will be and V_{in} of 0 gives me V_{gs} of -5 or V_{sd} of +5 which is this particular profile.

So, what I have done here is, input side I have the profile of the current versus the V_{ds} for the PMOS. The current versus the V_{ds} for different values of V_{gs} or V_{sg}, I have re-written in the form of the input voltages. Remember on this side also, I have stated the different current versus the V_{ds} profile of the NMOS in terms of the V_{in} voltages.

So somehow, I bring this particular portion this whole PMOS. PMOS current profile versus the V_{ds} value into this side, I will get, for a similar value of V_{in}, I will get the intersection points. So, that will be my solution for the inverter which is formed from the NMOS and the PMOS transistors which are in series. Now, notice that this V_{dsp} here is in x-axis, V_{ds} of NMOS is also in x-axis.

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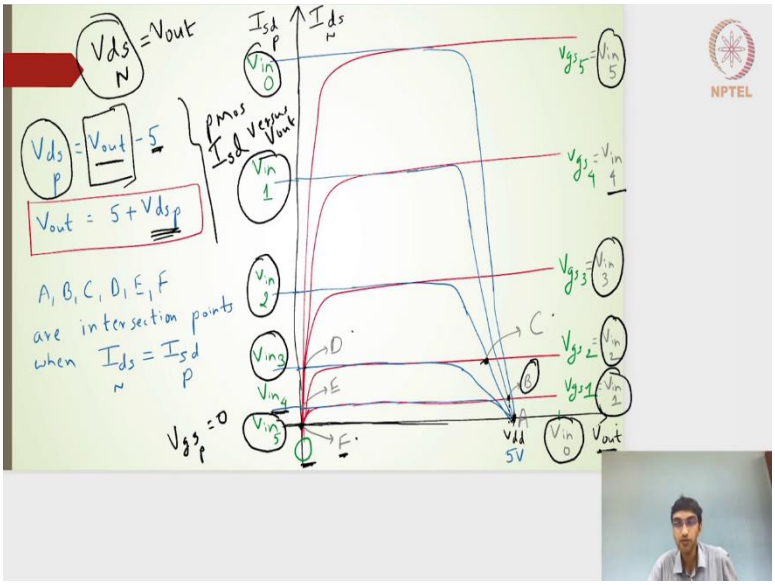

So in the next slide, V_{ds} of PMOS, I mean, I will just write it as V_{ds} of NMOS is nothing but $V_{out} - 0$, so it is V_{out}. If you remember the V_{ds} of PMOS is nothing but the drain side it is connected to the output and the source side is connected to the V_{dd} which is 5 volts. So, it is $V_{out} - 5$ volts. So, if I want to bring whatever the profile I had on the negative coordinates system. For example, this second coordinate system. If I want to bring it here, what I have is the V_{dsp} which is nothing but V_{ds} of the PMOS is $V_{out} - 5$ volts. So, we have drawn the profile with respect to V_{ds} of PMOS and if I want to shift or rather if I want to draw that particular profile in terms of only V_{out}.

So, this V_{out} turns out to be nothing but $5 + V_{dsp}$ and where this V_{dsp} or rather you know V_{out} is nothing but $5 + V_{dsp}$. So, if I can redraw the PMOS current versus the voltage profile in terms of you know for the PMOS. If I can draw the current I_{sd} versus V_{out} right, currently what we have is I_{sd} versus V_{ds} of PMOS, but what we want is really the I_{sd} current with respect to the V_{out}. So, the way we have the I_{sd} versus the V_{ds} of PMOS, but to draw I_{sd} with respect to the V_{out} profile I need to shift the profile by 5 volts. So, going back to this particular slide, whatever I have this particular profile of the PMOS, whatever I have this is the PMOS profile.

If I want to draw this particular profile in terms of V_{out}, not in terms of V_{ds} of p. I need to add +5 volts. So, every point here, if it is 0 point here, to change it into V_{out}, it will be nothing but 0 + 5 volts. So, it will be somewhere.

Similarly, if it is nothing but 1 volts here, so it will get minus 1 volts here, it will get shifted to +4 volts here. If it is -2 volts here, it will get shifted to a +3 volts here, because I am doing +5. Similarly, so -5 volts here will get shifted to 0 volts. So, the whole entire I-V characteristics of the PMOS will get shifted by 5 volts right towards the positive x-axis.

So, what we have now is, this blue line getting shifted. Earlier we had it in the second coordinate system, now it is in the first coordinate system. Because, I have made the PMOS current profile with respect to the V_{out} and if I want to do the same for the NMOS, NMOS V_{ds} of NMOS is nothing but V_{out}. So, the same x-axis is nothing but replace by instead of V_{ds} of NMOS it is now replaced by V_{out}.

For different values of V_{in}, on the red line represents the NMOS characteristics. The blue line represents the PMOS characteristics shifted. So, that I will be able to draw/ visualize the current of PMOS and NMOS with respect to the same V_{out} axis. Which remains the same for both NMOS and PMOS and the input is also the same now V_{in} 5, 4, 3, 2, 1. Now, I should be able to see both the current profiles with respect to the output node voltages for a specific input voltage on the same coordinate system. So, it somewhere it will intersect.

Let us say input of 1 volts, the PMOS is this particular blue line, NMOS input is one here. So, there is a linear region and then it goes to the saturation region. So, the intersection points here for the blue line of input of 1 volt and then the red line of input of 1 volts is this particular point the B point.

Where the currents of the NMOS and then PMOS for the same input voltages are the same. For the input voltage of one, the current of the PMOS should be the current of the NMOS in an inverter. So, that is nothing but the B point. So, if I actually drop this B point, if I actually find out what should be the output voltage the x-axis reflected point of in the x-axis will give me the output voltage of the B point.

Similarly, if the input is 2 volts, the blue line input of 2 volts, the red line input of 2 volts here, it will be nothing but intersecting at C point. So, the C point will give me the y axis reflection will give me the current of the inverter and the x axis reflection will give me the output node voltage.

Similarly, if the input is 3 volts, I will get the intersection point as D and then, similarly for the input of 4 volts, here the intersection point will be point E. If it is 0 volts you can see that it is actually 0 volts the NMOS current is anywhere 0.

So, the PMOS current should always intersect at the 0 line. So, the point A is nothing but having a current of 0 line and then, it will have the output voltage is nothing but the V_{dd} of 5 volts.

Similarly, if the input is 5 volts, which is nothing but V_{dd} value. We can notice that, for an input of 5 volts here, the red line will intersect with the blue line, which is anyways you know, if the input is 5 volts, V_{gs} of the PMOS is actually 0 or V_{sg} of PMOS is actually 0 volts. Which is less than the 0.3 volts and thereby the current is nothing but this particular line. It will intersect for an input of 5 volts, it will intersect at this particular F point, where the current is 0 and the output voltage is 0 volts. So, this becomes the A, B, C, D, starting from A, B, C and then D, E, F, will give us the intersection points or the solution point. Solution in the sense for the inverter what should be the current and what should be the output node to a voltage, for different values of the input voltages, that has been applied to the inverter.

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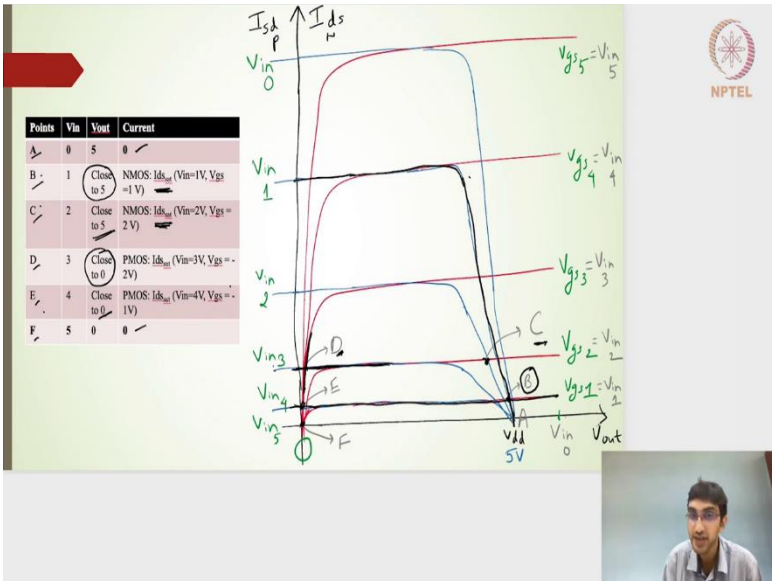

So, to be very very specific with respect to the points A, B, C, D, E, F. I have drawn a table here. So, the profile is nothing but the same, the input NMOS current profile with respect

to the V_{out}, PMOS current profile with respect to the V_{out} for different values of input voltages, the intersection points give me A, B, C, D, E, F.

So, this intersection points have now written down A, B, C, D, E, F. For the input voltage of 0, I will get the intersection point as A, for input voltage of 5 volts, I will get an intersection point of F. For an input voltage of 1, 2, 3, and 4, I will get the intersection points as B, C, D, E respectively.

Now, output voltage also has drawn it, although I do not know the exact value, what I have stated is the intersection point B. So, this particular point B, it is actually very very close to the V_{dd} of 5 volts. So, that is what I have stated here close to the 5 volts. Point C is actually very very close to this particular point again very very close to 5 volts and not to 0 volts. So, it is close to the 5 volts. So, that is what I have stated here. Point D here is actually close to 0 volts and not to the 5 volts. So, that is what I have stated here close to 0 volts and point E is also close to 0 volts. Let us try to find what is the current?.

The current of A and current of F is anyway 0. So, that is what I have stated here, current of A and current of F is 0. Current of B, so the current of B here so this is my intersection point. For the NMOS side it is the saturation current, which is intersecting with this particular blue line, although I have now made it black. But this particular blue line, the earlier blue line was nothing but the linear region. So, at point B it was actually the PMOS was in linear region, NMOS was in saturation. If I want to find out what is that particular current. I can actually go with point B, the I_d saturation of the NMOS and find out that particular current value. It is nothing but, the I_d saturation current of NMOS equated with that of the I_{ds} of the linear current of PMOS.

Point C is also the same, we have the NMOS saturation current, equated with that of the linear current of the PMOS, I will get the point C. Similarly, D is nothing but the PMOS saturation current. The PMOS saturation current here equated with that of the linear region where D is nothing but V_{in} of 3 here. So, this is my linear region of the NMOS and then the saturation region of the PMOS. E is also the same, PMOS saturation region equated with that of the saturation region of the PMOS equated with that of the linear region of the NMOS. Then, point F is nothing but 0. So, if I look into this B and C it is nothing but saturation region of the NMOS equated to that of the linear region of the PMOS for a particular value of the input voltage. Point D and E is nothing but the saturation region of

the PMOS equated with that of the linear region of the NMOS for a particular value of the input voltage will give us those points.

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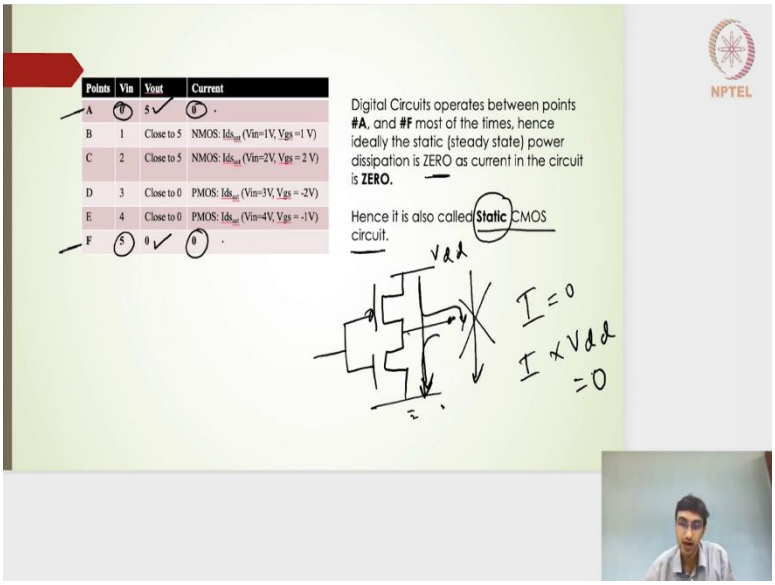

So, hope this is clear. Remember in most of our applications, we will always have the input voltage at A or F. In fact, input voltage at 0 or 5 point. So, my solution points are always A and F. So, the current if you look into the current for the points A and F which is always 0.

In a steady state operation of an inverter, steady state implies that, once the input is given and after a certain time is over, after the transition is over, the output voltage will be either 5 volts or 0 volts in a steady state voltage. Then, the steady state current is actually 0 in both the cases. Now, that is a very significant point or an advantage or a benefit for the CMOS transistors. So, the CMOS based circuits, whether it is an inverter or a NAND gate or a NOR gate or any such combinational circuits, ideally the current is zero in a steady state. Hence this particular topology or this particular CMOS, where the CMOS circuits or the compound or the combinational circuit is placed within the Vdd and 0 rail or ground rails. So, those particular topologies we call it as the static CMOS circuit families, right. And then the reason for this being called as a static is, in the steady state the current is actually zero. So, ideally the current should be zero, we will look into the leakage currents, later on where we will see that you know even though it is a static CMOS or even in a steady state there will be some current that has been leaking.

But apart from the leakage current, there is no actually current that will be flowing. If I draw the inverter here the V_{dd} here are connected. So, this is my inverter.

So, there is no direct current which will be flowing from V_{dd} to ground in a steady state. Of course, there will be some kind of a current which will be flowing to raise this output node from 0 to 5 volts or 5 to 0 volts and then from current flowing to the ground. But once it reaches the steady state value, after that there would not be any direct current from V_{dd} to ground. Thereby this particular zero current and that is why it is called as a static CMOS circuit families and that is one of the significant advantages of the CMOS. Static CMOS circuit families is the current dissipation from V_{dd} to ground is 0 and if the current is actually 0, current multiplied by V_{dd}. If the V_{dd} is nothing but the voltage the potential difference between this particular ground rail is also 0. So, the power dissipation is actually 0 in a steady state for a static CMOS circuit family. So, that is one of the significant advantages.

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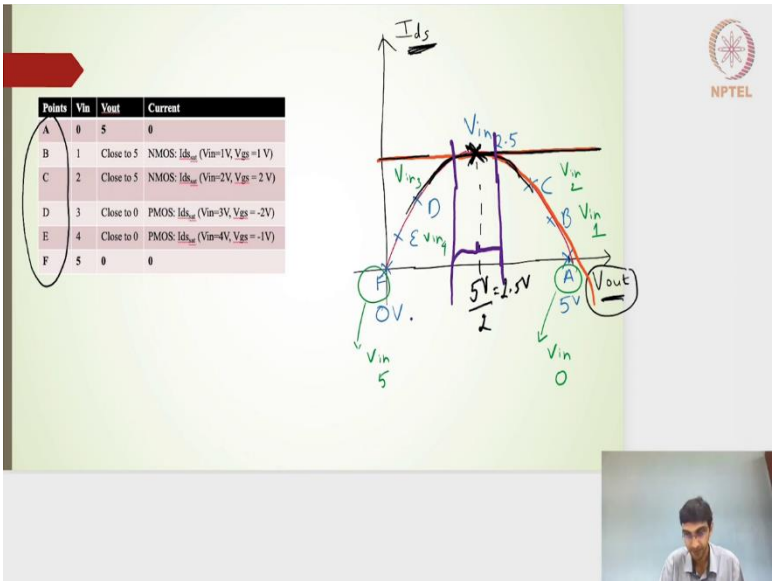

Moving ahead if I want to draw now, that we have this particular intersection points A B C, D, E, F and then it is the current value, it is input to voltage, is output voltage. Although we do not know the real output voltage graphically, we can only say, that it is close to 5 volts or close to 0 volts.

The current values, we know some particular or we can write an expression, but putting those points of A, B, C and then D, E, F and drawing the profile of V_{out} with respect to I_d.

So, it is basically capturing those particular values from the graphs, from this particular point where we had this intersection points. We should be able to draw the current here versus the output voltage.

So, I have taken out all other things, I have taken out the NMOS profile, current profile, PMOS current profile for different input voltages and only pick those points, A point, B point, C point, D point, E point and F point and I have drawn this particular and I have connected these points.

There is one additional input here, where I have drawn, I have taken a point of input of 2.5 volts. So, 2.5 volts actually lies between V_{dd} of 5 volts and ground rail of 0 volts and it becomes a very significant point here because at this particular point, intersects this particular solution of V_{in} of 2.5 volts. Now, if I want to find out what is the current, I need to actually equate the saturation current of the NMOS and then the PMOS.

So, graphically you can see that for 2.5 volts of input, the saturation profiles of the NMOS and PMOS are going to intersect. So, then if the saturation current intersect, I will get this particular point interestingly, if the betas are same, with the betas of PMOS and NMOS are same, which in our case we have taken to simplify these things. This will be nothing but 5V/2 so, nothing but 2.5 volts.

In fact, now for this particular point 2.5 volts, in fact I will get a series of points. So, the saturation profile of the NMOS, the saturation profile let me draw. So, this will be the PMOS the saturation profile of the you know let me draw the different one. So, saturation profile of this particular value is something like this.

So, I will get actually a series of points. So, I will use a blue ink for 2.5 volts of an input, I will actually get a series of points around this 2.5 volts. So, that is, if I am changing the input voltage from 0 volts to 1 volts to 2 volts to 2.5 volts to 3 volts and so on. I will get the series of saturation points or the transition region, where the output voltage goes from 5 volts to 0 volts.

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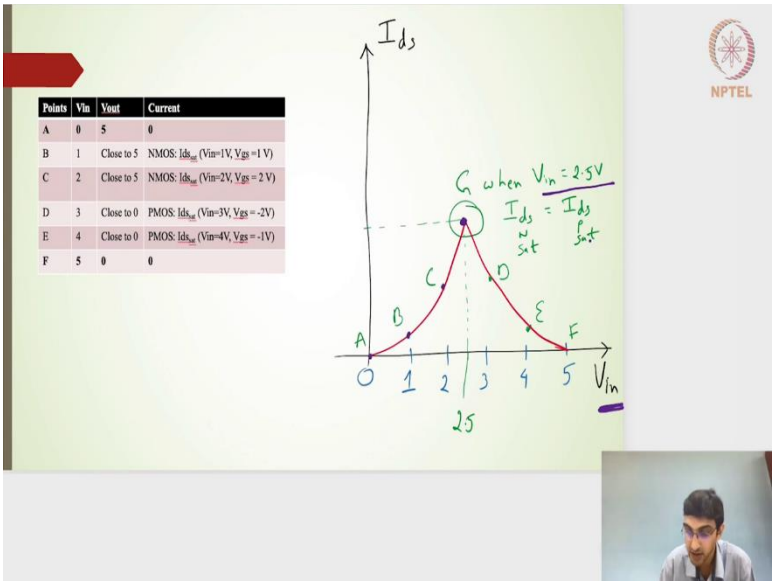

So, that is something we will see it now and then this is again another profile of I_{ds} with respect to input voltage. So, the earlier one was I_{ds} with respect to output voltage. So, I have drawn with respect to the input voltages those series of points A, B, C and then D, E, F and then this is one point G point, where the input is 2.5 volts and where I will have the NMOS and PMOS saturation current to be equated.

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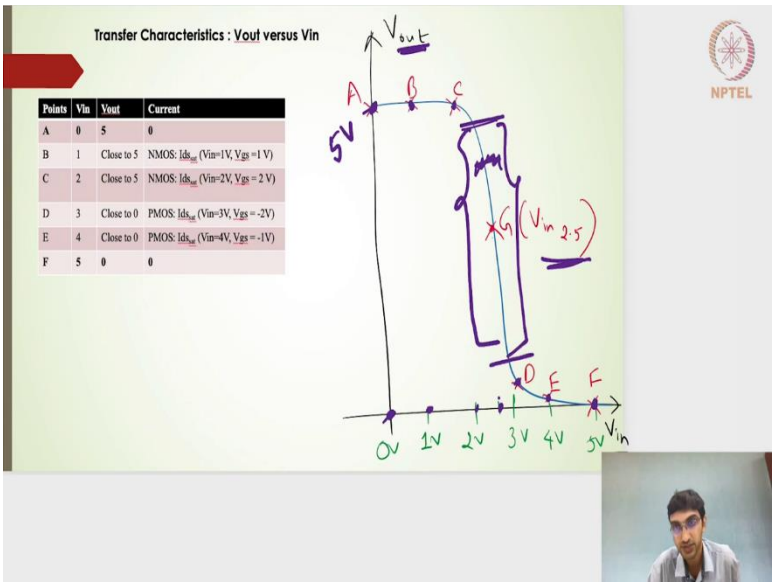

And then, this is the last one is the transfer characteristics, where we have the output voltage drawn with respect to the input voltage. So, I now have the points A, B, C, D, E,

F and then this particular G point. So, notice that the G point, I will actually get this particular, I should start from here so, G value. In fact, this turns out to be a straighter line. So, for an input of 2.5 volts, I will actually get a series of solution points around the G value.

The G value turns out to be close to the 2.5 volts. So, this transfer characteristics is one of the important characteristics for an inverter. We can always draw the transfer characteristics for a two input NAND gate or NOR gate or any number of inputs of the universal gates or any other combinational circuits. But this particular transfer characteristics states that, if I apply an input of 0 for an inverter, I will get the output of A here. If I apply an input of 1 volt, I will still get the output close to this one as 5 volts. So, close to 5 volts, if I apply an input of 2 volts, I will get the output close to 5 volts.

If I apply an input of 5 volts here the output is 0 volts, if I apply an input of 4 volts, I will get output close to 0 volts and if I apply an input of 3 volts, I will get an output close to 0 volts. So, this is how the transfer characteristics of the inverter looks like and it states the working of the inverter, it clearly represents the working of the inverter.