Digital Circuits and Systems Prof. Shankar Balachandran Department of Electrical Engineering Indian Institute of Technology, Bombay And Department of Computer Science and Engineering Indian Institute of Technology, Madras

Module – 53 Closing Remarks

Hi, we are at the very last module of this course. So, this module I am just going to have a few closing remarks and there is no technical content in this course in this module. So, this is just about the overall course and what my opinions and so on. So, before anything, I want to acknowledge a lot of people, who were part of this course in some form or the other, direct or indirect.

(Refer Slide Time: 00:39)



To Prof Dinesh Bhatia and Prof Poras Balsara from University of Texas at Dallas, I owe them thanks, because lots of the material that I used in the course are based on their lecture material. So, I have refined it over time, but the base is from their lecture material. I also want to thank my teaching assistants at IIT madras. So, they are either my... Either they are PhD students or Masters students, who are working in IIT madras. So, Praveen Alapati, Dennis Varkey, Swami Saranam, Biswabandan Panda, and Gnaneswara Jonna. So, they are my TA's; they took care of setting up the quizzes and checking the platform for errors and verilog assignments and what not. So, they have been a great help; and without them, I would not have been able to run the course.

(Refer Slide Time: 01:32)



Then, I want to thank the NPTEL team both at IIT Bombay and at IIT Madras. So, at IIT Bombay, which is where I recorded all the videos. So, there are quite a few people, who helped me recording this course to be able to bring it on time and bring it at the quality that is there. So, I want to thank the producer Mister Arun Kalwankar and Project Manager: Sangeeta Shrivatsava. So, they both were the coordinators for the NPTEL program itself. So, I have special thanks to the camera crew here and the editing crew here. So, I thank Tushar Deshpande and Amin Shaikh for the camera work and the editing work. And Vijay Kedare and Ravi Paswan and Vinay Raut for all the administrative help that I got from the NPTEL studio here.

So, without them, recording the videos for the past nine weeks or so could have been really hard; they did amazing camera work and editing work and what not. I am really grateful to them. At IIT Madras side, Project Officer: Bharathi Balaji, Project Associate: T. Senthil Kumar were quite handy; and they helped me through and through in setting up the course; and for various other logistic and administrative discussions, they have been quite handy. And they uploaded everything on YouTube and what not. So, I am very thankful to them. And Professor Andrew Thangaraj for coordinating the whole online course itself.

(Refer Slide Time: 02:57)



I also acknowledge a few other people, who brought the platform. And this platform – the course would not have not been possible unless we had a stable and scalable platform. So, I thank Abhinav Khandelwal and Ashwani Sharma from Google and whoever else who got involved in Google to provide us with this platform. So, I thank them. And I also thank Victor Lyuboslavsky; he is the owner of EDA platform. So, he let us use the platform for posting all the assignments and home works and so on. I am thankful to them. And finally, I am also thankful to the exam coordination team of Tata Consultancy Services; so it is a huge team that is going to get together to coordinate the exam. So, I am thankful to them too.

(Refer Slide Time: 03:55)



So, now, let us look at the course itself. In terms of a quick outline of the course, these are the several things that we did over the weeks. So, each bullet point actually corresponds to a week. In week 1, we looked at introduction, basic Boolean logic, basic Boolean theorems and minimization. In week 2, we looked at Karnaugh maps. Week 3 - we looked at combinational circuits including muxes, demuxes, encoders, decoders and what not. In week 4, we looked at sequential elements namely latches and flip-flops; we also looked at basic sequential circuits namely counters with reset and without reset and what not. In the fifth week, I introduced you to CMOS and I brought up why delays happen in circuits and how to measure them and how to characterize them; we also looked at the notion of state machines. In the sixth week, we looked at finite state machines, state machine synthesis, state minimization and state assignment. Week 7 - we did not have any slides; but I started with an algorithm and I designed a complete logic hardware for it and also wrote the whole code in verilog. Hopefully, that inspired you to take up a problem and divide that into circuit blocks and generate verilog for it.

In the eighth week, we looked at pipelining, parallelism and interleaving. This is a week in which we traded off size of the circuit or in terms of the number of the gates for delay of the circuits. So, we got better delay by spending more hardware. In the last week, which is this week, we looked at arithmetic circuits. So, we looked at number representation, adders, multipliers, comparators and so on. So, throughout these so many weeks, we have also been doing a lot of verilog modeling; and the verilog modeling – we started with assign statements, instantiations, basic primitives; we also looked at always blocks. We looked at blocking versus non-blocking statements. We looked at styles – appropriate styles for modeling different kinds of circuits. All of these we did in over nine weeks.

So, typically, packing so much content into nine weeks could have really hard thing to do; but this online platform and being able to write, take quizzes and so on probably helped you in understanding concepts better. And I also assume that, verilog – the way it was done was also helpful to you, because it was done in small pieces at a time; and primarily, I did not look at any simulation aspects of verilog specifically; instead, I taught you what is called synthesizable. If you look at the hardware verilog that is written, you should be able to imagine a circuit that is out of that. And that is exactly the way the tools also work. The tools take these things and generate circuits for you. So, it is better that you write synthesizable code and not write something like what you do in

software programming languages. So, I started at the very first week with the notion of handling complexity.

(Refer Slide Time: 06:50)

Design Level	System Design	Logic Design	Circuit Design	Layout Design
Graphical Representation				
Elements	Blocks, sub-blocks	Logic gates	FETs, R, C, etc.	Geometric structures

So, if you do VLSI courses, you will probably learn layout design and circuit design. That is not the level at which this course was dealt with. We did logic design namely designing with gates and equations directly. We also did some system level design. So, we were able to put components together and connect them together and make larger circuits out of that. So, I would say that, we operated at a level of abstraction, which is already fairly high compared to what you would do in VLSI circuits. So, if you want a complete package, you should try and take a course in VLSI later. So, either in your own college if there are online courses, you should try that; they will probably teach you how to do circuit design as well as layout design.

Of course, above system design, you can also do full-chip integration and so on. This is not something that I was able to do in the course; clearly, the course was meant for under grades at the second-year level. And I trust that even the material – all of that, that is, taught so far is already a bit of heavy duty material for a second-year student. Nevertheless, I assume that, you will be able to go back and look at the videos later; when you have a little more maturity about the field itself, you will be able to appreciate a lot of the concepts even if you did not appreciate it right away.

(Refer Slide Time: 08:03)



I also suggest that, you go and read up several other topics, which I did not cover here. Specifically, I did not talk anything about memory at all. RAMs and ROMs are also as part of a system as... In almost all the systems, you will have some amount of memory. So, I did not talk anything about memory at all in this course; I suggest that you go and read up. Full system design usually typically happens; once you have a basic digital logic course, you will be able to understand full systems. So, that is something that, you may have to take us a course later. In terms of circuit design itself, designing high speed arithmetic circuits and being able to do power and energy analysis is not something that I covered in detail at all. So, high speed arithmetic I still did a parallel adder; and the multiplier was parallel; I did not cover any of the other circuits like trigonometric operations and exponent, logarithm, power; there are circuits for each one of them; that is not something that I covered. Even high speed multipliers and high speed adders – I did not cover them in detail; I did not even touch up on dividers; these are other things that you may have to learn in more advance classes. Say if you are a graduate student, you will probably have courses, which covers some of these aspects.

Similarly, analyzing power and energy is very very important in current day circuits. So, mobile phones and various portable devices – they are all operating under batteries and they have severe energy constraints. So, understanding power and energy of a circuit is also very important; that is not something I did in this course. In terms of verilog, I did not talk about how to verify whether the verilog design that is given to you is correct or not. In fact, I did not event teach a lot about the test benches itself. So, you can go and

look up the test benches that I have used; and hopefully, by osmosis, you can learn some of these aspects. It is not the same as verifying a circuit; verification of a circuit is a lot more involved than being able to write just a test bench. That is not something that I am able to cover; however, usually, again there are graduate courses, which will cover verification as a full semester course. And I also did not assign large scale projects, because this course was broken up as lots of small home works and so on. So, I suggest that you take up problems even from text books or elsewhere and do verilog projects on your own. This is not something that I was able to do; but I think you should be able to pick up all the little bits of information and be able to create a project of your own and do it on your own. So, about the course itself, some summary I want to provide before I close the video.

(Refer Slide Time: 10:37)



So, there are about 10,000 odd students who registered for the course. So, it was a fairly large registration that was there; but soon I realized that, there are about only 1000 odd students who are really active. So, in the first few weeks, there were still about 4000-5000 students; and after that, when I say active, these are students, who were watching videos as well as submitting assignments and what not. So, in the seventh or eighth week, I still saw that, there are thousand students, who are submitting assignments and participating in the forums and so on. In terms of the population, a big section was actually students in the second and third year under graduate or probably some graduate students; there were also some faculty, people from industry and so on, who are also registered for the course. In fact, most of the students were from India; but there were

quite a significant number of students, who are taking it from outside India also. So, I am pleasantly surprised that, many many students from many many walks of life were able to derive something out of this course.

And, I am grateful to the students to have offered me an opportunity to teach a worldwide audience like this. So, there were lots of good responses in terms of assignments and quizzes; lots of you were able to turn in assignments sometimes with mild extensions and so on. But I am happy that, many of you are able to submit these assignments and quizzes. I would have liked a little more participation in the forums; it looked like the forum is mostly a one-way participation; either I was giving announcements or there was a one-on-one dialogue between a student and me. So, an online forum is typically meant for the whole class to participate. And even without disclosing home work answers and so on, you can actually participate in the very healthy and very lively manner; that is something that was missing in the course. But I am hopeful that, when you go to the other courses, you will be able to participate better and be more confident about participation. So, this is the summary of the course.

This brings me to the very last minute of this video of this course. So, I am quite glad that, I was able to do something like this for a worldwide audience; and a many many Indian students are sure to benefit from this. I know that, many of you are also taking the certification exam. I am thankful that, you stuck around till the very end of the course and are able to appreciate the contents from the course. If there were any mistakes in any of the lecture videos or anything, please feel free to contact me. Any mistake that I have done, I would like to correct it and have a correct set of videos and lectures slides available for any one for further use.

So, in the future, if you have any further request or comments about the course, please feel free to e-mail me; and I will be happy to oblige and take your suggestions. So, overall, a big thank you from all of us to all of you; and I wish you the very best for this course, the final exam as well as anything that you do in the future. So, I am hoping to return back later with more advance courses related to systems and VLSI and so on. So, I do not have a specific plan for that; but let us see how things work.

So, thank you so much and good bye and see you as good engineers in digital design. So, I hope that, companies and colleges, universities benefit from everything that you learnt in this course. Thank you.