Digital Circuits and Systems
Prof. Shankar Balachandran
Department of Electrical Engineering
Indian Institute of Technology, Bombay
And
Department of Computer Science and Engineering
Indian Institute of Technology, Madras

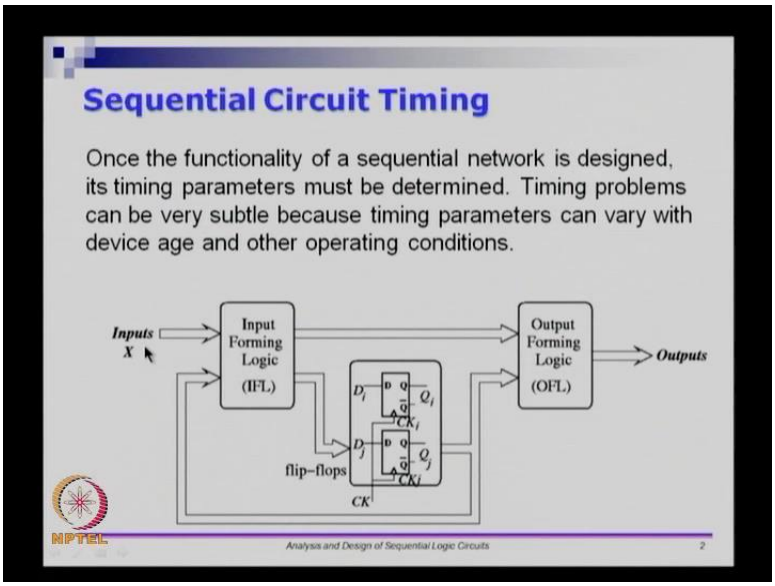
Module – 33
Timing Sequential Circuits

This module we are going to learn about a Timing Sequential Circuits. So, we talked about how we analysis combinational circuits and delay for combinational circuits. And in this class, we will look at the timing constrains required for sequential circuits. So, we look at two different components for sequential elements. For flip flops, we looked at the notion of what is called set up time and we looked at the notion of what is called hold time.

So, just to jog your memory, so set up time and hold time together form of window and this window is, for a flip flop it is around the clock pulse that is triggering in. So, if it is a positive edge trigger flip flop, around the positive edge trigger, you place a window. So, for some time before the clock edge arrives and once the clock edge arrives for some time, for this time window you cannot change your data. The data has to settle in, before the clock pulse comes at least TSU time units before that and it has to be held at the same value, at least for TH time units after it arrives.

So, we saw these two things, but as we saw in the previous week, we saw that the circuit, the sequential circuit is not just the sequential elements, it also has combinational logic around it. So, what we going to do is, we going to look at how we analyze for a sequential circuits, not just an element.

(Refer Slide Time: 01:46)



So, let us look at the basic sequential circuits, this is the same picture that I showed earlier. We have state registers and there is some input forming logic and output forming logic or the next state and output logic. The inputs come into the input forming logic, the inputs also go to the output forming logic and so on. Now, what we want is, we want timing relationships, so if I look at this whole thing as a black box, as a chip, there are inputs that I am providing, this may also include the clock and there are outputs that are coming out.

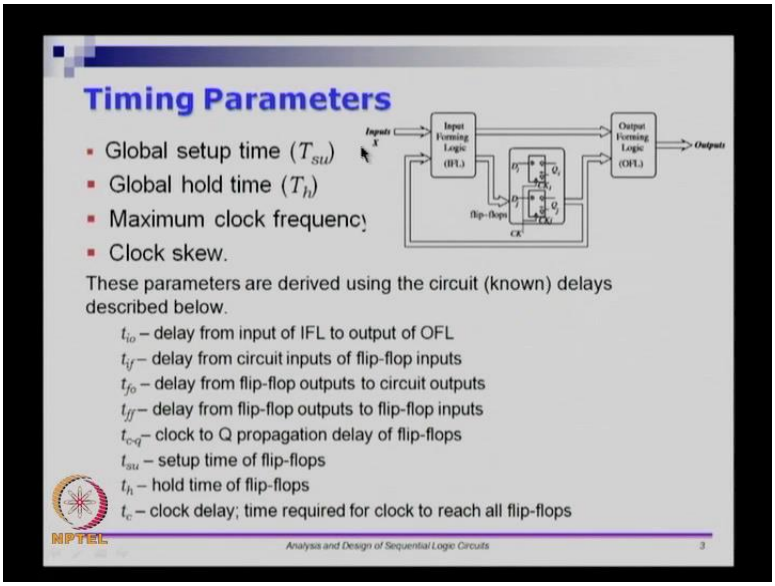
So, for instance these could be a check which have input on mother board and the clock input and the data inputs are coming from the external world and the output there is coming out of the chip is going into the external world. So, a signal that is placed on the chip input will take some finite amount of time to go inside, it has go to the input logic which is inside your chip, it has to go to the state registers.

So, it again inside a chip finally, the output that is coming out from your chip has to come out and travel through the bus that is in the printed circuit board or the mother board, and then go to another device. So, there are quite a few things that happen in a system. So, if we imagine this as a chip, then there are inputs and outputs that are external to it, we want to see at what rate you can supply the input.

So, we do not what input that I have given too fast, the circuit may not be able to process it at that rate, you also do not want the inputs should be too slow, because if I can process it at higher rate, why not. So, you want to be able to see, at what rate I can give the input

and at what rate, I can sustain the output. So, this is called sequential circuit timing analysis and we will look at timing problems that comes, because of various constraints. So, let us look at the basic parameters.

(Refer Slide Time: 03:42)



In terms of the whole chip, we first talk about what is called capital T subscript s u or the global set up time and we will also look at, what is called the global hold time. So, you are going to assume that, there is a clock pulse that is fed from the external world and with respect to that clock, there is some data that is coming from the external world. So, we will first argue that with respect to that clock pulse, we need to satisfy two timing parameters namely global set up time and global hold time.

We also want to look at, what is a logic frequency at which a chip can run. So, if I design a circuit, then I want to see, at what frequency it can run. So, high speed circuits are circuits that can run faster, so sometimes you want circuits that can run very fast and you want to be able to clock it at as much a high frequency as possible. So, if I making a processor, if I can change the design a little bit and if I can run it at 2 gigahertz, instead of let us say 1.5 gigahertz, then that is a nice thing to do.

So, we will see how to do all of that. There are various parameters or definitions that you need to know, but it is fairly straight forward. So, let us look at the subscript here in each of these parameters. So, wherever you see i that relates to inputs, which are given to the chip, wherever you see o, these are outputs from the chip. So, imagine a black box

around this, this is all inside a chip, but there is something coming from the external world, there is something going to the external world.

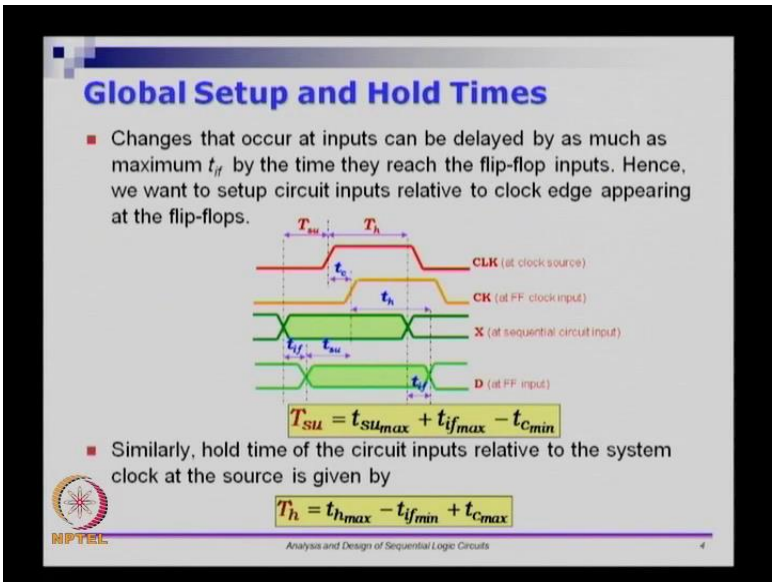
So, this i relates to input, o relates to output and f relates to flip flop. So, let us see these four parameters, i to o means the delay that it takes to go from the input. A change in input, it goes through the input forming logic, and then appears as input to the flip flop that is called, i to o is going through the inputs to the output logic to the output. I to f delay is from the inputs, going through the input forming logic, how long does it take to appear as input to the state register, that is called i to f.

So, the moment there is a change in the flip flops output, how long does it take to go to the output that is called f to o delay. So, the delay should account for output forming logics delay, and then there is flip flop to flip flop delay. If there is a change in output in the state register, how long does it take to go back through the input forming logic, took come back and appear as input to the state register. So, that is called flop to flop delay.

So, flop to flop delay... So, all these if you notice are all combinational delays, i o, i f and f o, f f are combinational delays. Then, there is c to q delay, this c to q delay is the clock to q delay of the flip flop that we are using. There is s u and h, which are also delays of the element. So, the moment you pick the flip flops that you are going to use in your circuit, t c to q and t s u and t h are the clock to q set up and hold time of the flip flops.

Finally, that could also be the something called t c or the clock delay, this is the time required to reach all the flip flops. So, there is a clock that is given as an external input to the chip and this goes through the bus on to the chip and at the chip, it is still has to travel within the chip to go and reach various flip flops and we will call that the t c or the clock delay. So, for now just remember that we are looking at parameters, these four parameters are combinational delays, and these three parameters are flip flop basic unit delays and this is something which is respect to the external world.

(Refer Slide Time: 07:26)



So, let us first look at the global set up and hold time, so the global set up time is as seen from the outside of the chip, when the clock pulse comes in, how long should the data be ready before the clock pulse comes in and how long should the data be ready, should be kept stable after the clock pulse comes in, this is called the global set up and hold time. So, let us see a signal called CLK, I am going to assume that the whole circuit is synchronized with respect to positive edge trigger of the flops.

So, let us assume that there is an external source called CLK and internally, it takes t c time units to appear at a flip flop. So, this could be because of the wire that connects from the input pin to the actual flip flops clock input. So, this t c could be 0, but let us assume that t c is some possible quantity right now, so we will call that signal as CK. So, CLK is from the external world, CK is as seen at the flip flops.

Now, you are bringing data from the external world, we will call that X. When this appears in the input of the flip flop, we will call that D. Now, any change in input in the external world is going to go through the input forming logic and appear as the inputs of the flip flop, that will take t i f time, so that is the input to flop delay. A change in input at the external world will go through the input forming logic and it will appear as D inputs, that is going to take i f time units.

So, some change in input here is taking t i f time units, then there is another change in input from here. So, if you notice, there is a change in input here, that is going to take some time unit t i f and so on. So, t i f is the time period between X and D, so we are

assuming that there is somebody watching all the events in the chip and we are drawing the wave form with respect to that observer. So, there is an observer who seeing all events with respect to the chip.

So, from the external world the data changes t at this time period, but it takes t i f time units to appear as the flip flop input and so on, so that is t i f. Then, our t s u and t h are actually specified with respect to the flip flop, remember. This small case t subscript s u and small case a t subscript h are actually with respect to the flip flop. So, let us go and look at that, with respect to CK not CLK with respect to CK, because that is your flip flop device.

So, with respect to the flip flop, there is some period of time before which the data has to be stable and some period of time, after the clock pulse arrives, it should be kept stable. So, t s u plus t h are a window around CK not CLK, now I want to know the relationship between in the external world. So, this is the external clock signal and how long should I keep the data stable with respect to the external clock signal, that is the global set up time and how long should I kept it stable after the external clock trigger with respect to the input data, that is called the hold time.

So, what we are looking for is, the mathematical relationship between capital T s u and the parameters here and capital T h and the parameters here. Can we derive t s u and t h in terms of various circuit parameters? This is what we are going to do in the class today. So, let us see this, let us look as T s u, so we are trying to measure the time between here, because this is where the external input is allowed to change. By this time, it should have settled down, you do not want it anywhere beyond that to the left side, so that is your T s u.

And we are trying to measure the time period between this vertical line here and this vertical line here, what is the allowed set up time. So, if we go and look at these parameters here, I am going to write an expression first. So, the capital T s u is T s u max plus t i f max minus t c min, so let us look at this. From this line here, I want to measure up to here, so t i f plus t s u minus t c brings me to this edge. So, that is t i f plus t s u that takes me to the clock pulse here, but if I subtract t c, it takes me to CLK.

So, T s u is t s u of the flip flop plus t i f, which is the input to flop delay minus t c, let us look at this maxs and mins. So, if there are multiple path from input to the flip flop, the largest of the input flop delay should be accounted for. If I have different kinds of flip

flops with different set up times, I should account for the largest set up time and if there are different flip flops, some flip flops may be closer to the external world and some flip flops may be far away from the external clock trigger.

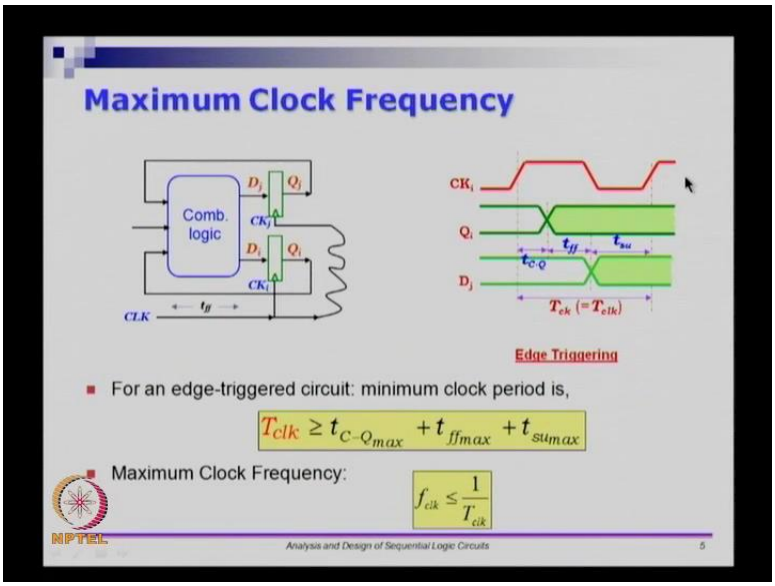
So, the smallest of that should be accounted for. If I have account for all of these, then t i f and t s u minus t c gives me the global set up time. Let us look at the global hold time, the global hold time, it starts from when the external CLK trigger comes and for some period of time you have to keep this green datas stable. You cannot switch the green data that is with the external world, x cannot change for some time period, we want to see how long it can be.

So, if we look at the picture here, T h is t c plus t h of the flip flop minus t i f. So, let us put it down, so capital T h is capital T c, this T c plus t h of the flip flop minus t i f. So, this is just written in a rearrange manner. So, t i h minus t i f plus t c, so it is the same expression written in a different form, now let us go and look at the max and mins here. So, I want to wait for the largest hold time among any of the flip flops and the largest clock to external CLK to CK delay for all the flip flops. So, that gives me t h max plus t c max.

And the reason why we have to wait for the smallest one is, if there is a change in the input, through the shortest path it can go to the D input and this may upset your flip flop, it may violate the hold time. So, with respect to T h the hold time constraint can be violated, because of the shortest path which will have the delay of t i f as minimum and with respect to the external world, the longest path or t i f max can actually violate the set up time.

So, T s u and T h, you can see the mathematical expressions, even if you do not have the max and mins, just get the expression right. It is t s u plus t i f minus t c and t h is t h plus t c minus t i f, these are the global setup time and hold times, these are with respect to the external world.

(Refer Slide Time: 15:14)



And if you want, so there are various parameters we talked about, we are worried about the global set up time, the global hold time and what is the frequency at which I can run the circuit. So, the frequency at which I can run the circuit, I should look at what happening within the chip, let us look at the chip inside. So, there is the CLK here, let us assume that there is no delay between CLK and CK, it is for now assume that t c is 0. CLK appears as CK i and CK j, let us assume that there is no delay between the CLK signal and CK signal as of now.

Then, let us assume that there are two flip flops Q i and Q j, Q i goes through the combinational logic and it means influence D j and Q j similarly may go through the combinational logic and implements D i, in fact Q i could influence D i and Q j could influence D j. So, there are four flop to flop path here Q j to D j, Q j to D i, Q i to D i and Q i to D j there are four flop to flop paths.

If I want to find out for edge triggered circuit, the smallest clock period, the smallest clock period is one in which it accommodates for all the delay that can happen in the circuit. So, what are the delays it can happen, when you go from one flop to another flop? So, as soon as the clock pulse comes in, the data could change, so that is t c to Q delay. So, let us say D i is stable for a while, let us assume that. So, you bring the clock pulse CK, as soon as I bring the clock pulse, this Q can change.

So, that is the clock to Q delay, then you go through the flip flops, that is the f f delay, and then you have to still account for the set up time of the flip flops here. So, if I go let

us say I am looking at the constraint from Q i to D j, if I want to look at it. So, this clock to Q delay of this flip flop plus the path through this combinational logic plus the set up time of this flip flop, if I add all of together.

Then, so any change in here will take at least, so much time to appear here, which means the clock width should be greater than that. So, that any if I place the current state here to get to the next state, I need to have at least, so much time accounted for. So, I have to delay the clock pulse by at least, so much time unit and that is why you have the greater than or equal to symbol here. So, t of the clock or the width of the clock should be greater than t c q max plus t f f max plus t s u max.

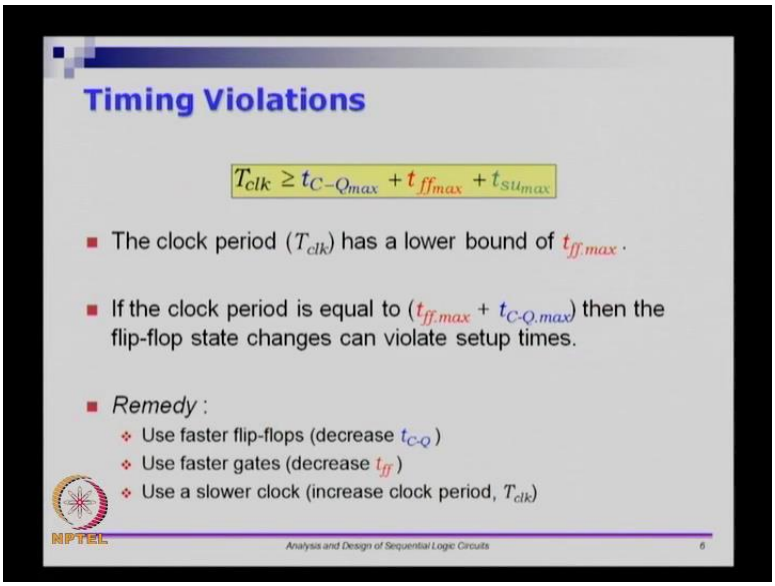
So, in fact t clock should be greater than C Q i plus t flip flop to flip flop. So, essentially i to Q i to D j delay plus t s u of this Q j flip flop, there will be four such constraints Q i to D j, D i to Q j, then Q i to D i itself, then Q j to D j itself there are four such things. Since, T c clock should be greater than each one of the four summations, then you can as well write it as max.

So, t c Q max plus t f f max plus t s u max, in each of the terms you pick the logic quantity, this is the most conservative clock that you can have. T clock is greater than the worst case, the clock to Q delay plus worst case flop to flop delay plus worst case set up time. You add all of that, your width of the clock must be greater than that, which means the clock frequency is upper bounded by 1 by T clock.

So, this is with respect to maximum clock frequency, here we assume that CLK appears immediately as CK i and CK j. So, the derivation you can see here, so CK i, t c Q, t f f and t s u. So, CK i is here, this is the... So, as soon as the clock comes, Q i could change the values after t c Q units, after some flop to flop delay, D j changes, but before the next clock pulse comes. So, this is the launching clock period and this is the landing clock.

So, as soon as this closes, use C to Q plus flip flop, so it will start appearing at D j now; however, you still have to satisfy the set up constraints of the landing flip flop. So, you go and push it till that, so t c Q plus t f f plus t s u that is how, why the clock pulse must be, so I hope this is clear.

(Refer Slide Time: 20:01)



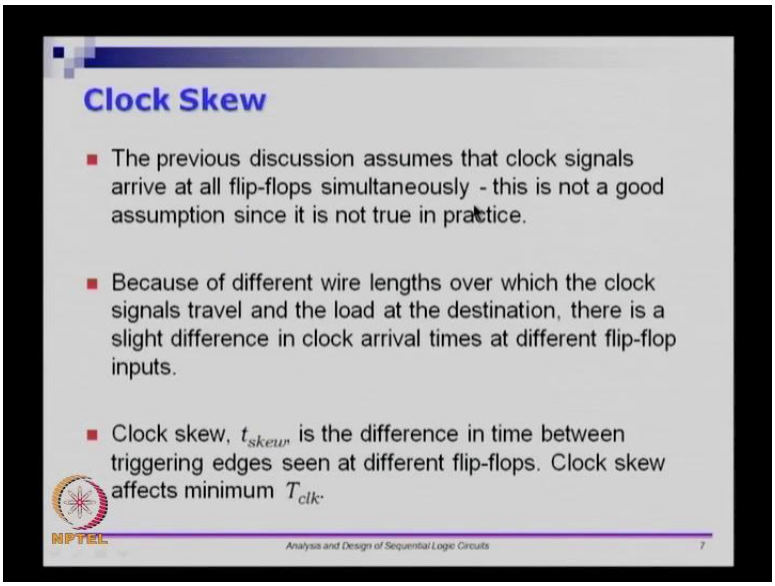
So, what could happen is, if you violate late that condition, T clock is greater than the summation of these, then we have what is called a set up time violation. So, if T clock... So, the first thing is T clock is bounded by t f f max, so your clock should be at least greater than; however, fancy a flip flop is, the flip flop only controls t c Q and t s u. So, instead of a d flip flop if I use a t flip flop or I get a better design for a d flip flop and so on it can only change C to Q and s u max, this f f max is the function of the combination logic that you used.

So, T clock is has a lower bound of t f f max it should be at least t f f max first up all, then if the clock period is equal to t f f max plus t C Q max. Let assume that T clock is not greater than equal to this sum with it is only just greater than C Q plus t f f, then what can happen is the flip flop is set to violate the set up time. So, if there is a set up time violation, then one way to look at it is... So, you want this summation to be this T clock to be greater than this summation.

However, you are not able to satisfy it, then I can bring down any of these quantities and make T clock is greater than equal to this. So, this is something that is under your control, but may some time you have a target I want to design a 2 gigahertz chip, in which case T clock will be 0.5 nanoseconds. So, if I want at chip at a set a target then have to go and redesign either the circuit or redesign the flip flops, so that the set up time are not violated.

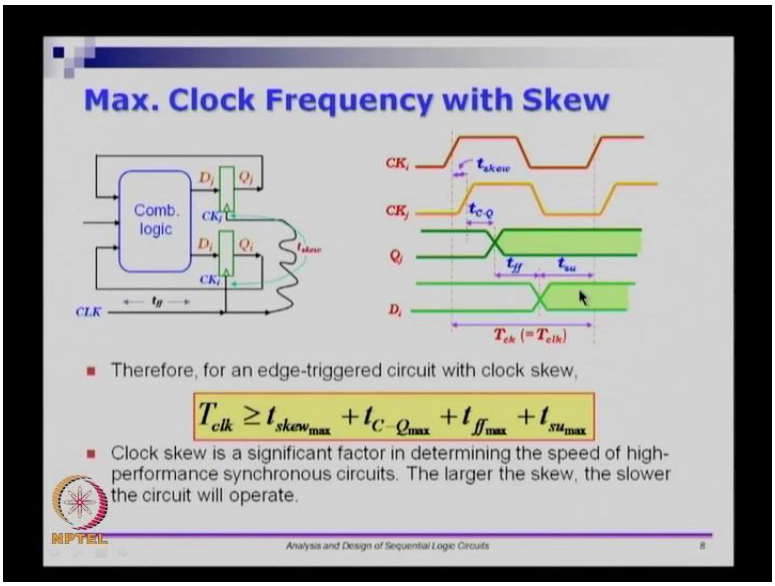
So, there is one is the analysis given the circuit you can tell me what is the largest clock with that you need, sometimes you given synthesis, you are as for as specific T clock you have to go and design in the circuit such a way that you never violate this condition. So, if you violate the setup time you have to go back and change either the flip flops are using or come up with the better circuit, so that the f f max goes down.

(Refer Slide Time: 22:10)



Then, there is this notion of what is called clocks Q, in the earlier case we assume that CLK which comes from the external world appears at CK i and CK j magically immediately. But, remember we are talking about electrical signals, the electrical signals also take some time to go from the outside of the chip to the clock pins of the flip flop, we called that t is Q. So, Q in English means change, so if there is a Q is that if some change. So, clock Q is the different in the time between the triggering edges seen at the different flip flops.

(Refer Slide Time: 22:47)



So, let us see this circuit here, so you have CLK and you have CK i and CK j what could happen is... So, imagine I am speaking, so or I am shooting LED light, so if I shoot from here the LED... So, if somebody at a closer distance will actually see the light earlier then somebody at the larger distance. So, forget the flag that the speed of the light is very high come back the human perception, but you can imagine that light arrives or even sound waves arrives at somebody whose closer, earlier than some body whose later.

So, the same thing happens here, if CLK pin from the external chip is closer to the flip flop i then CLK will be seen at i earlier than CK j. So, the same clock pulse between CK and CK j you may see that there is a difference that was be called as Q. So, let see the waveform first will come to the equation next. So, you have CK i which is the clock as seen by the flip flop i and CK j could have what is called a positives Q or negatives Q with respect to j.

So, CK i is here CK j may be some T skew time units away, because the flip flops is away from the CLK pin, it could be the CK j is actually seen the clock later. Now, if I want to look at the relationship between CK i and CK j let us look at the timing relationship. So, we are looking at the delay from flip flop Q j to flip flop i, so we are looking at this path starting from Q j what happens, if you have to go to i.

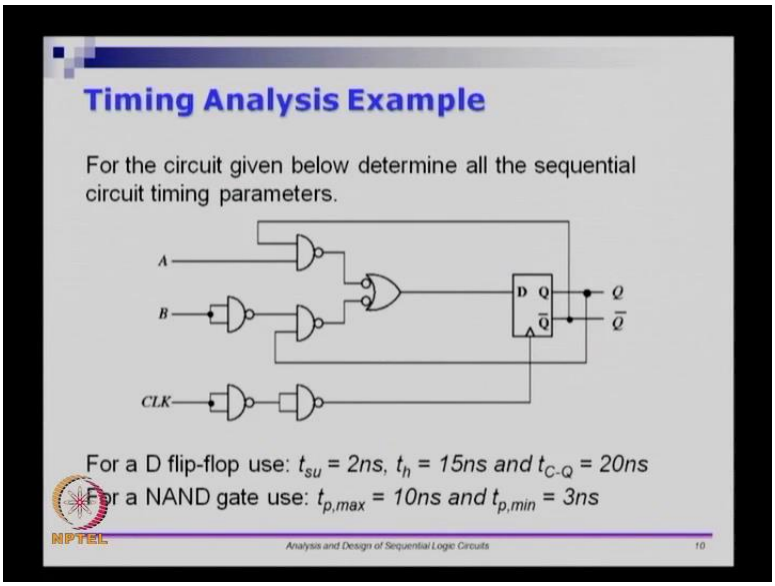
So, the moment CK j comes through then you have clock to Q delay of the Q j flip flop you have to account for that then you take t f f time units through this combinational logic, then D i gets ready and you have to get the D i ready for at least setup time unit

before the CK i comes. So, this the launch edge of the data and this the landing edge, so your clock pulse should take care of the fact that this t is Q plus t c Q plus t f f plus t s u.

So, the launching flip flop is CK j, the landing flip flop is i and the launching flip flop is actually seen with clock late which means it has lesser time to get the hold data ready. So, that the landing one can actually see it at the right time without any violation, so that is what you have here T clk is greater than to t c is t is Q max plus C Q max plus f f max plus s u max all of them are considering the largest value.

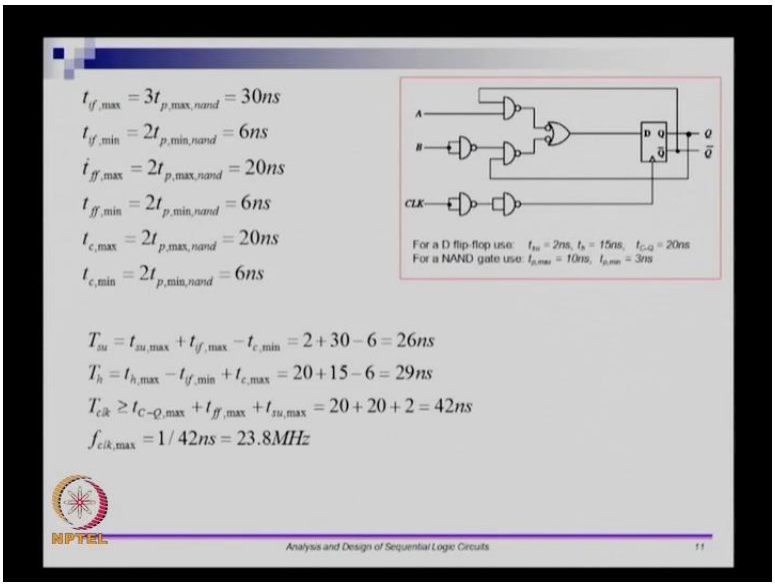
So, if CK i comes lightly to the left which means CK j is not too much delay come back to CK i then you have a little more breathing space. In fact, if it comes at the same time as CK i then t Q is 0 you get a little more breathing space, if it comes before CK i then that is actually good, because then you have a lot more space. So, if the direction of the difference in clock and if the direction which the data is going, so CK i is earlier than CK j, but CK j is providing something to D j, as a CK j is providing something to D i. So, the data is going in the opposite direction of the clock, so that is a tighter constraint, if it goes in the same direction then it becomes slightly easier, so this is called Q.

(Refer Slide Time: 26:46)



Let us do a small example, so we have a circuit it is not worry about what the circuit does there are two external inputs A and B and this an external input called clock and we are looking at what is the time at which the we want to do the timing analysis of this circuit, we want to look at various timing parameters like t s u, t h what is a frequency at which we can run and so on.

(Refer Slide Time: 27:11)



So, the same circuit is given here, let us do analysis of this, any change in CLK is going to take some time period to appear as CK. And that happens to be 2 NAND gates in the path, the NAND gates use we save that t p max is 10 nanoseconds and t p minimum is 3 nanoseconds, which means the largest delay is 10 nanoseconds in the smallest propagation delay is 3 nanoseconds. So, t c minimum is 2 times t p minimum of the NAND gate, so 2 times 3 is 6 nanoseconds and t c max is 2 times t p max of the NAND gate that is 2 time 10 which is 20 nanoseconds, so these two parameters at the easiest to drive.

Now, let us and go look at i f max, i f min, f f max and f f min, so if you look at i f max, i f max is from the input what is the largest time it takes to go to the d flip flop. So, clearly there is the path from A through here to go here and this a path from B through 3 gates to go to D. So, if I assume that this smallest delay here and the smallest delay here are added of up, then that is the smallest i f, so i f minimum is 1 NAND gate here and 1 NAND gate. So, this two OR with two not inputs is equivalent to NOR gate and NAND gate.

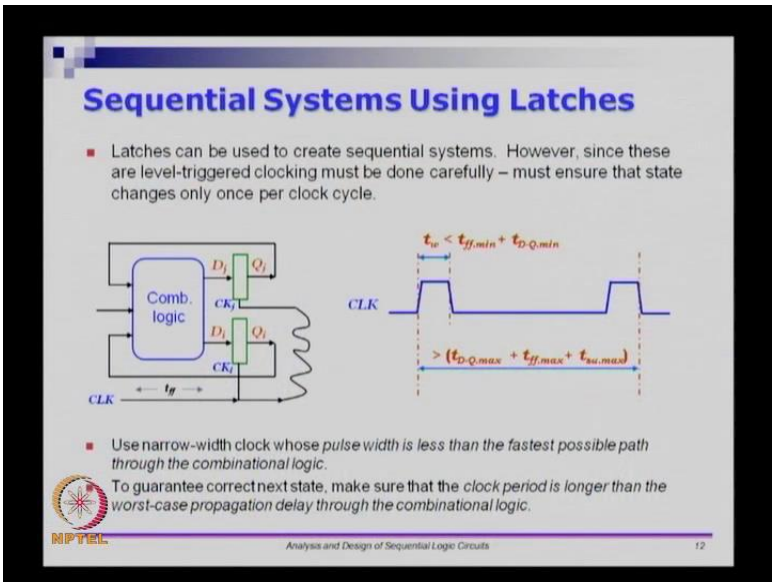
So, 1 NAND gate delay plus 1 NAND gate delay is a smallest path, so that is 2 times t p min of NAND. So, you look at smallest propagation delay of NAND that is 3, so 2 times 3 is 6, the longest time it will take is if there is change in B, it has to go through 3 NAND gates first of all and the NAND gates it could be exercise in the worst case path, the largest propagation delay of the NAND gates.

So, you take the largest of the delay that is 3 times 10 which is 30 nanoseconds, so t i f of max is 30 and t i f minimum is 6. Let us look at flop to flop delay, a changing Q bar it can go through 2 NAND gates and appear as D or change in Q could go through 2 NAND gates and appear it D. So, if either one change is it will take at least 2 NAND gates to go there. So, f f minimum you take the minimums, so that is 6 nanoseconds and f f maximum you take the maximum of the NAND gate that is 20 nanoseconds.

So, this takes care of all the paths i to f, f to f both minimum and maximum. So, if you look at the global set up time, global set up time is t s u max plus t i f max minus t c min, this is a summation 2 plus 30 minus 6 is 26 nanoseconds. The global hold time is t h max minus t i f min plus t c max, these are all just equations that I derived earlier that is 29 nanoseconds T clk is t C Q max plus t f f max plus t s u max plus actually there is a t C Q max, but we are looking at the clock pulse, the launching edge is on flip flop Q, the landing edge is also the flip flop Q there is no Q there, so Q is 0. So, this q is 0 here add all of that up that is 42 nanoseconds.

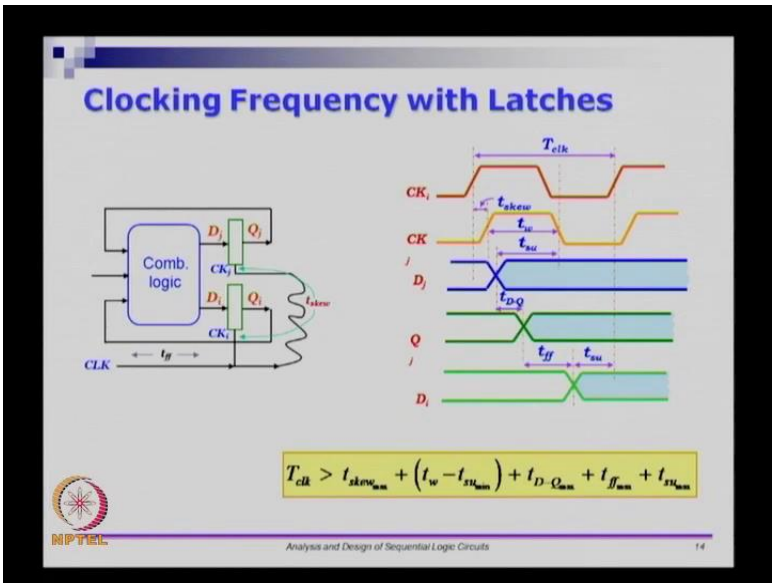
So, what this essentially says is your clock frequency cannot be more than 23.8 megahertz and when the clock pulse comes in the external world at least 26 nanoseconds before and at least 29 nanoseconds after. So, roughly for about 55 nanoseconds you have to keep that data stable at A and B, A and B should be stable for 55 nanoseconds, 26 nanoseconds before the CLK comes in and 29 nanoseconds after the CLK comes in you have to keep it ready, which means for 55 nanoseconds you have to keep your external inputs stable. So, if there is some other circuits that is going to drive A and B you should ensure that that is keeping the data stable for at least 55 nanoseconds and 26 before and 29 after. So, this is for sequential circuit with actual clock delay also.

(Refer Slide Time: 31:43)



So, you can also do the same thing with latches, so I am go to leave you the equations here and I want to go and thing about why these equations are correct. So, we are looking at width of the clock pulse, the argument is that the clock pulse should be at least so much wide and at most so much wide. So, this one says t w is at most so much it has to be it cannot be greater than t f f min plus t D Q min, this one says it should be at least so much t D Q max plus t f f max plus t s u max, this is about width of the clock. So, I would like to do go and argue that this is actually true. So, go and thing about why this should be true.

(Refer Slide Time: 32:29)



What I want to show is the clocking frequency with latches, so let us look at the circuit here, here these are not flip flops these are latches and we have a circuit like before except that these two are latches. So, I want to know drive the relationship for clock frequency of latches. So, we have various signals here, we are CK i, CK j, D j to Q j, so and D i. So, we have several data inputs, so D j, Q j, D i and so on I want to look at the relationship between various parameters.

So, if I want to look at what is the width of the clock that is the rate at which we can do at the inputs. So, width of the clock is the largest Q that you can have plus t w minus t s u plus t D to Q plus t f f plus t s u. So, let us just look at all the parameters and then will go minimum and maximums. So, from CK i to CK j there is t C Q plus t w width minus t s u plus D Q plus t f f plus t s u. So, you will see all the parameters appearing here.

So, T clock the width of the clock pulse, the argument is it should be greater than this expression here with the appropriate maxes and mins, even let say there are no maxes and mins, they are all just the same value. So, let us go and seen why something like this must be true, so we are looking at D i input with respect to Q j, but we cannot do with respect to just Q j, because it not just the Q j is changing D i, if the clock is on if D j change as Q j can change and Q j change as D i will again change we want to ensure that this chain of events D j to Q j to D i we want to control all of that that is why we a done with this way.

So, any change in D j may actually go back to change D i with in the same clock pulse and in fact a change in D i could go through Q i and go back and change D j also, in the worst case, several of these events can happen before the clock this latch closes. So, what this relationship is capturing is from the opening edge of the latch till the close edge of the latch, what is the relationship. So, if there is a change here, this is still in the level of CK i.

So, if we look at CK j it still in the level of CK j, if you look at Q here that is the delay through the latch of j and D i is happening here, if D i moves somewhere here it is possible that CK i is on and it may actually go and change D i could change Q i. So, this expression takes care of the fact that none of those untoward events happen, we want to keep the data inputs table for one full cycle, we do not want intermediate changes.

So, this expression T clock tells me that we have to keep for a latch, we have to be more careful there are lot more parameters involve and your T clock should be greater than to

this expression here. So, I also suggest that just like we what we did earlier, we go and argue why the maxs and mins are here and also convince we are self that the expression is correct. So, this brings to the end of module 33 and in this module we look at timing analyze of both latches and flip flops.

So, the most important thing for the latches and flip flop is what is a frequency at which you can run and for flip flops is that of set of valuation, sometimes we are also interested in hold valuations, for latches again setup at the hold violations. So, the latches are less frequently used done flip flops, so I suggest that you understand the flip flop material lot more thoroughly. And once you are more comfortable with flip flops, we can go and look at the material for hold for latches, latches are used in very specific sonorous it is not use all the time.

So, even if you do not understand latches for now get I thorough understanding of flip flops and may be later when we do a VLSI class or when go in do a masters you may have to understand the things behind latches also. So, that is bring me to the end of lectures of this week, the thing that is left out is some Verilog lecture for this week. So, we will do that in module 34, and till that bye, bye; I will see you in the next module.