Digital Circuits and Systems
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Module - 25
Delays (Contd)

Hi, welcome to twenty fifth modules for the course. And this is the third module in this week. So, in the last module I talked about combinational circuits, and combinational logic blocks and how to calculate delays of circuits, given the delays of gates. So, it is fairly complicated. And there are several tools which actually give you help.

So, it is not something that is done manually. Tools actually do all these things for you in the real world. However, it is good do know that there is some basic notion of the delay coming from the electrical proprieties of the devices that we have; because of that the gates have delay. And once you have delays of gates, calculating the delay of the combinations circuit is still quite involved because we have to look at not only the delays of the case, but also to what they are connected to. So, in the real world there are tools, which actually do all these calculations for you. In this video, what I want to talk about is what is the scenario when we look at sequential elements.

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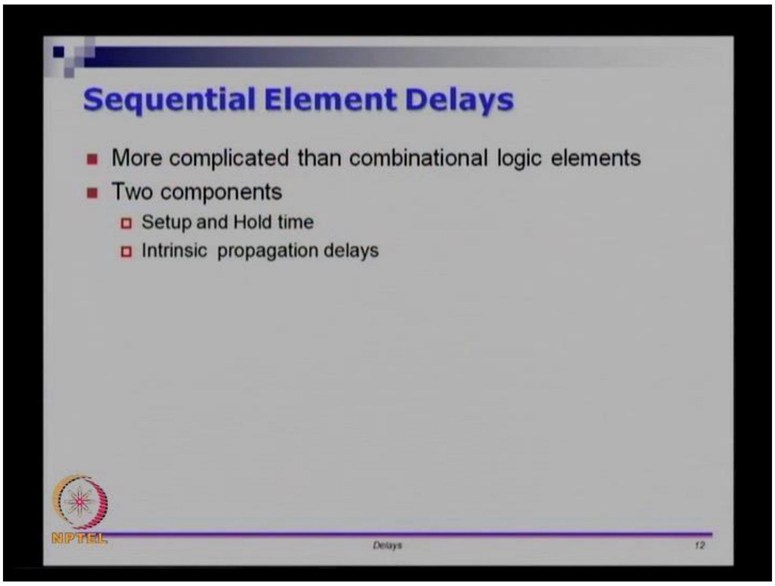

Sequential Element Delays

- More complicated than combinational logic elements
- Two components
  - Setup and Hold time
  - Intrinsic propagation delays

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So, there are two kinds. So, sequential components of delays. the delays in the sequential elements are more complicated than the combinational logic elements. So, in combinational logic elements we looked at inputs and we saw the outputs and we looked at tplh, tphl and so on. And when we took the combinational gates and put them in to the circuits, it got quite complicated. So, that is just the combinational part.

The sequential part adds to this complexity. There are two components of sequential elements. We will first look at the delays in sequential elements, then we will go back to and design some sequential circuits. In later week, we will actually see how to analyse the delay of sequential circuits itself.

So, let us start with sequential elements. There are two kinds of delays for sequential elements. The first kind of the delay is actually the intrinsic propagation delay itself; because your basic circuit, even a sequential element still has gates inside; because of that there is a intrinsic propagation delay. But, there is something new which is there for sequential elements. They are called the set up and hold time. These are three different components of delays in a sequential element. The first two components are the set up and hold time and the third component is intrinsic delay in the gate itself.

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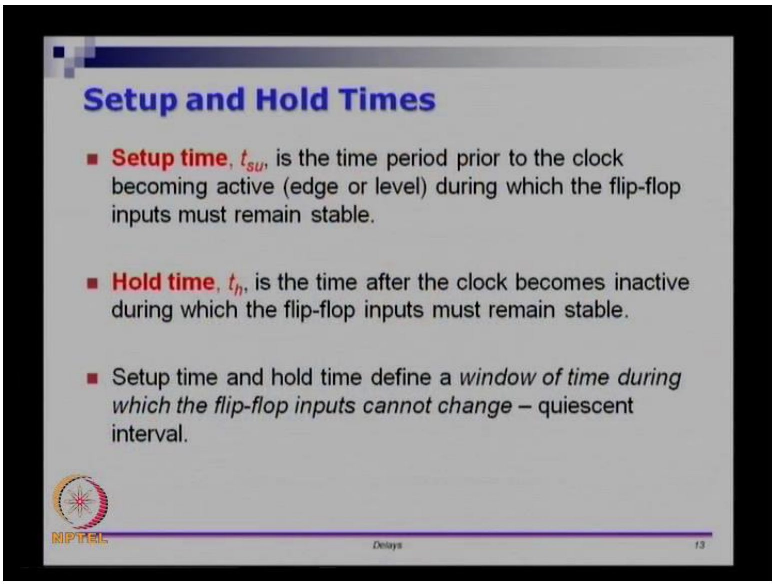

Setup and Hold Times

- **Setup time**, t_{su}, is the time period prior to the clock becoming active (edge or level) during which the flip-flop inputs must remain stable.
- **Hold time**, t_h, is the time after the clock becomes inactive during which the flip-flop inputs must remain stable.
- Setup time and hold time define a *window of time during which the flip-flop inputs cannot change* – quiescent interval.

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So, let us see what the definitions are. Set up time usually refer to as t subscript su; is the time period prior to the clock. Remember, we are talking about sequential elements here. So, there is always the notion of clock when we talk about sequential elements. So, t s u is the time period before the clock becoming active, during which the inputs to a flip flop must remain stable. So, we are talking about a flip flop. It has a clock and it has a data input. And you want to keep the data input stable for some amount of time before the clock comes in. and, this is called the set up time.

And the hold time is the time after the clock arrives. So, once the clock comes in, till what period? So, you have to still hold the input steady for some time period. And during this time period there should not be any activity in the input of a flip flop. So, this time period is called the hold time.

The setup time and hold time together define what is called a window of time, during which the flip flop inputs should remain stable, so that the flip flop can sample the input correctly. So, remember flip flops or when the clock edge arrives, let us say that the raising edge arrives, it has to sample the input. You do not want the input to be changing during this time. So, there is a window around the clock's arrival, during which you want the things to be quite. So, let us see a pictorial representation of that in a little while. There is also this inherent propagation delay. So, this is the intrinsic delay for a circuit.

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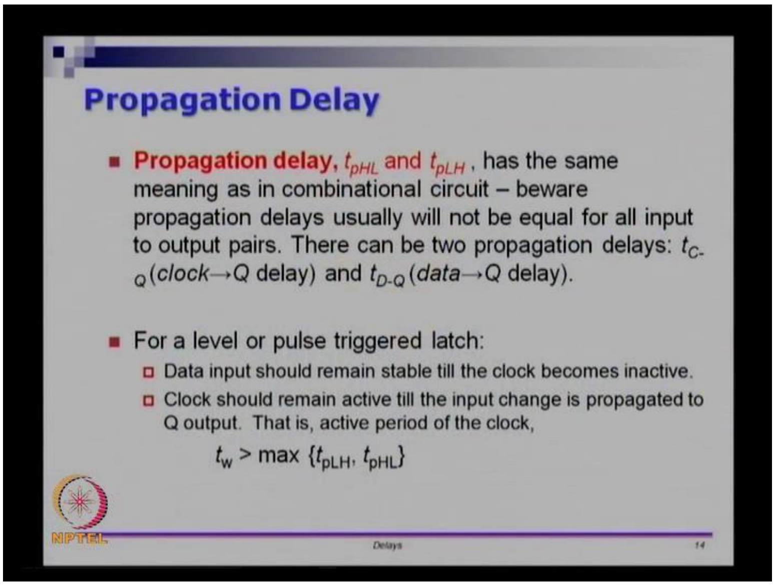

Propagation Delay

- **Propagation delay, t_{pHL} and t_{pLH}**, has the same meaning as in combinational circuit – beware propagation delays usually will not be equal for all input to output pairs. There can be two propagation delays: $t_{C\text{-}Q}$ (*clock*→Q delay) and $t_{D\text{-}Q}$ (*data*→Q delay).
- For a level or pulse triggered latch:
  - Data input should remain stable till the clock becomes inactive.
  - Clock should remain active till the input change is propagated to Q output. That is, active period of the clock,

$$t_w > \max\{t_{pLH}, t_{pHL}\}$$

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So, the propagation delay has the same meaning as we had in a combinational circuit. Only that there are different kinds of parts, because of which there are different kinds of delays. So, we will get to this in a little while.

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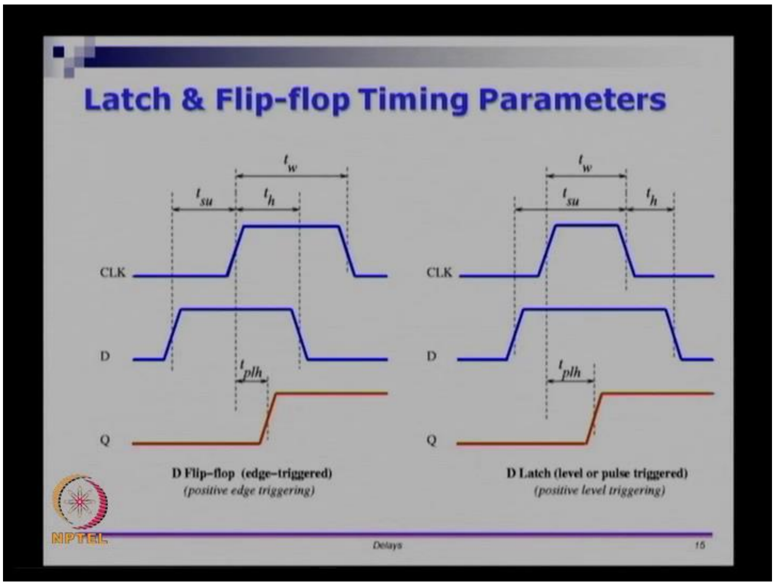

Latch & Flip-flop Timing Parameters

t_w
t_{su}
t_h
t_w
t_{su}
t_h
CLK
D
Q
t_{plh}
CLK
D
Q
t_{plh}
D Flip-flop (edge-triggered)
(positive edge triggering)
D Latch (level or pulse triggered)
(positive level triggering)
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So, to understand the timing parameters for latches and flip flops, so I want to give some small definition. So, let us look at flip flop first. For a flip flop, let us say it is positive edge triggered. So, there is a window of time in which the flip flop is actually letting you sample. So, this window of time is just the raising edge of the clock. So, you are going to sample the input only at the raising edge of the clock. And no matter what happens to the inputs at any other point of time. It does not matter to a flip flop.

So, if you want input to be correctly sampled, there is a window in which you are opening it. There is a time period at which the input is supposed to be there, which you can sample. So, with respect to that I want to define something called an opening edge and a closing edge.

So, the opening edge for a flip flop is when the clock comes in. Opening transition is when the clock goes on; right, when the clock goes up, already the input must be available. And once the clock becomes one, again the change in input is not something that is going to be captured. So, the opening and the closing edge of a flip flop is actually the raising edge of the flip flop itself. You go and look at that edge. It opens the window or it opens the flip flop for the output to copy from the input. But, it also closes; once the raising edge is gone, then changes in the inputs are not going to translate to changes in the output. Right. So, this is the notion for a opening and closing edges.

Similarly, for a latch the opening edge; so if I have a positive level triggered latch, in this case a D latch, then the opening edge is as soon as open the; as soon as the clock edge goes to one, the latches actually open, which means, it is can start copying the values from the input to the output. However, there is a closing edge beyond which any change in input will not result in change in the output.

So, for a flip flop the opening edge and the closing edge are both just one edge itself. So, there is a very narrow time. Between the opening and closing edge, there is hardly any; actually, these are the same edges. And in this case it is the positive edge for this flip flop, where as in the latch the opening edge and the closing edge are actually separated by a distance. So, if it is a positive level trigger latch, then the time period at which the clock remains one or the enable remains one; that separates the opening edge and the closing edge. So, this opening and closing edge could be either positive edge trigger in the input or negative edge trigger. That is, it does not mean that the opening edge is always zero to one and closing edge is always 1 to 0. So, for a positive edge triggered flip flop, it is so. The opening and closing edges are both zero to one transitions on the clock. And for a positive level triggered latch, the opening edge is zero to one transition and closing edge is one to 0 transition. So, given that in mind let us see how various parameters are defined.

So, the setup time is defined as the time period. So, you start from the closing edge for the device and you go backwards and you go and look at how long should I keep the input constant, so that the output remains stable. So, that is called the setup time. You go from the closing edge and you go backwards and you see how long you should keep the inputs constant. So, the closing edge for a positive edge triggered D flip flop is the raising edge itself.

So, remember there is a difference between open and closing verses raising and falling. So, I am talking about closing edge. So, the closing edge for a D flip flop of positive edge trigger is the positive edge itself; the raising edge itself. I go from there backwards and go and look at how long should I keep the input stable, so that the output is stable. So, this is called the setup time.

The hold time is the time period from the closing edge to the; so it is a small window from the closing edge of the flip flop. Beyond small period, for which you have to keep the output constant. So you start from the closing edge, which is the again the rising edge here and you go and see how long the output should be held constant. And that is this time period. That is called t h.

So, t h is measured from the closing edge of the flip flop to when the data should be kept constant. And similarly from the closing edge, backwards in time. If we go and look at it as a window, the setup time plus hold time, they both are defined with respect to the closing edge. So, t s u plus t h is one continuous window, for which the input should remain constant. So, if you keep the input constant bit for t s u plus t h time units, t s u separately and t h separately. But for overall, window of t s u plus t h time units. Then, a change in input will be captured as change in the output. So, you can see that change in the input from zero to one. It happens before t s u and it was held constant up to t h units after the clock edge arrived. So because of this, the output actually transitions from zero to one. And the definition of t p l h or the low to high transition is with respect to the opening edge of the flip flop. When does the flip flop open? It is also opening at the raising edge itself. So, you take the raising edge of the flip flop, which is also the opening edge. And look at when Q transition from 0 to 1. The difference between that is called t p l h.

Now, let us go and look at the equivalent definitions and see what it is there for latches. You go and look at the closing edge of the latch; which is for this positive level triggered latch, the closing edge is the falling edge. So, from the falling edge for some time period before that you have to keep the input constant.

So, t s u is a time period before the closing edge for which it has to be kept constant. And t hold is, after the closing edge it has to be kept constant. So, again t s u plus t h is actually a window of time in which you have to keep the input constant. However, t p l h is measured from the opening edge of the latch. The opening edge is actually the raising edge. So, from the raising edge you go and measure how much time it takes for the Q to react. And that is t p l h. And t w in both these cases is the time period for which the clock is kept on. So, t w here is the on time for this clock and t w here is on time for this clock here.

So, in summary what we have is the opening and closing edges or could be two different edges. For a flip flop it is actually one in the same edge; for a latch, it is usually two different edges. And depending on whether it positive or negative edge triggered flip flop, the opening and closing edges could both be either the raising edge or both be the falling edge. And depending on whether you have a positive level triggered latch or the negative level trigger latch, you could have opening and closing which are different edges.

And in all these cases setup time is always defined with respect to the closing edge and hold time is also defined with respect to the closing edge, whereas the propagation delay is measured with respect to the opening edge. So, these are various parameters.

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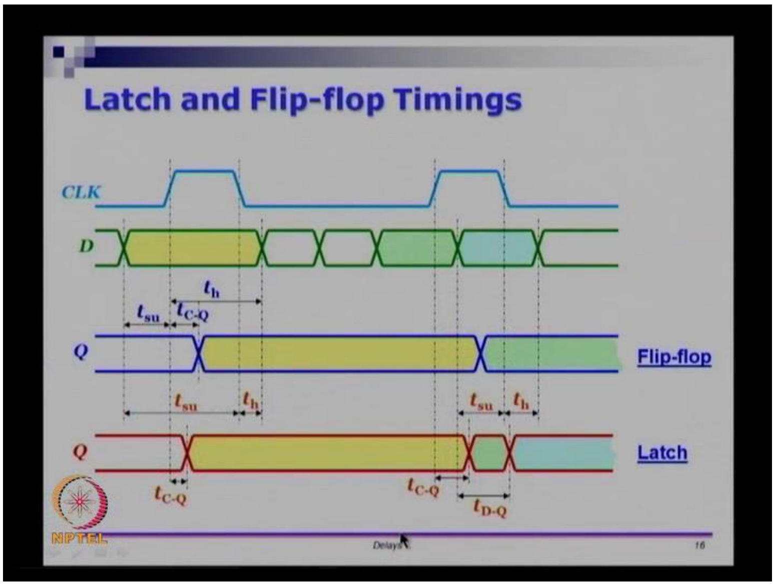

Latch and Flip-flop Timings

So, this picture actually shows the same thing in a little more detail. It not only shows propagation delay in different forms, it also shows various values. Let us assume that there is a clock which is periodic in nature. The on time seems to be much lesser than the off time. And let us see some data inputs that is changing. So, what is shown here is we do not worry about what the actual value is... Let us assume that there is data input that is changing. And every time you see a cross is changing from 1 to 0 or from 0 to 1. So, let us not worry about what the actual values are. Let us see what will happen if it is a flip flop verses what will happen if it is a latch.

So, if I go and think about what should happen here, this is a positive edge triggered flip flop and a positive level triggered latch. So, for a positive edge triggered flip flop, at this edge the value is yellow; which means I should get a yellow value. And at this edge the value is green. So, I should get green. These are the two values that should be projected from the circuit. It should be yellow and green and nothing in between. So, you should not be able to see the blue value, the white values and so on. Even though I am giving colours to them, I am calling them by names of the colours, so it could be anything.

So if this is 0, this could be one and there is some other change and so on. It could have happened. So, what I want is whatever value was at this raising edge and whatever value was at this raising edge, so you can see the wave form for Q is clean. There was a yellow value that got sampled. It was kept constant for some amount of time, till the next clock edge arrives. And when the clock edge arrives, it is sampling the green value. And that is what you have here.

Now, let us look at all the set up time, hold time and so on. So with respect to this edge, the data was kept constant for this amount of time. So, it is the requirement from the flip flop. You have to keep it for so much time; that is the set up time. And once the clock edge arrives, you have to keep it for so much time later. So, that is the hold time. So, set up time is time before the edge arrive and time after the edge arrives. And the propagation delay is from the opening edge of the flip flop, till the change is seen in q. So, the opening edge of the flip flop is also the raising edge, but Q changes only here. So, this is the propagation delay. It is also called the t C to Q delay of the clock to Q delay. So, clock to Q is the propagation delay.

If you go and look at latch, this setup time is measured from; again, we have the closing edge which is coming here. With respect to here, you see how long should the input be kept constant. That is called the setup time. Once the closing edge comes, how long it should be kept constant; that is the hold time. And the set up plus hold time is continuous window of time in which the input should be kept constant. So, it is kept constant during that time. And after the pulse has arrived, so if you go and look at the t C to Q delay, the opening edge of the latch is this raising edge and Q is changing here. So, t C to Q is this. Now, the latch actually got closed at this edge. So the transitions, the two white transitions, will not be seen.

Now, let us look at the blue edge. This second blue edge is the raising edge. When this came in, you have the green value here. So, this green value will come after t C to Q delay. You saw that. This is the clock, after t C to Q the green value gets reflected here. However, what is happening is the clock is still on, the latches not closed. The latches still on and the data input change. When the data input changes, then you can go and measure the time difference between when the data input was observed; when the change in the data input was observed, till when the corresponding output changes. In this case what happens is you see part of the blue and part of the green in the output wave form here.

So, the difference between clock to Q is the data was kept constant, clock changed; that is, C to Q delay. And now the clock is remaining stable at one, the latches enabled; you are changing q. At this point, it does not make sense to go and measure clock to q. Now, you should measure D to Q, because data is changing the latches; latch enable is kept constant. You measure D to Q. So, this is another factor that is necessary for a latch. So, for a latch there are two kinds of the propagation delays; the clock to Q delay and the D to Q delay. For a flip flop, there is no D to Q delay because D should be kept constant with respect to the clock edge anyway.

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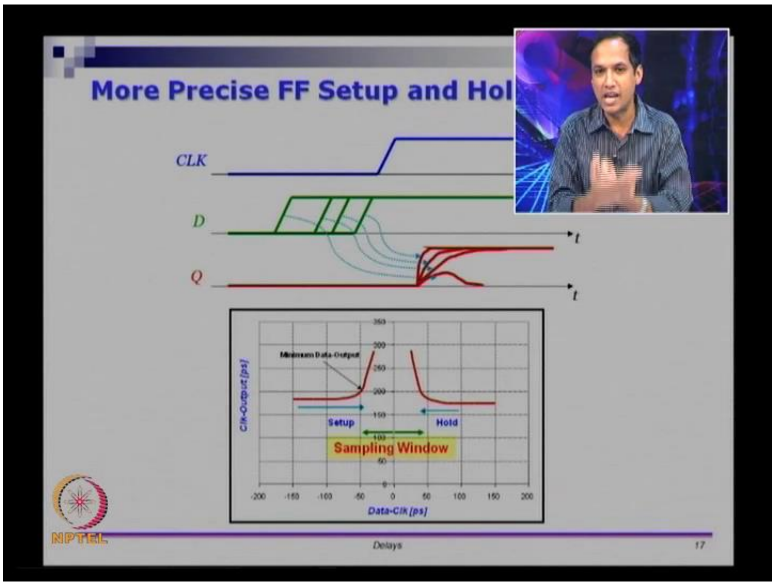

More Precise FF Setup and Hol

So, you always measure clock to Q delay in a flip flop. So, if you want to look at it more precisely, there is a clock, that is there. if the D comes very, very close to it, you can see this wave form here. If D comes very close to it, it may result in something like this. it may not be registered as a one itself. As D goes further and further, D is with respect to the set up time; it is cleaner with respect to the clock. We will see that this wave form outside will come. So, the direction of the arrows are incorrect. So, this is the right most arrow. So, this is the left most red wave form should go to the left most input and the right most one should go to the right most. So, the arrows are drawn incorrectly. So, this is clean with respect to the clock. it will result in a clean output. As you get closer and closer, then the output may not be following the input at all. So, this is the problem and this can happen in real world.

So, generally what happens is you want to bring your clock at some point of time. You change the input either very close to when the clock came in or you change it right after that clock came in and this gets affected. In either of these cases, it is possible that clocked output delay actually increases tremendously. And this is the problem. There is a narrow window in which you want to sample. And in this sampling window if you change the input, then clock to Q delay increases in without any control. And this is the problem.

So, this is what we want from a flip flop. We want a bistable device, we want either one or zero. But, what can happen is in the sampling window if you change the input wave form, then the clock to Q delay will become very high. You may not have one, you may not have 0, the circuit may go into what is called metastable state.

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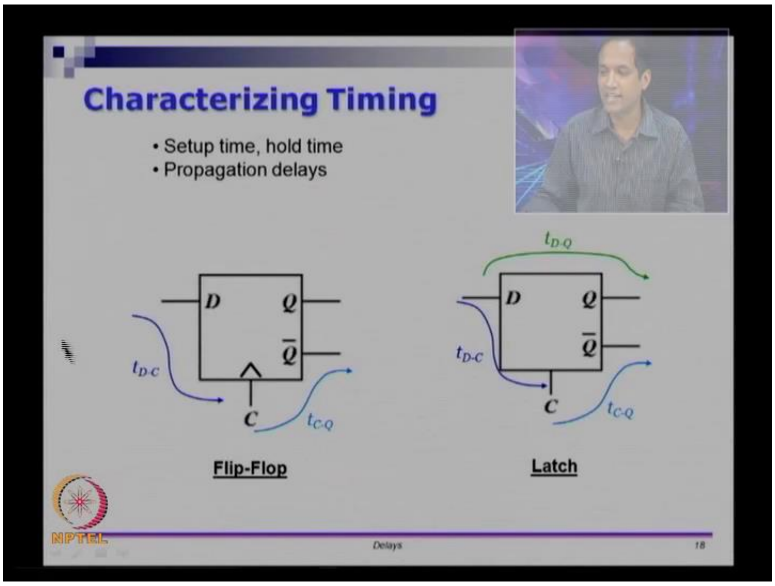

Characterizing Timing

- Setup time, hold time
- Propagation delays

So, to characterize timing there is setup time, hold time in propagation delays. So, for a flip flop there is set up time and a hold time, which is inherent to it. There is a D to C delay, which is the delay between the time period between the delay of D and clock. But, more importantly you are worried about clock to Q delay. Once the clock comes in, how long is going to change; going to take to change q. For a latch, however clock is not just a edge, it is actually a level. So, you are worried about the time difference between D to clock, clock to Q as well as D to Q. What all are the different delays in each one of them?

So, the propagation delay for a flip flop is usually t C to Q; the propagation delay for a latch, it is both D to Q and C to Q. And set up and hold time are inherent proprieties of the basic blocks. The basic blocks require that the input satisfies these conditions.

In the all the wave forms that I have shown, so even though we were measuring, setup time is not measured with respect to one data input or the other. It is a requirement that for the certain period of time before the input arrives, it has to be kept constant. And for the certain period of time after the input after the clock arrives, the input has to be kept constant. So, this brings me to the end of this module.

So, again what we saw is this notion of set up time and hold time. These are properties which are inherent to the basic logical element. And you have to satisfy these properties. You cannot change the input within the sampling window. In the sampling window, the data has to be kept constant for the flip flops to copy the values. In latch, however the sampling window itself is large enough. The change of D during the sampling window will result in a change in q. However, when it gets close to the closing edge of the latch, again you have to keep the data constant, so that the latch does not go into metastable state.

So, we have the basics covered for the sequential elements. We will see in a later week how to take the sequential elements delays as well as a combinational circuits and put together delay and ((Refer Time: 23:05)) for sequential circuits. We will do that in a later week.

Thank you and I will see you in a little while.