Digital Circuits and Systems
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Module – 24
Delays

Welcome to module 24. In module 23, we saw the basics of cMOS and if you have seen the video, then you would notice that, there are lots of electrical parameters that I talked about. You need to have a very, very rough understanding of, what these electrical parameters are and that will be necessary for this video. So, let us look at the notion of Delays. So, in this lecture, we are going to look at Delays.

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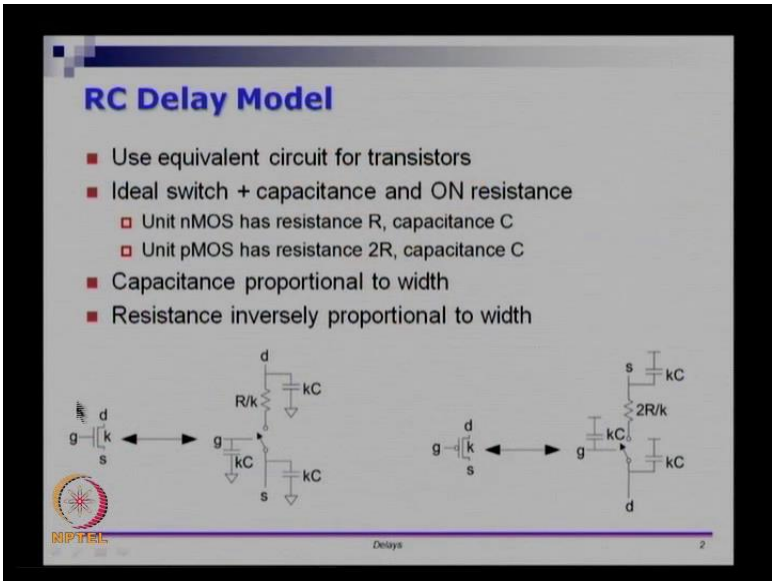

So, I am going to take a basic device, so it could be nMOS and pMOS. So, in this case, if I look at an nMOS device, I want to see, what is the delay, because of this. So, first of all, it is a physical entity, we are going to look at a physical entity, it is not an abstracts switch, where I can talk about 0's and 1's. Eventually, it is an electrical circuit which I want to talk about.

So, there are two devices here, there is a pMOS device and nMOS device. So, there is an nMOS device here and there is a pMOS device here. I want to talk about, how to equivalently transform them into electrical circuits and this will be useful for delay

calculation. What we are going to do is, we are going to assume that, there is this nMOS device here and I already mentioned in the previous video that, there is a gate to various kinds of capacitances, there is gate to drain, gate to source.

So, different kinds of capacitances were there, AND gate to substrate, let us say I add all of them and I put them as one capacitance here. So, let us not worry about these quantities here. So, g is gate, d and s are drain and source and what I have is, if I have an inverter, then I am go to have a nMOS device. So, I am taking one particular nMOS device. So, in this nMOS device, I know that, there are several capacitances from gate with respect to d, with respect to s and with respect to substrate.

So, since all these are capacitances in parallel, I could all add of them up and I will have that as one single capacitance here. Similarly, between the drain and substrate, I have some capacitance; I will have that as a capacitance here. Similarly, I have some capacitance between source and substrate and what not, I will have them here. So, what we have is, we have three different capacitors and I am also going to assume that, this is an electrical circuit.

So, it has equivalent resistance, I am going to assume that, there is a resistance. So, what I am going to do is, I am going to take a transistor and I am going to treated as though it is an ideal switch like here plus some capacitances and resistances. So, once I put in ideal switch here with this extra paraphernalia, all the capacitances and resistances, then I can forget that, there is a switch there. So, I will assume that the ideal switch has 0 delay, I will analyze the delay only in terms of all these capacitances and resistances outside. So, otherwise we need to deal with the actual device every time.

So, instead I will that there is an ideal switch which has 0 delay, but all the delay in the transistor is actually exposed to as though they are because of resistances and capacitances. So, if I have a unit nMOS device, what that means is, if I have a nMOS device of width 1 unit in whatever technology you make, then let us assume that, it has equivalent resistances R and some capacitance C. So, after all these are physical material.

So, physical material, if you put a metal or different kinds of material, you will have some resistance and capacitance, because of that. So, will assume that, unit nMOS has a resistance R and a capacitance C. Typically, in most, in older technologies it is used to be that, unit pMOS device, if I take pMOS device, which has a same bit as the nMOS

device, it is resistance is usually double. So, there is a physical reason why it is, but let us assume, let us takes this for a fact now.

A unit pMOS device usually has double the resistance, but has the same capacitance as though as it is for an nMOS device. So, pMOS device has almost twice the resistance of an equivalent nMOS device, if they are of the same size. So, let us see how nMOS device would look like. We took various gate capacitances lump dump here and we took various capacitances and put them here and there is a resistance here.

So, resistance is usually inversely proportional to the width and capacitance is proportional to the width, again these are to the first order it is correct. So, resistance is usually inversely proportional to the width. So, if I have a pMOS device of width k, then the unit resistance gets divided by k, but the capacitances is all go up by a factor of k. So, if k equal to 1, then I have R here, C here, C here and C here, but if k is greater than 1, then the resistance goes on by that fraction and all the capacitance is go up by that fraction. So, that is true for the pMOS device also.

So, if I k equals 1, I have again equivalent gate capacitance, which have lump at the gate terminal, I have some capacitance, which have lumped at the source terminal and some capacitance which have lumped at the drain terminal. And in this case, the capacitances are actually between Vdd and the source terminal and Vdd and the ground terminal and Vdd and the gate terminal.

Unlike here, where it is capacitance between the ground and the three terminals and now, if I put k equal to 1, I have three capacitors for the three terminals and one resistance, one resistor which has an equivalent resistance of 2R. So, for a technology for equivalent nMOS, you will have twice the resistance. However, if k is greater than 1, if I have a transistor; that is wider, then what would happen is, all the capacitances go up by that fraction and the resistance actually goes down by that fraction. And this is the basic set up behind a pMOS and an nMOS device.

So, now, if I give you a pMOS, if I give a cMOS circuit, I can take the nMOS devices, put this network there, take the pMOS devices, put this network there and treated as though it is an electrical circuit, instead of a semiconductor circuit. And in electrical circuits, we go and look at what is called the RC constant or the RC delay. The product of resistance and capacitance gives you the notion of a delay, higher the resistance larger the delay, larger the capacitance, larger the delay. So, R and C as a product gives you the

overall delay.

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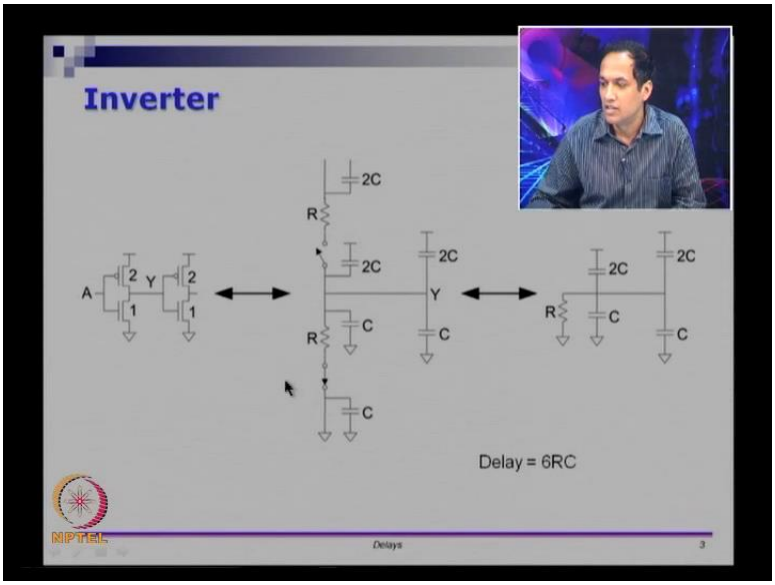

Let us take a basic inverter, so the basic inverter is here. So, let us say, I take this inverter and I corrected to another inverter. So, Y is A bar and let us say Z is Y bar. So, Z is actually A, I have. So, this is just to show you electrical parameter. So, this is not how to design a buffer, I am just showing you, how to calculate various electrical parameters and so on.

So, I have this pMOS device here, instead of a pMOS device, I will put the equivalent circuit here. So, what I have is, I have a transistor of width 2 here for this pMOS and a transistor of width 2 here for this pMOS. So, this capacitances is 2C, this resistor is 2 R by 2, which is R and this capacitance is 2C also. This is the nMOS device, so nMOS device of width 1 will have two Capacitances of C and C respectively and one resistance R.

And if I go and look at it from this gates perspective, this inverter is driving 2 gates, it is driving the gate terminals. It is driving the gate terminals of this device and this device and at the gate terminal of this inverter. So, this inverter has two devices, one pMOS and one nMOS, so this branch is seeing a capacitance of 2 C and this branch is seeing a capacitance of C.

So, the equivalent circuit as seen from this inverters perspective is this set up. At this point, we can assume that, these resistances, so these two switches are ideal switches. Now, if I put A equals 1, then this switch will act as a conducting switch and this switch

is open or non conducting and if we go and look at the resistance, then this is the pull down network, if I put A equals 1, this Y will get pull down. So, what you have is, the equivalent electrical circuit for the pull down network.

So, this capacitance and this resistance gets detached, you are not in charge for that; however, you have this capacitance, this capacitance, this, this 2C and C. So, what you have is, you have this resistance and you have equivalent of 2C plus C plus 2C plus C are six equivalent capacitances. So, we have to discharge six equivalent capacitances through a resistor R, which means the delay of the circuit is 6 times RC.

So, let me just quickly run you through what I did. I took two inverters, from this inverters perspective, if I go and look at the delay. What it has is, this is the equivalent of the pMOS device and this circuit is the equivalent of the nMOS device and the capacitance that you are seen, because of the load from here this 2C and C here. And if I put A equals to 1, then this device is cut off. However, this device is on, when this device is on, this capacitor does not have to discharge.

So, it is already at 0's, so this will 0, you have this capacitor here and this 2C here and this 2 C and C are here. So, if you add all of that up, that is 6 C, so delay is 6 times RC for this inverter to pull down the output from 1 to 0. Similarly, if this transistor is closed and if this transistor is open, then you will have a 2C here and 2C here and you will have these two capacitances and this capacitance here.

So, equivalently you can go and derive the delay for it and you will see that, the delay is proportional to R and C. So, there is some constant involved here, it is proportional to R and C. So, this is the notion of a delay. So, if I have this delay equals 6 RC, this is what is called the high to low delay, if the output goes from 1 to 0, to do that, I need delay of 6 units or 6 RC.

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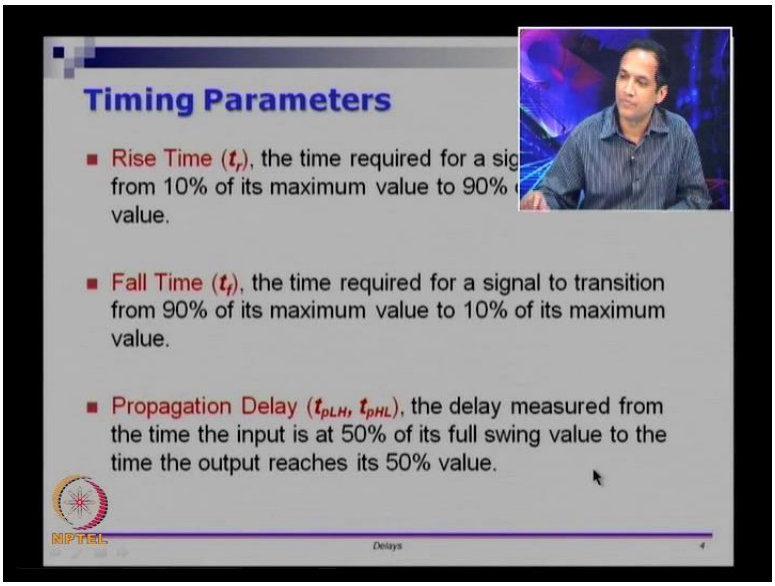

So, let us look at different parameters now with related to timing. The first parameter we are going to call it Rise time, rise time is, if I give you a voltage waveform, then the time required for a signal to transition from 10 percent of it is maximum value to 90 percent of it is maximum value is called the rise time. And fall time is the time required from 90 percent of it is maximum value to 10 percent of it is maximum value.

So, generally the maximum voltage that we want to operate the devices at Vdd, so we are talking about 10 percent of Vdd to 90 percent of Vdd is the rise time and the fall time is 90 percent of the Vdd to 10 percent of the Vdd. And propagation delay is usually you measure from when the input crossed 50 percent of the input voltage to the time at which the output goes from, crosses the 50 percent value.

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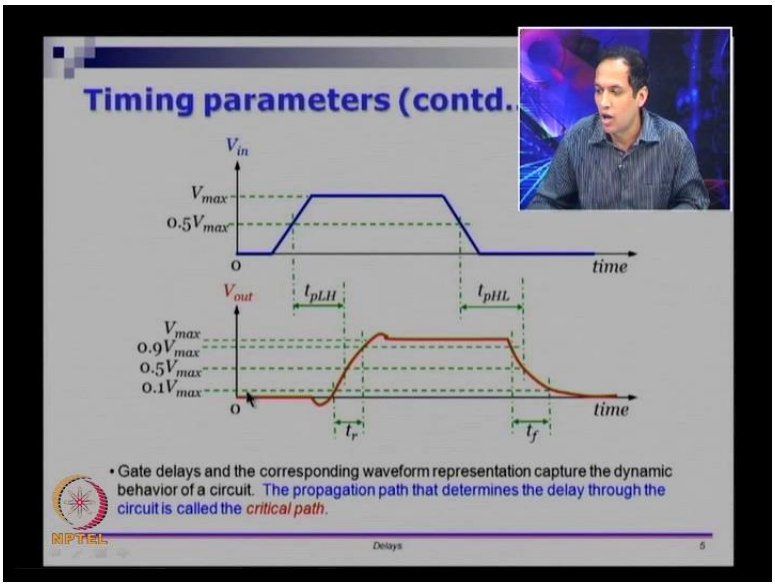

So, let us see various parameters as we go along. So, let us look at this picture here, we have this blue waveform here and this 0.5 times V max is here. So, if I measure the amount of time taken to go from 0 to Vdd, so that is usually the rising edge, this is the rising edge. Instead of measuring from 0 to Vdd, we usually measure from 10 percent of Vdd to 90 percent of Vdd; that is usually called the rise time.

And similarly from 90 percent of Vdd to 10 percent of Vdd will call that the fall time. So, this signal is usually an ideal signal; however you may have a waveform, which is somewhat like this. So, this is what you may see in a real circuit, it may not even be and nice trapezoidal structure like this, you may see things just slightly different. And the notion of tpLH or the propagation delay from low to high is, if I give this as the waveform, what is the time taken for the output to go from low to high? That is called tpLH and tpHL is from 50 percent of the input to 50 percent of the output, whatever time it takes, that is called tpHL.

So, this is just a circuit to illustrate various examples and with these waveforms, you can understand, what rise time and fall times are, what tpLH and tpHL are. So, basically LH is low to high, HL is high to low, t r is rise time and t f is fall time. So, various ways in which you can measure the delay itself is possible. And when we have various gates, gates have different values for tpLH, tpHL, t r and t f; we need to be able to combine them and say that this is the delay of the circuits.

So, eventually, if I want to sell you a chip, saying that, so this is my processor and it will

run at 2 Giga hertz, I want to tell you that, this will be operating at 2 Giga hertz. So, which means every 0.5 nano seconds, you should be able to do an operation. You are not quit worried about, whether it is rising from low to high or going from high to low and so on. If I give you two many parameters, it is very confusing, but this is the underlying set up, the underlying set up is, we have all these parameters.

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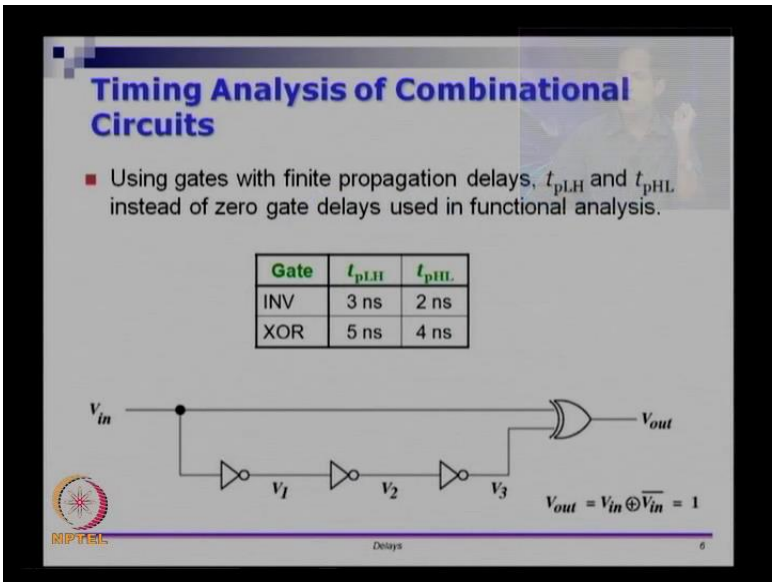

So, let us look at how to analyze the combinational circuits for the delays. So, for every gate, I can associate something called tpLH and tpHL. So, there is a certain time, it will take to go from low to high and there is a certain time that it will take to go from high to low. Typically, tpLH is usually higher than tpHL. This is because of the asymmetry between nMOS devices which will bring down the value from high to low being better conductors than pMOS devices which can pull up.

So, pulling up takes more time usually and pulling down for circuits that are, for transistor that are sized similarly. So, let us assume that, you have a circuit like this. So, I give you a circuit V in and there is V out. And what I have done is, I have taken V in, I give it in to XOR gate and I have given three inverters here and so on. If I do something called basic functional analysis, functional analysis is I want to derive V out in terms of V in as an equation.

Then V 1 will be V in bar, V 2 will be V in itself, V 3 will be V in bar. So, V out will be V in XOR V in bar. So, anything XOR with it is complement is 1, so V out will be 1. If I take this circuit and if I logically analyze it, V out should be the same as V in itself.

However, all these inverters and this XOR gate have delays in them, they take a certain time once an input appears, they take a certain time for the output to switch and I want to characterize that.

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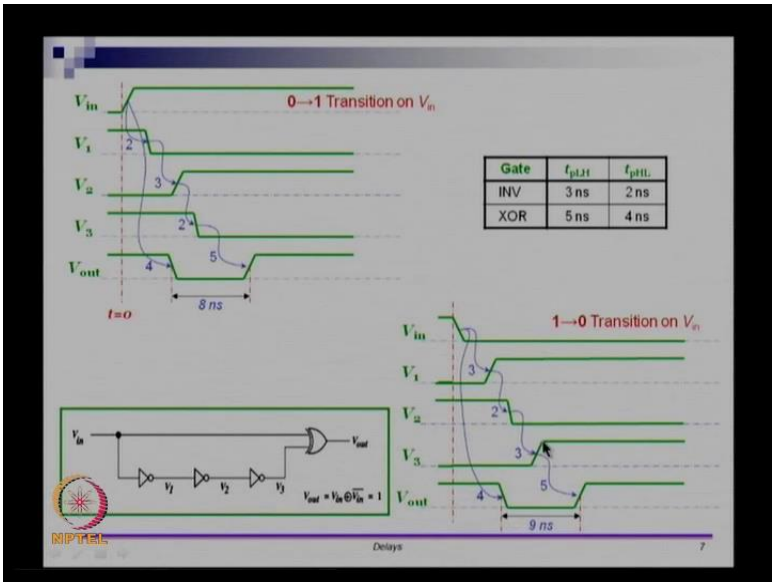

So, let us see the delay of this circuit, so the circuit is given here and the delays are given here. So, let us start with the waveforms, I will start with time t equal to 0 and let us say that, there is a 0 to 1 transition at the input. So, I know the high to low and low to high transition delays for each of these gates, I want to see, what is the transition delay for the whole circuit? So, if I give 0 to 1 transition at V in, V in is directly connected to V 1 and this XOR gate.

So, at delay of 2 units, I can expect V 1 to change from 0 to… So, V in is changing from 0 to 1, I can expect V 1 to change from 1 to 0. So, this 1 to 0, this is the high to low delay the inverter; that is 2 nano seconds, if we observe the output of output V out, V in is also driving V out. So, the output is also going from high to low, let us assume, if it is going from high to low, then it is delay is 4 nano seconds.

You can see that this transition from 0 to 1, this causing V out from 1 to 0. Since, study state V out would have been 1, if I give V in and if I give any V in, then output will be 1 at all the time. However, if there is a change in input from 0 to 1, what is happening is, there is change in output from 1 to 0. So, that is there, now this transistor has seen a change in it is output. So, this inverter has seen a change in it is input.

So, it reacted and it is output change from 1 to 0, which means, V 2 inputs this changing

from 1 to 0. So, V 2 will go from 0 to 1, but that is the tpLH delays, it is going from low to high. So, we are looking at 50 percent of it is input to 50 percent of it is output; that should take 3 time units, because that is what the inverter says. Then, you look at V 3, V 3 is input is changing from 0 to 1, which means, it is output to change from 1 to 0, but that is the tpHL part of the inverter.

So, that will have and finally, so V 1 settled down already. So, you can see that V 1, V in settle down already with respect to this XOR gate, V in as already settled down, but there is a change in V 3. This change in V 3 is going from high to low. However, this is going to flip the XOR gate to go from low to high, if you go and look at low to high of the XOR gate that 5 nano seconds. So, after 5 time units, when after this transition, you will see this transition.

If I go and look at, what is happening here, this output is suppose to be remaining at 1 through and through. However, because of the changing input, there is some change in all the input waveforms here, which is changing input waveform at the XOR gate. The XOR gate momentarily goes to 0 and then the output goes back to 1. Logically, it should have been 1 all the time, but it momently goes down to 0 and comes back up and that is about 8 nano seconds delay. So, it is taking about 8 nano seconds of time.

So, for the 8 nano seconds, what we have is something called a glitz. The output should have been 1, but it goes momenterly to 0 and then goes back to 1. So, let see, what happens if there is a 1 to 0 transitions in V in, 1 to 0 transitions on V in will make V 1 rise after 3 time units, V 2 of all after 3 plus 2 equal to 5 time units and V 3 to raise after 5 plus 3 equal to 8 time units.

So, at time t equal to 8, XOR gate is going to see a change from 0 to 1. This XOR gate is going to see V 3 changing from 0 to 1, the XOR gate also see is V in changing from 1 to 0 at time t equal to 4, because that is the tpHL delay. So, that is 4 time units. So, the change in the input here as resulted in the change in the output here at the time t equal to 4 itself, however there is another change is coming through the another path, which also results in change in the output.

So, this time the changes from 0 to 1 and for about 9 time units, the output is not in the steady state, the steady state output must have been 1, but the output is not in the steady state, there is a glitz of time period 9 nano seconds. So, this is a way to analyze combination of circuits. So, remember this is a still combination of circuits, because

there is no feedback path.

Generally, what we do is, we determine the worst case propagation delay to this circuits. So, if look at the previous slide, ((Refer Time: 22:57)) this circuit can either I can report to delay of 8 nano seconds or 9 nano seconds, but I have to say that for 0 to 1 transitions and back to. So, from 1 to 0 transitions and back to 1, it is going to take 8 nano seconds. However, the input goes from 1 to 0, the output will go from 0 to 1, 1 to 0 and back to 1 and that will take 9 nano seconds. So, every time have to report to delay values. Typically, what we do is, we take the worst case delay and report that has the delay of the gate.

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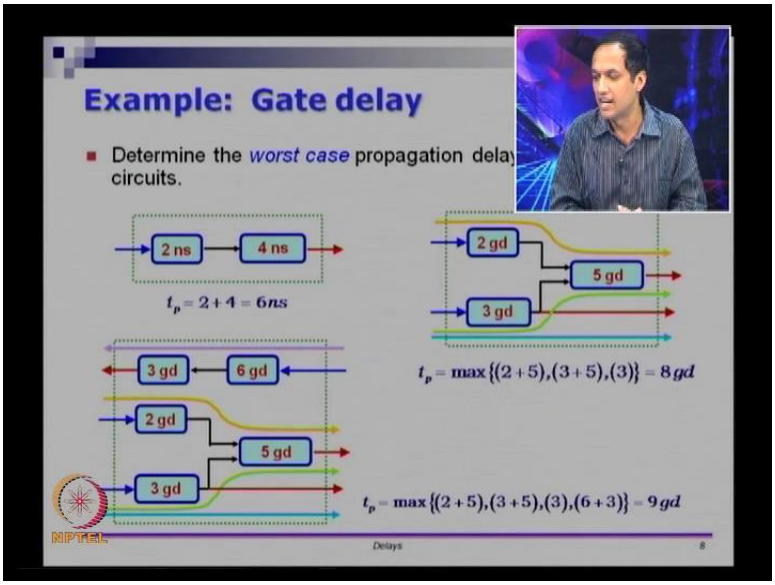

So, we have a gate here, which is of delay 2 nano seconds; that is the worst case delay, whatever it takes. There is some other gate which has delay of 4 nano seconds and if I may a circuit which puts these two, back to back, I want to find out what is the worst case delay; that is happening in the circuit. If I put 2 components back to back and the propagation delay for this one, could be any change input here in the worst case will required 2 time units to come here plus another four time units to go here. So, it is t p is 2 plus 4 equal 6 nano seconds here.

So, is the slightly straight forward, I take the worst case here, I take the worst case here, I add both those up that I will give me the worst case here. Let us take this circuit is a slightly more complicated. We have some gate here and another gate here, which is feeding another gate here and which is driving one of the outputs. The output of this gate

is also directly given to the output of the circuit.

So, in terms of the circuit over all circuit, I have 2 inputs and I have 2 outputs, I want to capture the relationship between these inputs and these outputs. I want to see, when these outputs will arrive depending on when the inputs were given or I want to calculate that time different. So, let see what the delay is in the circuit R. So, if I change this input here, then it will take 2 time units to come through this plus another time units. So, this red line will change at 7 time units, if thus a change in input here. So, that is the first part.

The second path is this path, in this path, if there is change in input here, then after 3 plus 5 equals 8 time units, the red line will change. So, the red output this is top output the one here can change either at 7 time units or at 8 time units depending on which input changed. If I do not tell you, which input changed, if you ask the question, what is the worst case delay. Then, we take the worst case path, which is this green path and we have to report this output in the worst case will change 8 time units after any of the inputs have changed.

In fact, it is only this input change that the results in 8 time units delay; this input is actually straightly faster. However, the worst case have to report 8 time units and there is also the direct path from this line going through this gate to the output; that is the blue line and this change in input will result in a change in this output. The change in input from of this line will not change the output there. So, only this input can control this output. So, that is 3 time units.

So, t p is maximum of 2 plus 5, because of the yellow path, 3 plus 5, because of the green path or 3, because of the blue path. So, t p is 8 gate delays, if I treat this whole thing as black box, if I do not specify various input output combinations, if I just ask you what that delay of the circuits. Then, you have to give me the worst case delay through all the paths for all the outputs with respects to all the inputs.

So, this is crucial, if I just ask you for what is the delay of the gate, you have to first of all find out all the input output paths. And I want just 1 number which means you have to take the maximum of all the path delay across all the different gates and whatever their connections are and so on and you capture the relationship between all outputs to all inputs.

So, if I want something specific, then this output line is only 3 units away from this input and the change in input here will not really change this second output line. However, as a

circuit, it takes 8 time units the worst case, because you do not know, what input is going to come the worst case is going to take 8 time units. Let us do a slightly different circuit in this case, there are two sides. So, this circuit is given here and there is another circuit.

So, let say, there is agent a here and agent b here, agent a is giving some inputs and transforming it. So, this circuit is transforming a's inputs and giving it has input as b, it is also taking something from b and transferring it back to a. So, that is what this green box this circuit is doing. If I want to calculate the delay of that, then we already know the delay of this sub circuit it is 8 time units.

However, there is also path going from this direction to this direction that will have a delay of 9 time units. So, as a circuits this green box will take maximum of all of those. So, it is a maximum of 2 plus 5, 3 plus 5, 3 and 6 plus 3 or 9 gate delay 9 time units. So, in the worst case, if I ask you, what is the delay through this, you have to report that it is 9, because without telling you the inputs and outputs requirements that I have. If I ask you for the delay of the circuit, it is actually 9 time units in the worst case you have to do it for you have to wait for 9 time units.

So, this notion of waiting for 9 time units and so on in is this necessary this understanding that it will take. So, much time is necessary we will look at the notion of timing analysis in a later video, but has of now these are combination circuits. So, if I the gates have basic delays, you can calculate the delays of combination of circuits.

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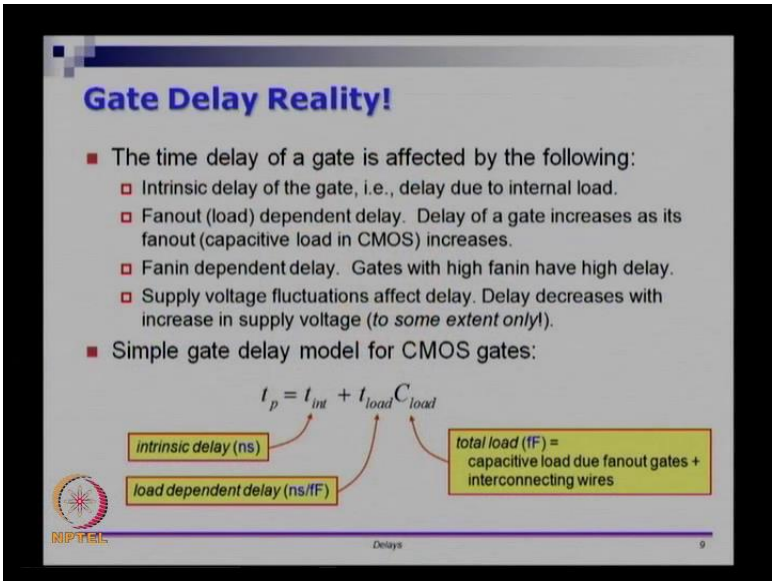

In reality, gate delay are not so simple, the time delay of a gate is affected by various

parameters. So, typically the propagation delay is the intrinsic delay plus some factor due to the load. So, there is every gate has some intrinsic delay plus depending on what here connecting to it may take some output. So, I can give you a small analogy here, let say, I am teaching the live class room and there are two parts of this preparation for this class.

So, I need some amount of time to prefer for the class itself and let say, I give you and assignment and if there are 10 students I need to grade 10 homework papers, if there are 100 students, then I have to grade 100 homework papers. The amount of time that I take to prepare for the class is the intrinsic delay, whether I am teaching 10 students or 100 students or 1000 student, I still need to prepare for the class that is intrinsic delay.

And then there is low dependent delay, depending on the number of students, there is there in the class, the amount of time that I will take to in preparation for this course will wale. So, t p equivalently an electrical circuit the propagation delay of a gate is where is in sum intrinsic delay plus something due to the load. Even, if the circuit is not loaded, even it is not connected to the anything, there is always sum intrinsic delay or some basic delay that the gate will have. So, change in input will take some finite amount of time to change the output.

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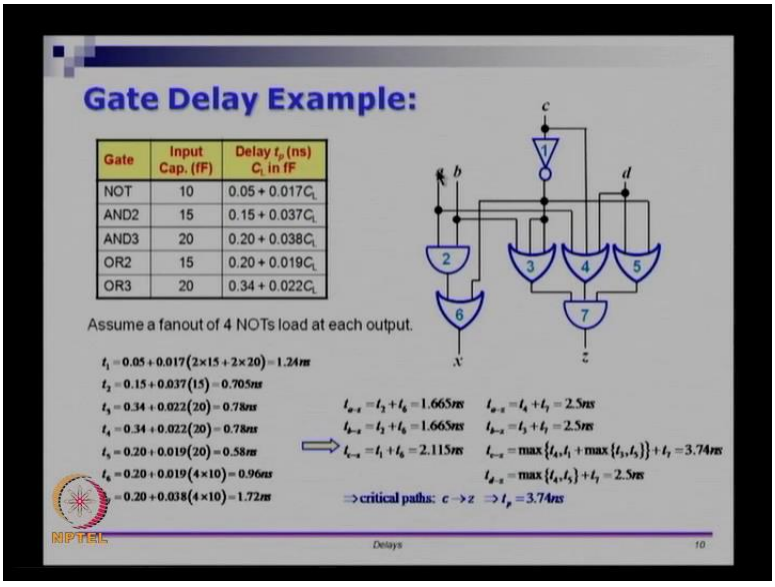

So, let us take is slightly complicated example, what we have is, we have various gates here, we have one inverter here, which is gate number 1. We have 2 OR gates, which have 3 inputs, 2 OR gates, which have 2 inputs, 1 AND gates with 2 inputs, 1 AND gate with 3 inputs. So, all the gate types are listed here, let us assume that, the input

capacitance for each one of these gates are given here.

So, it is 10 from to ((Refer Time: 31:47)) 15 from to ((Refer Time: 31:48)) and so on and I also know for each gate, there is some intrinsic delay plus some factor into the load that the gate drives. So, for NOT gates let us assume that the intrinsic delay 0.5 and the load dependent delay is 0.17 in to C L. So, this is the overall propagation delay of the NOT gate.

Similarly, the 2 input AND gate, there is in intrinsic delay of 0.15 plus output dependent delay of 0.37 times C L and so on. And let us also assume that, x is connected to a load which I equivalent of four inverters, z is connected to a load, which is equivalent of four inverters, let us assume that is this is the basic setup. So, each gate has in intrinsic delay and each gate also offers some inputs capacitance to it is to driver.

So, this gate number 2 will offer some capacitance in 2 inputs and b, the gate number 6 will offer some capacitance to input capacitance is the gate number 2 AND gate number 1 and so on. So, let us look at the delay through each of these gates. So, let us look at t 1 first once you understand t 1 is worked out, the other things are all straight forward, let us look at t 1 worked out. The delay through t 1, if I look at gate 1, any change in input C will change in the output here.

So, you look at the output of gate 1, it is connected to gate 6, gate 3 AND gate 5 correct. So, there are three places were the gate is connected and so now, let us look at the overall delay. So, if I look at delay through the inverter, it is 0.05; that is the intrinsic delay plus 0.017 into C L or whatever the load capacitance. What is the load for the inverter? There is a load coming because of this input.

So, in fact, there are two places to which it is connected. So, this C bar is connected to 2 inputs of the OR gate and this is 3 input OR gate. Let us look at the 3 input OR gate, at the 3 input OR gate offers a load of 20 firm to fair it is to it is drivers. So, you have 2 into 20 here, because of that and if you go and look at where else is going is going to gate number 6 and it is going to gate number 5. So, gate number 6 will offer input load capacitance of 15 firms to fair it is, because OR gate 2 offers 15 firm to fair it is input capacitance.

Similarly, this OR gate 5, number 5 is also 2 inputs OR gate; that also gives another 15. So, 0.05 plus 0.07 into 2 times 15 plus 2 times 20 is 1.24 nano seconds. So, that is the delay of the inverter t 1, let us look at t 5 for instance. So, if I want to calculate the delay

of the t 5, then t 5 is driving only 1 gate, which is an NAND gate. So, let us look at t 5, it is a 2 inputs OR gate. So, 2 inputs OR gates delay is points 0.2 plus 0.019 times, it is load capacitance.

What is the load capacitance? Load capacitance is coming because of 7 and this is the 3 input AND gate, 3 input AND gate offers capacitance of 20 to it is driver. So, you put 20 here. So, 0.2 plus 0.019 time 20 is 0.58 nano seconds. So, let see how t 6 and t 7 are calculated. So, t 6 if you go and look at t 6 t 6 is 2 inputs OR gate. So, 2 inputs OR gate and it is driving. So, as assumption says here is driving four inverters here. So, t 6 has point to plus it is going to drive four inverters here, so that 0.019 times 4 into 10; that is 0.969 nano seconds.

Similarly, this AND gate here t 7. So, if you go and look at 3 inputs AND gate, so that has 20. So, it is offering 0.2 plus 0.038 into C L, so that is 0.2 plus 0.038 into 4 times 10, because it is we are assuming that, there are 4 NOT gates that are connected and 4 NOT gates gives to 10 firm to fair it is as their input capacitance. So, that is 4 into 10, the delay is 1.72.

So, again if I break it down what he did is, every time I want it to calculate the delay through the gate, I first of all look that what the gate is look at the formula and once, I know the formula I need the load capacitance though. So, the load capacitance, I go and look at where all it is driving, I will pick up those gates and look at their input capacitance, I will add all of them appropriate and that is what I did here. This is the delay through each of the circuit components.

If I want to delay through the circuit itself, then there are several paths, there is path from a to x, their paths from b to x, then there is path from c to z, d to z, then there is a path from a to z, b to z and so on, there are several paths that are. For each of these paths, so if I look at t of a to x is going through an AND gate and an OR gate, I look at the delay of the AND gate is 0.7 o 5 delay of the gate number 6 is 0.96. So, I will add 0.96 and 0.7 o 5 that gives me 1.665.

If I go and look at b to z, b to z goes through gate number 3 and gate number 7. So, I am looking at this here gate number 3 and number 7, gate number 3 as delay of 0.78, gate number 7 has a delay of 1.72, I add all have that are that is 2.5. Let us look at c to z and d to z these are more interesting, if I look at c to z, there is path coming from c through 4 to 7 to z, there is path coming from c, through gate number 3 to 7 to z. So, there are two

parts.

So, if I have two paths I have to look at the maximum of the delays and that is what this one does. So, if I look at t of c to z, there is one path going through 4. So, it is t 4 or t 1 plus t maximum of t 3 comma t 5. The reason is, it is going through two different path and finally, it is converging at t 7. So, what we have is, so let us do the slightly more carefully. So, all changes in c will take t 7 any way. So, t 7 is added outside and there are multiple paths to go from c to z.

So, I want the maximum of all those paths and to find out maximum of all these paths, I go and look at each one of these path, c to z goes through 4. So, there is t 4 there, then c to z also goes through t 3 comma t 5. So, I take the maximum t 3 comma t 5, but both of them go through the inverter first. So, you look at this input, it goes to t 5 and this also goes to d 3.

So, maximum of t 3 comma d 5 plus t 1 is the delay d 2, the path going through the inverter; t 4 is the path that is going without the inverter, all of them go through t 7. So, if that is the expression eventually we get and if you do the arithmetic, it will be t 0.74. If you look at t of d to z, so d has one path going from 4 to 7 and then one path going from 5 to 7. So, both of them have 7, so you have t 7 plus maximum of the delay through t 4 or t 5. So, t 4 and t 5 you pick up the delay from here 0.78 and 0.58 the maximum of that is 0.78 add it to delay of 7 is 1.72 summation of that is 2.5.

Now, if I go and look at all these delays, t of c to z is 3.74, which is the largest of the delays. So, in the worst case if I do not know anything about when the input are coming and so on is possible that c come the last and because of it is z will change at 3.74 away from that. So, this path, were he takes the largest delay is call the critical path. So, critical path there is c to z, it is the critical of all of these delays. So, that takes 3.74 time units.

So, this is the how you analyze the delays of combination of circuits. So, what we will do in the next lecture is, we look at some basic of sequential delays. So, circuit elements which are sequential elements will see how the delays are coming through. But this is the slightly involved example, but I suggest that you go through this to understand what we are done so far.

So, in this circuit is I took the appropriate formula added the appropriate loads and got the delays for each of those gates, then I look that all the paths going from inputs to outputs and I added up the all delays carefully. So, I got several path delays and from the

several paths delays, I pick the path with the largest delay, I call that the critical path. I say that the delay of this whole circuit is now 3.74 nano seconds.

So, all these other internal details are now hidden away from you, if I have to cell this circuit you, I have to say that in the worst case is going to take 3.74 nano seconds of delay and for some input cases, it could be faster. But in general I have tell you that is going to take 3.74 nano seconds delay and that is why I can say the circuit I cannot say that the circuit is faster than that. So, I will stop this video at this point and we will resume which sequential elements in the next video.

So, thank you so much and I see you in a little while.