Digital Circuits and Systems
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Module - 23
Logic Gates and Electrical Properties

Hi, welcome to week 5's lecture series. We are in the middle of the course now. And I am happy to see that, many of you submitting assignments and quizzes and so on. The forums are also quite active. So, I have one short request though. I see that the number of quiz submissions are going down. And there are still many, many questions that are being asked on the forum to which I have repeatedly given answers earlier. So, I suggest that you go to the forums and search for questions before you open a new thread, because new thread would mean more confusion. So, I try to mark threads as duplicates also whenever possible. But I suggest that you go and search on the threads on the question that you have. Especially when it is related to quizzes, you can go and search on the quiz number and the quiz question; I am sure there are students who have had similar questions and so on. So, I suggest that you use the forums more effectively.

So, coming to this week's lectures; so I am going to talk about a few different things this week. So, first of all, I am going to talk about the notion of delays in circuits. So, this is something that we have not seen so far. And being electrical components, they have fundamental intrinsic delays. Gates have fundamental intrinsic delays. So, I want to talk about what is the nature of the delay and what is the source of the delay for electrical components. And we will see how delays add up and so on in a circuit. We will do that for one or two lectures and then will switch back to sequential circuits and we will start looking at sequential circuits in a little more detail. And as before, I will also have something in verilog at the end of the week. So, let us start with other notion of delays. So, this lecture and the next lecture are going to be slightly more inclined towards electronic circuits than rest of the videos that we have seen so far. So, if you are from background that has electronics; so this will probably be something that is familiar to you. But, even if you are not, I am going to try and keep it at a level where you can understand and appreciate the fundamentals if you know basic electrical engineering and basic electronic circuits. So, I will not get into too many details or derive too many

equations. But, at a very top level, I want to give a notion of where the delays come from for a digital circuit.

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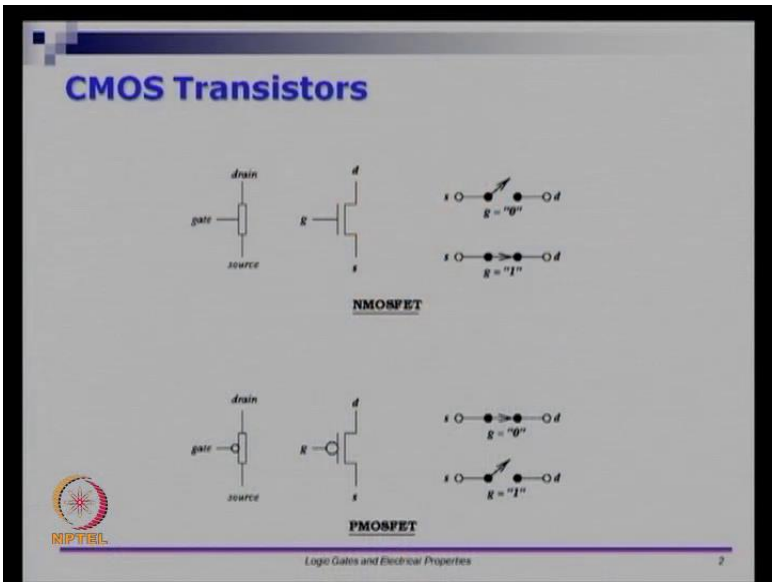

So, let us start with basic CMOS transistor. So, CMOS stands for complementary metal-oxide semiconductor. So, it is a semiconductor transistor. And this is something that you may learn in more detail if you take a VLSI course later. So, even if you are CA student, the video that I have today and the next lecture will have similar flavor that you will have to understand basic electrical circuits and I am sure you have that from your twelfth grade or from your first year engineering. So, let us start looking at a transistor. So, transistor is usually a three-legged device. So, you have something called the source, something called the drain, and another terminal called the gate. And the NMOS transistor… There are two types of CMOS transistors. So, there are two types of transistors used in CMOS; there is the first type called the n-type MOS and the second type called the p-type MOS. So, these are symbols used for n-type and p-type respectively. You can see that, there is a bubble at the gate terminal for the p-type; whereas, for the n-type, there is no bubble. So, let us see what these transistors actually mean.

So, as I said earlier, transistor is a switch. So, NMOS type switch has two different positions. If you apply a 0; if I put voltage equivalent to 0; g equals 0 at this terminal; then the switch is open or non-conducting. So, any voltage that you place at s will not be seen at d; however, you apply gate voltage 1; then the gate is closed or you can see that it is conducting; and when it is conducting, any voltage that you place at s will be seen at d.

So, you have source and drain, which are the two terminals in which you want the voltage relationship to be captured. And a gate terminal, which actually controls whether d follows s or d does not follow s. So, this is the deal with NMOS transistor. In a PMOS transistor, the opposite of what the NMOS transistor does. When g equals to 0; the gate is closed. So, anything that you place at source will be at drain. And similarly, when g is 1; the transistor is considered open or non-conducting. And any signal that you place at s will not be seen at d. So, s and d are disconnected in that case. So, this is the basic setup behind a PMOS and a NMOS transistor.

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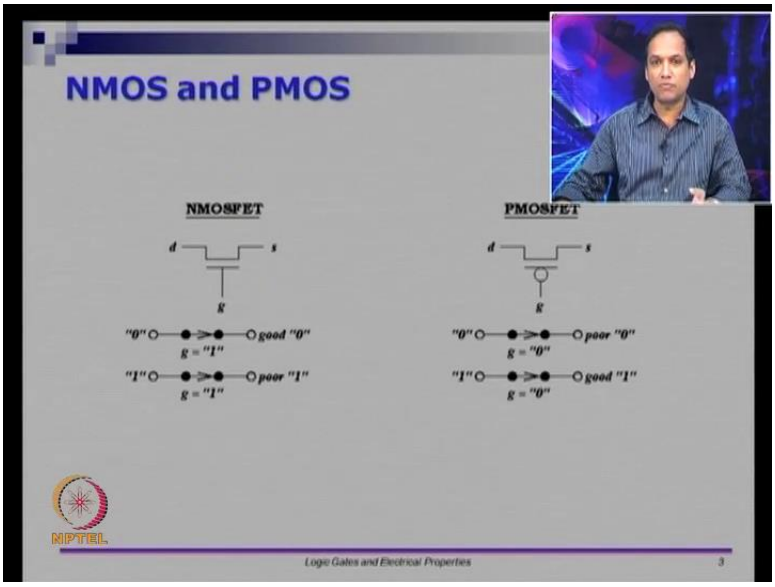

And there are a few properties of PMOS and NMOS transistors. So, what you saw earlier in the previous slide is just a switch-level description; but there is also something which I have to talk about electrically. So, typically NMOS transistor is a good conductor of 0, but a bad conductor of 1. So, let us assume that, g is equal to 1; which means the gate voltage for the NMOS is 1. So, the gate will remain closed; which means it will form as a conducting device. But, 0's are conducted better than 1's in a NMOS device. Equivalently, a PMOS device when it is closed; which means when g is equals to 0, it can conduct; but it conducts 1 better than 0's. So, this is something that you have to remember. Both NMOS and PMOS devices are different in the way what gate voltage is applied for it to close the path to act as conducting device and they also differ in which voltage level they conduct better. So, NMOS device conducts 1 better and PMOS device conducts 0 better.

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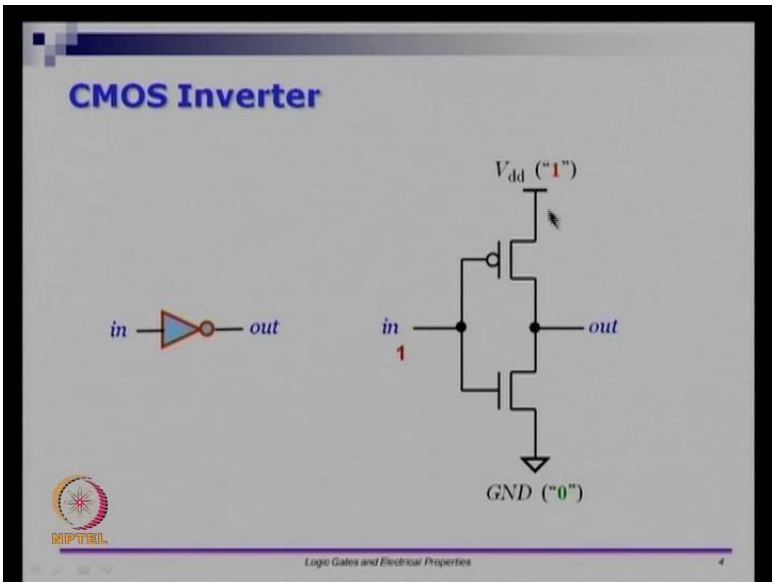

So, with this in mind, let us go and look at a basic inverter. So, we know that, the electrical symbol for an inverter is this; I am going to show you electronically how this device would look like. So, electronically, this is what you will have. You will have… This is called a fully-complementary MOS inverter. So, you have a PMOS device and an NMOS device. And the gate input for both the transistors are connected to the input. And for this PMOS device, this is the source and this terminal is the drain. For the NMOS device, this is the source and this terminal is the drain. So, the source terminal is 1 or V dd for the PMOS and the source terminal is ground or 0 for the NMOS device. And what we do is we connect the drains together and we will call that the output.

Now, if you want to see how this inverter would work; so if you place let us say 0 at the input here; we know that PMOS device will be conducting when you place 0 at the gate input. So, this device will be conducting; whereas, this device will not be conducting. So, you can as well as assume that, there is no connection between output and ground. So, this path is open because 0 applied to the gate voltage of the NMOS device will turn the NMOS device off. The PMOS device is turned on; and as I already mentioned, it is a good conductor of 1. So, you would expect the V dd that is placed here to conduct. So, you have a V dd equal to 1; because of this being a conducting device, you will see that, this output or the drain gets charged to 1. So, this happens when the input is 0. So, when the input is 0, the output is 1.

Let us see what happens when the input is 1. If the input is 1; then we know that the PMOS device turns off and NMOS device is going to turn on. So, the NMOS device is

on; at this point, if this voltage is kept at 1; if the input is 1; because this is opening; so you have in equals 1. Now, this transistor is going to be conducting. And if output voltage is 1, this will now discharge through this path, because there is a path to ground; it will discharge. So, in summary, what you have is you have two devices, which are connected like this; you have two drains connected together and the two gates connected together. If the input is 0; then this device is on; V dd will make the output charged to 1; if the input is 1; then this device – the NMOS device is on and any output voltage that is there will discharge through this device to the ground. So, this is the basic setup of a CMOS inverter.

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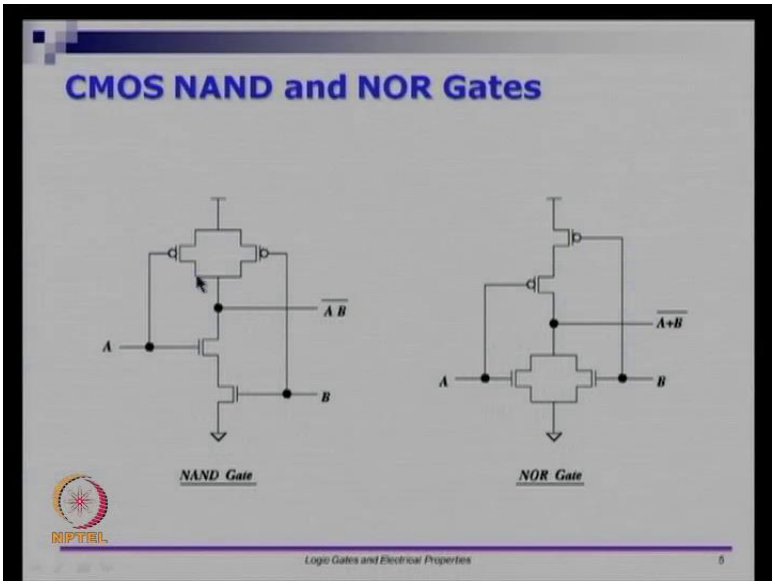

Now, let us look at how to make more complicated gates – so more complex gates – NAND and NOR gates. So, if you want to realize a NAND gate, what you have to do is you have to take two PMOS transistors; connect them in parallel. And take two NMOS transistors; connect them in series. And you take one of the inputs A connected to these two transistors as follows. So, you connect it to one of the PMOS and one of the NMOS devices. And similarly, take B and connect it to the other sets of inputs. Now, let us go and think about how this will work. So, let us first take the case; where, both A and B are 1. So, if both A and B are 1; then this is 1; which means this device is turned on. B is 1; which means the bottom NMOS device is also turned on. If both of them are turned on, then any output voltage that is there will discharge through the two devices and go to 0. So, if both the inputs are 1, the output voltage will discharge to 0. So, this is the characteristic of a NAND gate. If both the inputs are 1, the output is 0.

And the rest of the combinations – 0 0 0 1 and 1 0 combinations – the output should remains at 1. So, let us see how that will work. Let us take the case, where one of the inputs is 0. So, let us say A is 0. If A is 0; then the PMOS transistor on the left will turned on. But, this device will still be turned off. So, because this is turned on and you have parallel paths going through this device as well as this device; this output line will get charged. So, you can see that, if the left PMOS device is turned on, you have a path that goes from V dd through the device to the output line. So, it will get charged; it will become 1.

And because this device is turned off; this – whatever you are charging cannot discharge, because this device is turned off. So, if you keep A equals to 0; then you have this output line charging to 1; by symmetry, if B is kept at 0, the output will charge to 1. If both are kept at 0; then you have a path, which is conducting through this device as well as through this device. So, you have two paths through which the output line can be charged. So, v dd – you have two paths through which it can be charged. And in fact, the output will get charged faster. We will see why later. And for the combination when AB is 0; both these devices are turned off; which means there is no path to discharge the output voltage. So, essentially what we have is if both the inputs are 1; then these two transistors in series are on and you will have discharge; otherwise, you will charge it to 1. So, this is the case for a NAND device.

For a NOR gate, it is very similar to this, except that series and parallel are switched. So, you put two PMOS devices in series and put two NMOS devices in parallel and you get a NOR gate. So, again if you want to see how this will work; we know that, the combination 00 will keep it charged; all the other combinations will keep it discharged. So, if we put 0 for A and 0 for B; we can see that, both these devices are turned on. So, v dd will actually charge through both these things and the output will get charged. However, if one of them is 1 and other one is whatever it is; if one of them is 1; then one of the PMOS transistors will turn off; which means there is no way to charge the output line. However, what would happen is if one of them is 1; there is a discharge path through the NMOS devices. So, this part is the NMOS device. So, you have one of them will discharge; through one of them, the output will discharge and the output will go to 0. So, generally, what we have is we have what is called the pull-down network in the bottom and pull-up network at the top. A pull up network is responsible for making the logic circuit 1 – the logic output 1; and the pull-down network is responsible for making

the logic output 0.

In fact, if you want a three-input NAND gate; then you have to put another PMOS transistor in parallel here and one NMOS transistor in series. If you want a three-input NOR gate; then you have to put one PMOS in series here and one NMOS in parallel here. So, this is how NAND and NOR work. In fact, you can notice that, if you want AND and OR; then you cannot do it directly with this. In fact, you have to attach a separate inverter at the output here to get AND, a separate inverter at the output here to get OR; either you do that or you give complementary inputs here; then the output will actually be A plus B in this case. If you gave A bar and B bar here; then apply to a NAND gate will give A plus B. Similarly, if you give A bar and B bar here; the output will be AB. So, there is no direct way to get basic logical AND and basic logical OR without using some inverters. So, this is something that I alluded to earlier; I mentioned in one of the earlier videos that, NAND and NOR actually have lesser transistor count than AND and OR.

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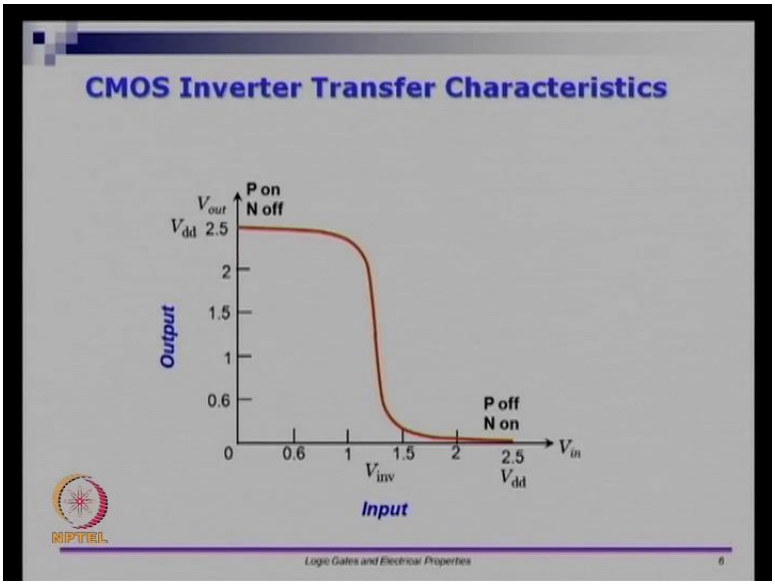

Now, let us see the transfer characteristics of a CMOS inverter. So, transfer characteristics capture the input to output relationship. We will see how the output behaves with respect to input. So, if I have an input, which can change from 0 to V dd; so I can take all possible values from 0 to V dd for the input; I want to see what will be the value of the output. And ideally, you want a CMOS transistor to behave like this. So, when the input is 0; when you have V in equals 0; then we know that, the PMOS transistor is on and the NMOS transistor is off. You want a voltage, which is equivalent

to v dd. Equivalently, when the input voltage is 1; the PMOS transistor will turn off and the NMOS transistor will turn on and you would want a voltage level, that is, 0; which means inversion of V dd should be 0; inversion of 1 should be 0. So, a typical transfer characteristic would look like this. So, you want for a large range, you want this input. So, for a large range of the input, you want the output to be 2.5.

Similarly, for a large range of the input from let us say middle of V dd to V dd. So, let us say V dd by 2 to V dd, you want the device to act as though it is a… You want the NMOS to be on and PMOS to be off and thereby inverting logic 1. And what you want is typically you want to sharp drop from V dd to ground if you change from let us say something slightly less than V dd by 2 to something slightly greater than V dd by 2. Ideally, you want that; however, in reality, you would usually get something like this. A transfer characteristic shows that, V dd actually slowly dips; the output voltage slowly dips; and then at some point, it sharply drops to something which is equivalent to a logic 0. So, at this place, you have something equivalent to a logic 1; at this place, you have something equivalent to a logic 0. However, if you give an input voltage, which is equivalent to let us say V dd by 2; then you would see that, the output is also somewhere in the middle; it is neither logic 0 nor logic 1. Ideally, you do not operate at this point. At least digital circuit – you operate either here or you operate here. So, let us see the definitions of various relevant definitions here.

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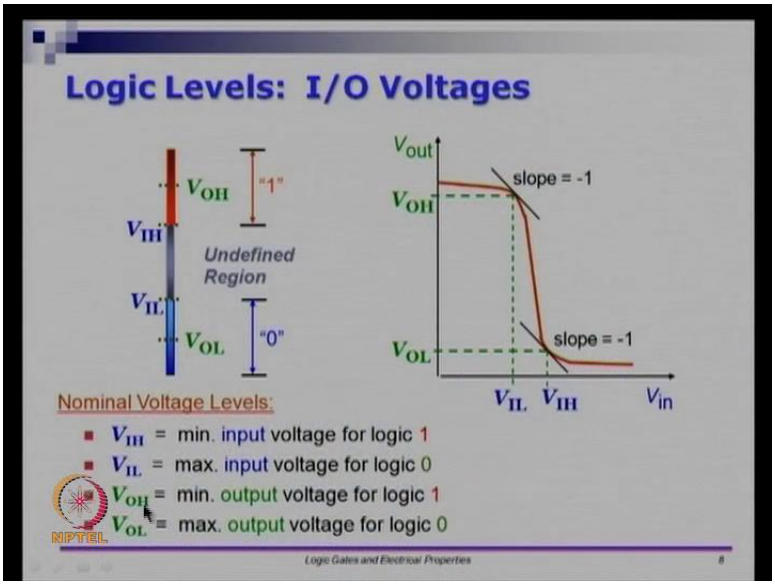

So, we are going to have a four voltage levels that I want to explicitly identify; they are V IH, V IL, V OH and V OL. So, these are not 1 and 0; these are V IH and V IL, and V

OH and V OL. So, V IH is the minimum input voltage for logic 1. So, if I am going to give 1 to a circuit; then I have to give at least some input voltage to be recognized for this voltage level to be recognized as a 1. That is called V IH. And similarly, V IL is defined as the maximum input voltage for logic 0. Say if I am going to give some input to a logic circuit and if I want the input to be interpreted as 0; I should not exceed a certain voltage level. So, V IL is maximum input voltage for logic 0. Equivalently, V OH and V OL are for the outputs. So, V OH is the smallest output voltage that can be guaranteed, so that it can still be interpreted as 1 by the following circuitry. And V OL is the maximum output voltage that you will drive from a circuit that can still be treated as 0 by the circuit that follows. So, remember – V IH, V IL, V OH, V OL are actually defined with respect to either the input side or the output side. So, you are looking at a gate; but you are not looking at an isolation. This gate is going to derive inputs from some other input circuitry and they are going to drive to some other output. So, the gate is going to drive some other gates.

So, if we go and look at it; then we are looking at the relationship between the input and output wave forms. We are looking at what should be the constraints on the input voltage and the output voltage, so that if I say that, this is an inverter; I actually want to interpret the voltage levels as though they are 0's and 1's. Similarly, if I have a NAND gate; I want to see if I give 0 0 as input. What is the safe level at which I can give 0 0; and beyond which, I may actually start thinking about it as 0 1 or 1 0 or 1 1 combination. So, these are four voltage levels that I want to define.

And typically, what happens is if you have an input beyond a range, it V IH; beyond the range below V IL, it is considered 0; and above V IH is considered 1. If these two happen to be the same; then you have a nice separation between logic 1 and logic 0. But, invariably, you will have a separation between V IH and V IL; which means if you operate the device within input voltage that is anywhere in between; then it is neither interpreted as 1 nor interpreted as 0. So, you have a problem. So, ideally, we usually do not operate within this region. So, V IH and V IL – usually, there is a gap between these and you do not want to give us input, which is somewhere in between these two. Either you want to be clear – clearly give something above V IH or give something below V IL to be treated as 1 and 0 respectively.

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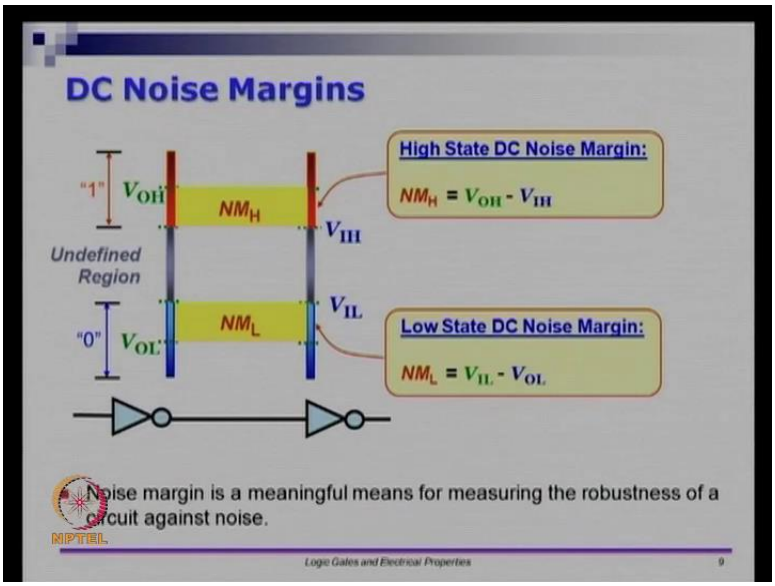

So, now let me define something called a noise margin. So, there are two noise margins: one noise margin is called the high state DC noise margin and the other one is called the low state DC noise margin. So, the high state noise margin is defined as V OH minus V IH. And the low state noise margin is V IL minus V OL. So, be careful about the relationships; it is V O minus V I here for high and V I minus V O for low. So, now, let us see why this is interesting. So, if I have a noise margin that is very high; let us say NM H is high; what that means is first of all, let us assume that it is positive. If it is positive, then V OH is above V IH. So, something like this.

And if NM H is wide; let us say this is yellow band that you see is wider; then what that means is it is able to tolerate even a poor 1 coming in as input; but its output is going to be a clear 1; the gates – if I have a circuit like this; then higher the noise margin for H; then it can take relatively weak 1 so to say; and it can still drive a very strong 1 at the output. Similarly, if this noise margin is high; then even a noisy input – even a relatively very high value of V IL could potentially get treated as a 0 and the output of the gate will still be a clear and nice 0. So, higher the noise margins, a better the device is. If this V OH gets closer and closer to V IH; then weak 1 is taken as input and in turn it will also drive a weak 1. So, this is something that is usually undesirable. What we want is we want to design circuits, so that the DC noise margins are quite high.

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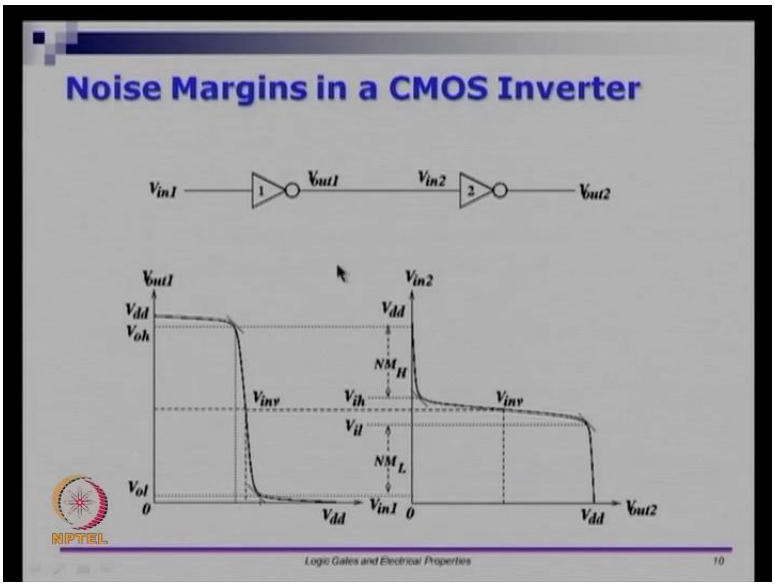

So, let us see this circuit here. We have two inverters, which are connected back to back. And V in 1 versus V out 1 is an inverted relationship. Similarly, V out 1 to V out 2 is an inverted relationship. V in 1 to V out 2 is actually just a buffer. But, let us assume that, there are two inverters; the logical relationship between V out 2 and V in 1 is that, V out 2 should follow V in 1 as it is. So, let us see the transfer characteristics of V out 1 with respect to V in 1. So, we have V out 1 in the y-axis here and V in 1 in the x-axis here. So, the transfer characteristics I already said would resemble something like this. So, this kind of wave form is just pictorial; but this is what you would get a few designer circuits nicely; you would get something like this. So, let us see what is the implication on the other side. So, you get a voltage from here. And the transfer characteristic here has just flipped around. So, what we have is we have input in the y-axis and output in the x-axis for the second inverter. So, there is a reason why it is done; I will quickly come to that.

So, let us apply a small voltage level – voltage at input here. Let us assume that, V in 1 is something very, very small. If V in 1 is very, very small; then V out 1 will be very close to V dd; you can see that here. If I apply something here; then V out will be very close to V dd. And if I apply that as the input to this circuit; that is the reason why we flipped it around. A very large value of V in 2 will again result in a very small value of V out 2. So, as small value of V in 1 results in a large voltage level at V out 1; that in turn will result in a small voltage level at V out 2. So, 0 gets buffered as 0 itself. So, let us follow this line here. Let us follow this line. So, let us say I give you this voltage level as input. So, it is still going to be considered as a logic 0. So, if I get logic 0 as an input; then the first

inverter gives logic 1 as an output; that in turn will get logic 0 as the output of the inverter 2. If I give somewhere in the middle; let us see what happens. So, if I give an input that is very close to V dd by 2; then the output of inverter 1 will be somewhere very close to the middle; that will be V dd by 2. That in turn when you apply to the second inverter; you have V dd by 2 applied input as input; it will in turn give you V dd by 2 as the output.

So, if I have very low noise margins; what would happen is – if you operate in the middle range; the output is going to stay in the middle range itself. If you have a fairly high noise margin; then what would happen is good, even a weak input that is coming in will eventually get translated as a good output here. So, buffers are usually used, so that you can boost up the voltage levels if it is a logic 1 or boost it down if it is logic 0, so that you get a clean 1 or 0. So, this is an example of a CMOS inverter connected back to back. And you can see that, higher the noise margin – higher the difference between… Let us assume… So, let us look at the noise margin only of this transistor. Higher the noise margin here; then you will have more cleaner output – V out 2 than otherwise.

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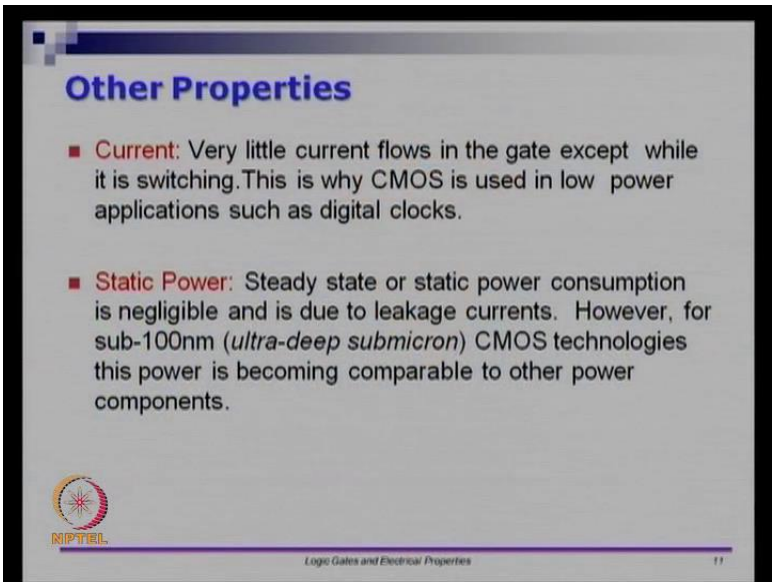

There are several other properties, which are interesting for a circuit. First thing is current. So, in a CMOS device, actually, very little current flows in the gate except when it is switching. So, once the gate has switched; then the output will actually remain in a Kaisen state. So, this is true of any nicely designed CMOS device.

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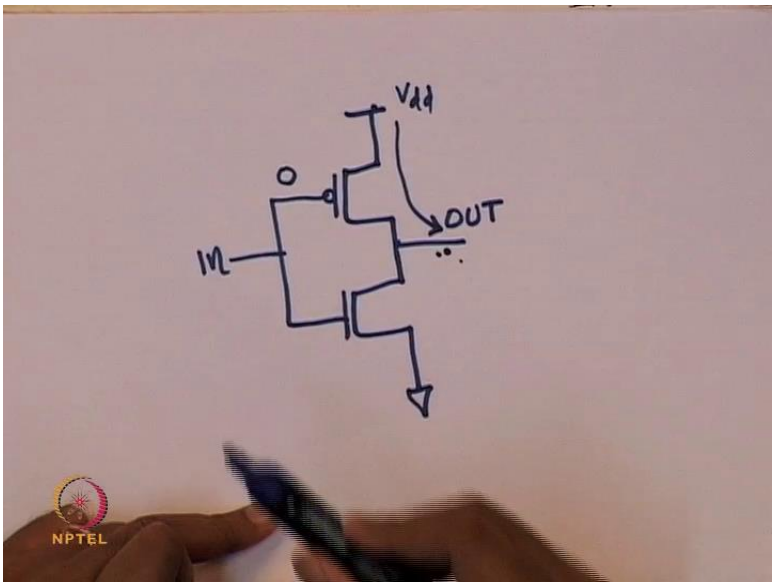

So, for example, let us look at the picture here. So, let us say I did an inverter. So, in the inverter, I gave input here and the output would be here. So, if I gave logic 0 here; then this device is turned on. So, this is that V dd and this is whatever it is; this will charge. Eventually, when this is completely charged; turning the gate on here is not going to change anything here. So, whatever you have V dd as here, the potential difference between this terminal namely, the source terminal and the drain terminal; once the potential difference is 0, there will be no more conduction. So, if there is no more conduction; then there is no electron or hole that is going to be passing here. If there is no transfer of electrons; then you do not have any current. So, this is what I meant when I… So, let us get back to the slide. So, very little current flows in the gate except when the input is switching. So, if the input remains constant; then the output will switch from 1 to 0 or 0 to 1; and after that, it will remain at that point. So, this is why CMOS is used in low power applications such as digital clocks and so on.

Then, there is another interesting electrical parameter called static power or the power dissipation. So, this is something that I talked about in the very first week – power consumptions of a circuit. So, steady state or static power consumption is also usually negligible in CMOS devices. So, what is happening is in the older CMOS devices, static power used to be very very low; in the current technology, static power is also very high. So, what that means is even when the device is not switching; there is something called static power consumption; it is not negligible anymore. It used to be true in the older technologies; nowadays, even if you do not operate the circuit; then there is some current

that is leaking; this is called leakage current; and because of which, the device will discharge. So, this is the reason why even if you keep your cell phone; let us say you cut off, you put it in aero plane mode; you do not want to operate anything and you do not operate it for a few days; eventually, the phone will discharge. So, that is because there is some power consumption that is there in the device even if you do not operate the device at all. That is called static power.

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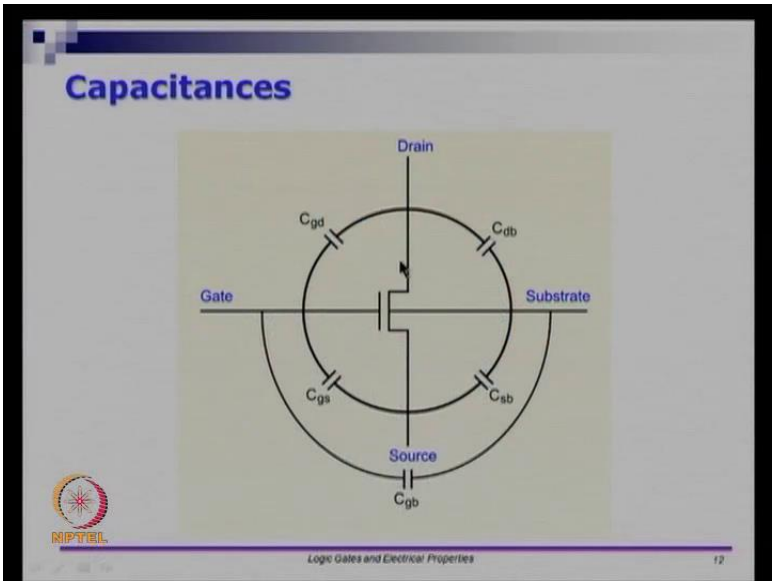

Then, let us look at the device itself; if I look at a transistor. Let us say I look at a transistor. We have three terminals: drain, source and gate. There is also an implicit terminal called the substrate, which you do not operate usually in a CMOS device. And because these are made of different devices and the way they are constructed; there are capacitances between each of these terminals. So, between drain and gate, there is a gate to drain capacitance; between the drain and substrate, there is drain to substrate capacitance. Between the gate and source, there is a gate to source capacitance. Similarly, between the source and substrate, there is a source to substrate capacitance. And finally, between the gate and substrate, there is something called a gate to substrate capacitance. So, all these are capacitances that are built up because of the way the devices are manufactured.

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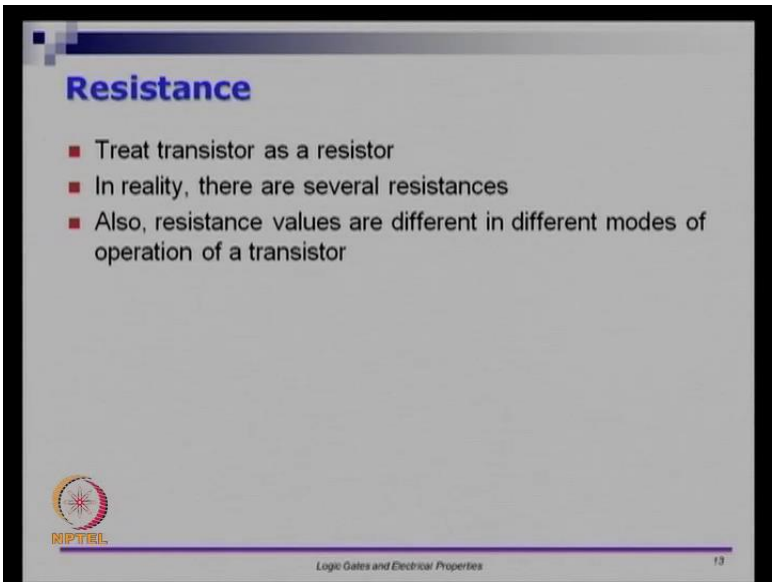

And every transistor also has an equivalent resistance. So, you can treat the transistor as a resistance – a resistor. And in reality, there are several such resistances. And in different modes of operations, there are actually different resistances. So, again without getting into too many details about what the actual values of the resistances and so on are; you can treat conducting transistor as though it is a resistor and a capacitor. If it is a non-conducting transistor; the conditions for the transistor are keeping it open; then you can treat it as a resistance, which is very very high. So, this is one way to think about a transistor. So, when the device is conducting; so let us say I take a PMOS device; if I put gate equals to 0; then the device should be conducting. So, I will assume… So, at that point, I have some value of resistance; however, if the gate input to a PMOS device is 1; it is supposed to be non-conducing; I can think about a device having a very very large resistance at that point. So, now we have resistances and capacitances. So, because of these, we have various other electrical properties.

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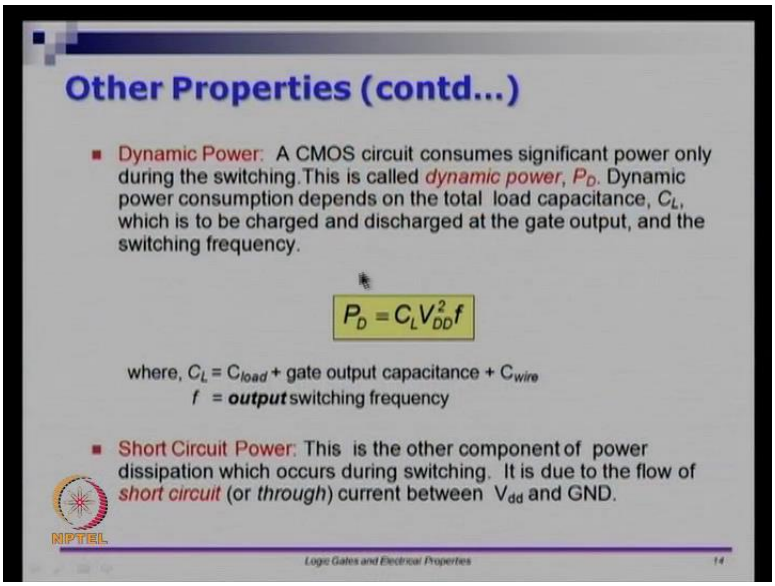

So, there is a notion of dynamic power; dynamic power is the power consumed because of gates, which are switching. So, dynamic power is usually expressed by this expression here. So, dynamic power is proportional to the capacitance that is at the load. So, from a gate, if you are driving another gate; the second gate is called the load to the first gate. So, we have the drive. So, we have the capacitance of the load; and it is also proportional to the square of the voltage supply and it is also proportional to the output switching frequency. So, dynamic power… So, we do not have to worry about these details right now. So, P D is C L into V DD square into f. And finally, there is something called short circuit power; this happens just at the moment of switching. So, this happens because there is a path from V DD to ground. Again, let us not worry about all these details right now.

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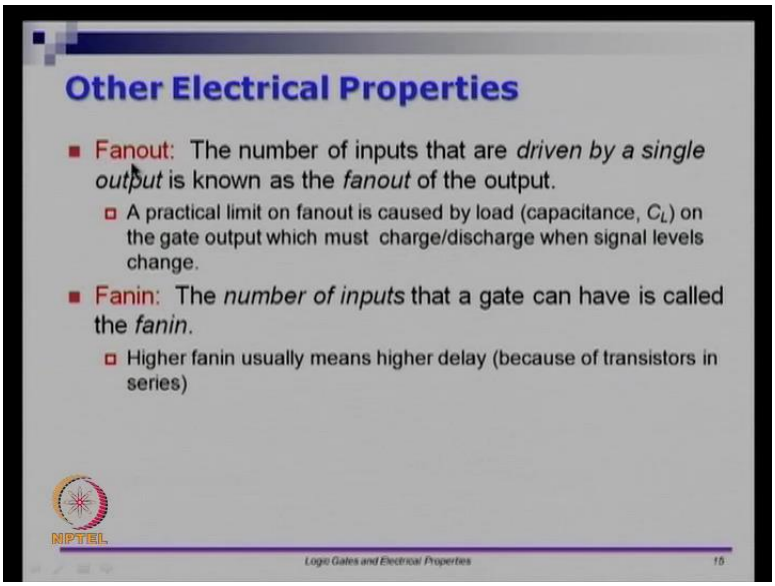

But there are different components of power. These are all electrical parameters. Then, there are two other electrical parameters that are very useful. So, for example, there is something called fanout. So, fanout means the number of inputs that are driven by a single output. So, if I take a gate and connect it to two other gates; it is supposed to have a fanout of 2. Fanin is the number of inputs that a gate can have. So, for example, a two-input AND gate has a fanin of 2; and a three-input AND gate has a fanin of 3 and so on. Typically, what happens is higher fanin means the gates actually have higher delays. There are issues why the gates have higher delays. But, typically, higher fanin means higher delays. And in terms of fanout, you cannot arbitrarily design a circuit that can drive any load. So, the output capacitance or the output load controls how well a circuit behaves. So, these are various electrical properties.

So, we started with the basic properties of a CMOS device and we looked at an NMOS device, a PMOS device, a fully complementary MOS inverter, basics of NAND and NOR gate. And we looked at various electrical principles or electrical properties that are there for the circuits. So, what I want you to get is not really understand all these in all the detail, but you should appreciate that, these gates are electrical circuits. The electronic devices have some constraints and the abstraction that we have as logic 0 and logic 1 eventually translates to voltage levels in the device. And we are talking about devices that are semi conducting devices. So, they turn on under appropriate conditions and they act as insulators under appropriate conditions. So, given all these things, I suggest that, you go and look at the video once more just to get a basic understanding of

how CMOS devices work, because we will need some of this understanding for the following lectures. So, this brings me to the end of module 23. And in module 24, all the basic concepts that I talked about here, that the notion of resistances and capacitances and so on; we will use that to look at the notion of delays.

So, thank you and I will see you back in a little while.