Digital Circuits and Systems
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Module - 20
Flipflops

Hi, Welcome back to this week's lecture and we are at module 20. So, I did suggest that you should review the materiel in modules 18 and 19, before you go to 20. Because, 20 gets a bit intensive, unless you understand materials from 18 and 19 all together, you will have a bit of difficulty in understanding 20. So, the some of the concepts that you needed in the fact that, the cross couple circuit gives you memory element and there is S and R which can change independently and the basic S R latch.

Then we slapped on gating to it and we said only when the gate signal is on, the S R latch will behave like an S R latch, if the gate signal is off, it will keep the values as it is. This still did not prevent, S and R being change simultaneously. So, we introduce a notion of what is called a gated D latch. In the gated D latch, we prohibit S and R from taking the same values, but connecting them to the same input line, one with the complemented version and another with the uncomplemented version.

So, you have to understand all of that, and finally we also said latches are what are called level sensitive circuits. The changes in the output, there may be changes in the input and this will reflect as changes in the outputs as long as the gate is turned on, as long as the enable of the latches turned on. So, we need to be able to control that and that brings us to this module which is on flip flops.

So, the word flips flop itself, it is a funny word, so flip flop also means slippers for instants. In this case, this case flip flop actually means the values can go from 0 to 1 and 1 to 2, so that is why, it is called a flip and a flop, so it can flip or it can flop. So, the flip flop is essentially a memory element, again it is just a Bistable multi vibrator.

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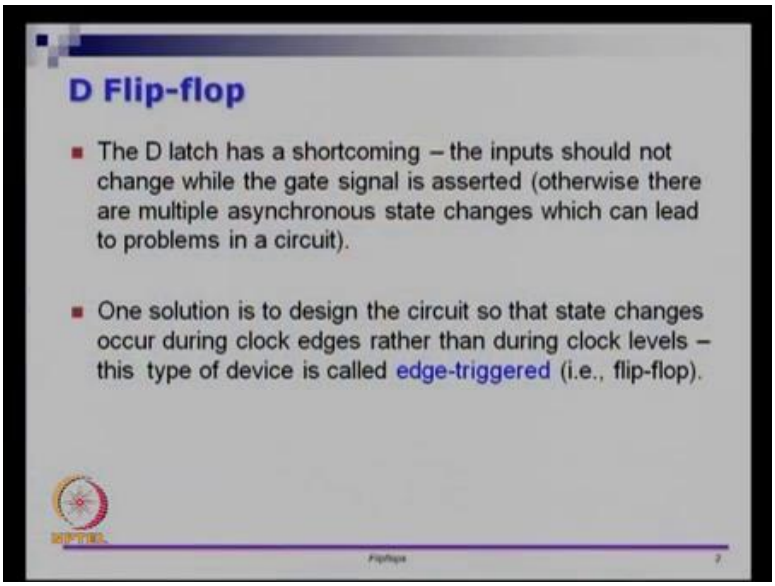

The first thing we will start with is, what is called D flip flop. So, we saw that the D latch has a short coming, the input should not change, while the gate signal is asserted. So, otherwise, what can happen is, there are multiple events which can change and you may not have a reference point with respect to the clock for that. So, once the enable signal comes in, we do not want changes in D to go to Q, if you want anything like that, then if you want to prohibit changes in D to go to Q, then the latches not enough.

Instead, we will design a circuit, which will ensure that Q will change only doing the clock edges rather than during the clock levels. So, instead of latch which is changing Q, when as long as the latch is enable will ensure that Q in a flip flop will change only when the clock comes in. At the time of the clock, if there is anything in D, we will capture that, any further changes in D will not be captured, till the next clock comes in. So, this is called a D flip flop. So, the symbol for a D flip flop is as follows.

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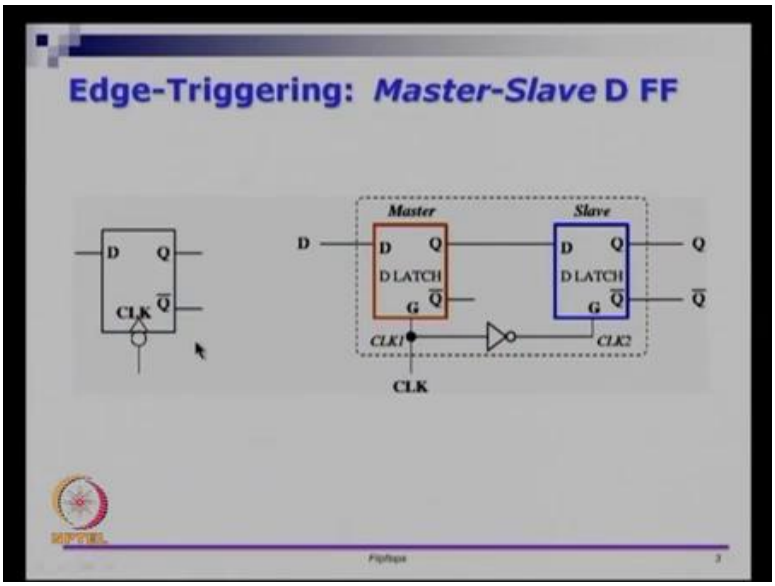

We will see how these circuits come about and so on in one step after the other. The first thing is the symbol for a flip flop is usually drawn as a rectangle like this and D input and there is Q and Q bar. And in a latch, we actually had just a single line coming in and we called it Clk. Now, we also have a small traingle kind of thing here. So, forget the bubble for a while now, we also have a triangle kind of a thing, that is indicating that, it is a flip flop.

So, this triangle here not the bubble. So, the triangle here indicates that it is a flip flop. So, you look at a rectangle with an input here 2 outputs here Q and Q bar and a triangle like this, that is a flip flop. If it does not have a triangle, it is a latch usually and this bubble is something extra. So, this bubble is equivalent to inversion, we will come to that in a little while.

So, the first circiut that we are going to look at is called a Master-Slave D flip flop. So, what is a D latch? A D latch has D as a data input, Q follows data input as long as enable is on; that is what a D latch was. A D flip flop is going to have two latches connected back to back. So, you have something called a Master latch, which is in red and you have another latch called the Slave latch which is in blue, these are your basic D latches.

So, we have two of the D latches, put them back to back and we take the external input D connected to the Master's D input. We take the Masters Q or the output of the Master's latch connected as input to the Slave latch and the output of the Slave latch goes to the external world. So, infact the Slave has 2 outputs Q and Q bar, you tap those two, you get

Q and Q bar for the external world.

The Q bar of the Master latch is not conneted to anything and from the external world point of view, it takes an input Clk and D, there is D and there is Clk and there are 2 outputs Q and Q bar, so you have 2 outputs Q and Q bar. So, the most important thing that we have done is, you have taken Clk, we have given to one of the enables, we have given it directly, we will call that Clk 1, to the other latch the enable is negation of this Clk. So, Clk 2 is a negation of Clk and Clk 1 is Clk directly.

So, in some sense, when if this latch is enabled, this latch is disabled, if this latch is enabled, this Slave latch is disabled. So, at any point of time, there is only one latch which is enabled, the other latch is disabled. So, the first thing, I want you to see is this fact, that since G is the enable for this, when Clk is on, Master will be enabled, Slave will be disabled and when Clk is 0, Master will be disabled and Slave will be enabled.

So, when we say enable and disable, what we mean is, if Clk is on, then any changes in D can go to Q. However, because Clk 2 will be off, changes in Q will not be propogated to this Slave Q. Similarly, if Clk is 0, then any changes in D here will not reflect as changes in Master's Q. But, if there is anything in Master's Q, it will go to Slave's Q. So, this is what the whole circiut is doing.

The best way to think about that is, think of it as a balck box first, it is taking 2 inputs, it is giving 2 outputs and there is some intersting internal connections of the latches that we have done, so to get you the D flip flop. So, this is called a Master-Slave D flip flop. Specifically, the circiut becomes what is called a edge trigger circiut. So, this circiut is not level triggered anymore, so it is not that at a particular level of the clock, D gets coiped to Q.

So, once you connected like this with respect to this Clk, this D cannot be asynchronously copy to Q, which means the change in D can reflect as change in Q, only at very specific time intervals, not any time that D desires to. So, there is also this bubles here, we will come to that in a little while.

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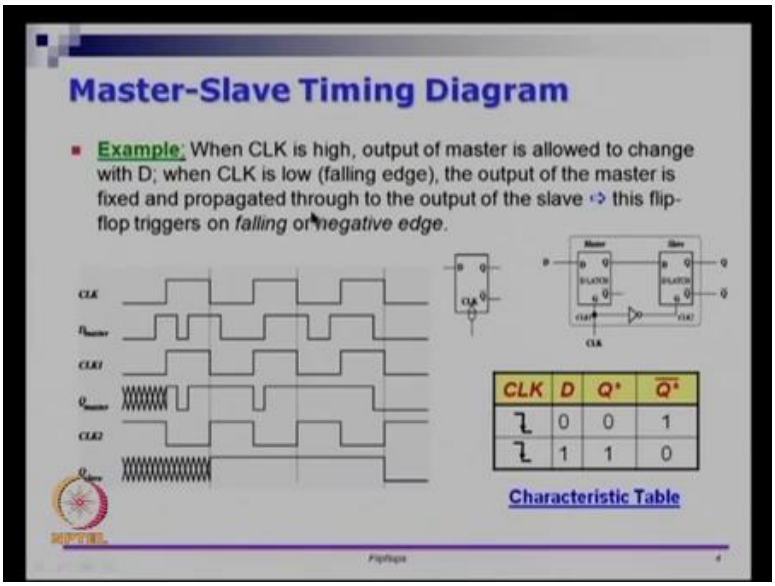

So, let us see a quick timing diagram. What you are seeing is, you are seeing the same circuit here and the symbol for that circiut is here. So, I also put the bubble here, because the bubble is necessary and let us see, how the circiut will work. So, I am assuming that Clk is a periodic signal, so that is coming an on and off at some regular intervals. So, let us assume that this is some time line, this is some time line and so on.

So, between this line and this line, vertical line here, that is 1 time period, between this line and this line, it is another time period and what not. So, Clk is something periodic and that is coming from the external world and D is also an external input. From the circiuts point of view, you look at this as a black box, D is an external input, let us assume that D is changing whenever it is wants to.

So, the change in D is not with respect to the clock signal, D is an external input, it is changing whenever it is changing. Now, let us see the effect of this, the changes in D and see what happens and what gets resisgtered in the Q. So, Q of the Slave is going as Q of the circuit, we will observe, what is happening to the Q of the Slave. So, let us start with this point.

So, there is one edge coming here, when clock comes on, see at this point, if you look at here, the clock is on, so there is positive level here. So, whenever Clk is 1, Clk 1 is also 1, so this is 1. So, all changes in D, which is coming in to the Master will go as Q of the Master. So, even if I do not know, what is happening before the clock, so this hatching kind of thing that you see there is something that indicates, I do not know what the value

of D is or I do not care about, what the value of D is.

Let us see from this point onwards what happens. The clock came on, once the clock comes on, the Clk 1 is the same as Clk itself. So, this is the clock for the Master and this is the data for the Master. Now, let us see, how the Q of the Master will change with respect to D of the Master. So, as long as clock is on, you will see a copy of D coming on to Q.

So, we do not know what is happening till this time point and after that, it is 1, you will see a 1, then it is go to 0 for sometime, so it is go to 0, then come backs to 1. So, that is what happens here and between this and this, Clk 1 is off. So, because Clk 1 is off, this change in D will not change the Q Master. So, if you see the clock Clk 1 here of the Master, this is off which means the Master latch is disabled, if the Master latch is disabled, then change in D will not change the Q of the Master.

So, Q of the Master is remaining stable, finally again this Clk comes on, which means Clk 1 also comes on. So, when Clk comes on, so at the positive level, it starts with a 0 goes to 1, stays 1 till the clock is on. So, you will see that happening in Q also. It goes to 0, because when Clk 1 came in, D Master is 0, it starts with that and then it goes to 1 at some point stays at 1, till the clock goes off.

So, when Clk is goes off, again there are changes here, it changes form 1 to 0 to 1, however, those changes are not seen in Q of the Master. And finally, when this signal comes on, when the third clocting comes on, at that point, D Master is already 1, it goes down to 0 once, that is captured in Q Master. So, if you notice, what is happened is, we just traced, what is the relationship between external clock D Master and Q Master.

So, if you look compare D Master and Q Master, you can see that not all the transactions in D Master are transfered to Q Master. So, a subset of the transitions are actually left out. So, for example, this 1 to 0 transition does not appear in Q Master. Similarly, this 1 to 0 and 0 to 1 transition does not appear in Q Master. So, some transitions are captured, some are not, but Master is still a latch.

So, whenever Clk 1 is on, if there are changes in D, that will be captured in Q Master. So, now, let us look at the connection between Q Master and D Slave. So, with respect to the Slave, the clock signal is Clk 2, so Clk 2 is the complement of Clk. So, you can see this wave form Clk here and the wave form Clk 1 here, they are the complement of each other.

So, when Clk is 0, Clk 2 will be 1 and Clk is 1, Clk 2 will be 0, so we have a complement of each other. Now, Q Master is the same as the D Slave, so this is the same as the D Slave, let us see, what happens to Q Slave with respect to Q Master. So, now, when is this latch going to be on? Whenever Clk 2 is on, so let us go and look at when Clk 2 is on.

So, Clk 2 is on at this point of time, so it is on here. So, whatever is in Q you copy to D, the Clk 2 is on here, at this point Q Master is 1. So, we do not worry about, what is happening here, for now, because this is the time, when Clk 2 is on. So, we know all the data input as well as… So, here the data is not known, the clock 1 came on, so we do not care about this and Clk 2 is off, so we do not care about Q of the Slave here.

So, once we come pass this point, this Q Master is 1; however, Clk 2 is 1. So, when Clk 2 is 1, Q of the Slave should copy D of the Slave or the Q Master, so which is 1. And at this point, Clk 2 goes off, when it goes off, it seems to be a transition on Q Master to 0 and then back to 1, but that is not even seen by the latch, the Slave latch, because the Slave latch is disable at this point. Then, the Slave latch gets enabled again here.

So, when the Slave latch gets enabled here, we see that Q was already 1. So, it copies that, when the Slave latch is disabled, what are value was there in the Slave before the clock went off, that is continued. So, it was at 1 just before the clock went off, clock Clk 2 went off, so it will continued in that value. Finally, again at this point, Clk 2 comes back on, at this point; Q Master is 0, so you copy Q Master to Q Slave.

So, now, if you are look at Q Slave, Q Slave has for few a transitions than D Master. So, if you look at the output of this whole circiut, the Q was the D relationship, Q has for few a transition than D. This few a transitions is not the goal here; however, there is something else that is happened interstingly. So, now, I am going to make a claim and we will verify that with the picture.

The claim I am goin to make is that, this circiut that I did here is overall black box, which I am going to call the D flip flop is going to sample D, only at the negative edges of the clock and it is going to keep the value every where else. So, let me restate it. So, my claim is that, this circuit here, this black box here which is called the D flip flop is going to sample or it is going to check, what the value of D is on the negative edge of Clk signal.

If on the negative edge of Clk if D of 0, it will copy that, if D is 1, it will copy that only

during the negative edge of the clock. Once, the negative edge happens of Clk signal, then Clk will remain at 0, Clk will come back to 1 and remain at 1 and then again go back to 0; that is the periodic nature of Clk. During all these periods, any change in D will not reflect as change in Q of the circiut, this is my claim. So, let us validate that.

So, let us go and look at Clk as a signal. So, I am going to look at Clk D Master and Q Slave, because that is the black boxes inputs and outputs. So, when Clk is 1, the change in input will not go to Q Slave. So, that is clear from the picture. When Clk goes off, whatever is the value of D, so what is the value of D, when the clock goes off, D Master is at 1, I am going to sample it. Just at one period of time, I am going to take, so just that one nick of time, when the clock is going from 1 to 0, I am going to observe the value of D, I will read in that as the value, till the next negative edge comes in.

So, I sampled 1 here, if I sampled D here, Clk is negative edge, if I sample D, it is 1, I am going to keep it till the next clock edge comes in. And during this time period, D actually went to 0, went back to 1 and so on, all of that, I do not care. So, essentially what I have done is, I have sampled D signal only at this time point and it is retaining it till the next clock edge comes in.

So, when the next falling edge of clock comes in, at this point again D is 1. So, if you observe at this point, it is again at 1 and I will keep that as the value and continue that keeping that value at Q, till the next clock edge, which is falling which comes through. When, that happens D is 0 and when D is 0, Q of the Slave is 0. You can see that Q Slave or Q of the D flip flop is actually following D Master or D of the flip flop. Only that it is not following the signal wave form blindly, it sampling D Master at whenever there is a negative edge.

So, this clock in some sense is our triggering signal and at this triggering signal, we are going to come and capture the values. So, the analogy that I can give is, let us say I want to take attendence in class and I have a camera, which is setup in the class and I will some algorithm, which will figure out the faces and figure out, who is in the class and who is not in.

Let us say, I have all of that, what I am going to do is, at 8:50, I will take the picture of the class, who ever the class at that point of time, they get attendence. So, I sample it and who ever in the class at 9:50, they get attendence. So, it is possible that people walked in at different points of time, starting at 9 o clock till whatever time it is. But, at 9:50, if

they are in there class, I am going to treat that, they were in the whole class and I will give them attendence.

Let us say I do that, then all I am doing is contineously monitoring, who is in the class from 9 o clock to 9:50, I am just going to take a snap shot of at 9:50, I will treat that as my data, thus the same thing that is happening here. On the negative edge of the clock whatever is in D, I am going to copy that and all the rest of the time till the next negative edge comes in, I am going to care about D.

So, let us look at the characteristics table. So, this is Clk signal, we are showing it has a down word going arrow, so that means, it is a negative edge. So, on the negative edge of Clk, if D is 0, Q should be 0 and Q bar should be 1. On the negative edge of the Clk, if D is 1, Q star is 1 and Q star bar is 0. In all the other cases Q, Q star should just keep the value previous value itself.

So, Q of t should be the same as Q of t minus 1, so this is called a negative edge triggers flip flop. So, the reason it is called negative edge trigger is that, the sampling of D is done at the negative edge of the clock. If I do sampling at the positive edge of the clock that would be called a positive edge triggers flip flop. So, now, let us go back to this picture here ((Refer Time: 22:18)) that I showed.

So, in this picture, what we have is, I put a bubble here. So, a positive edge trigger flip flop which samples value of D, only when the clock it raises; that is called positive edge trigger flip flop. That will not have this bubble, when you see a bubble; it means that, it is a negative edge triggers flip flop. So, if we see a rectangle with three opens for D, Q and Q bar and just a triangle like thing; that is a positive edge flip flop.

In this flip flop, in the positive edge flip flop D is being sampled only when the clock rises. In a negative edge flip flops D is sample when the Clk signal false. So, once you do this, this is Clk 1, Clk 2 and so on, does not matter. You can now think about this is whole circuit; this is D flip flop as a block box. What is the block box give you, whenever Clk comes from 1 to 0, D will be sample. In all the other time periods, Q will be retain that is the characteristics table of a flip flop.

A D flip flop, which negative edge trigger and it is still following D. So, that is why we call it a D flip flop on the data flip flop, it still following D as it is. This most special meaning attach to D here, D is not set or reset are anything, whatever the value of D is your passing that on to Q's. So, it is just the data input; only that we can now forget the

fact that is actually made two flip flops and there is some careful connection inside and so on.

We can now go up in one level of abstraction and we can start using this circuit as a D flip flop as it is. So, I will treat it as a block box, I will not show the connections later on. Only, I need it I will show it till than I will assume that D flip flop is just this external block box, I will assume that you understand what the internal details are all. So, now, we have something called a D flip flops, there are lots of interesting think that you can do with the D flip flop. So, I want to show quick summary of what this level verses edge triggering means.

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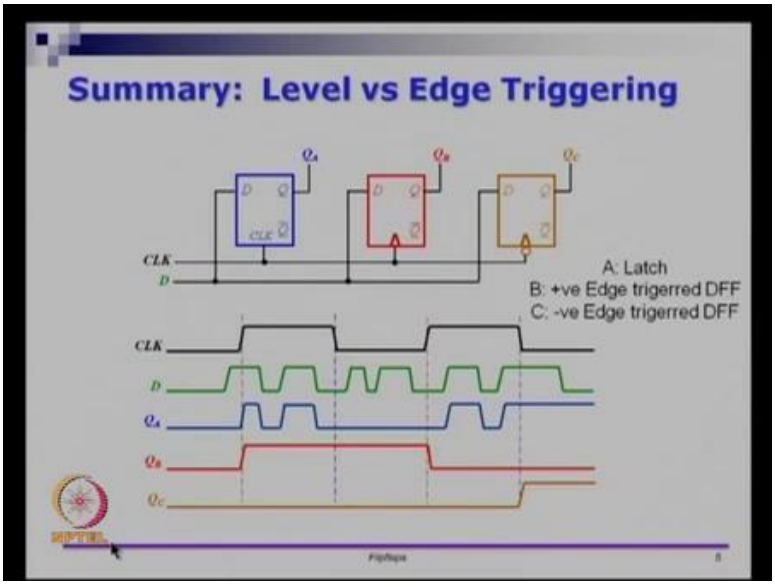

So, in this circuit, I have three difference logic elements sequential elements on the left side, you have a latch. So, latch is just D, Q and Q bar and an enables signal that comes in. And in the middle is the red one which is actually a positive edge trigger D flip flop. So, this flip flop will capture D, whenever the clock signal goes from 0 to 1, otherwise it will ignore the changes in D, it keep the values of Q and this brown one is the negative edge trigger D flip flop.

So, you have three logical elements all are memory elements, this is the latch, this is the positive edge triggers flip flop, this is the negative edge triggers flip flop. What is if give the same D and clock to all of them, what it be they behavior on Q a, Q b and Q c. So, this is not a circuit that is usual for any practical purpose, this is just a show you, how this circuit behave. So, let us assume that clock and D are as follows.

So, there is clock and you have this here and D changes several times in no matter where clock is, D is changing asynchronously with respective to Clk. What I mean by that is, the changes in D are not align which changes in Clk. So, it is changing independently of Clk. So, C is asynchronously with respective Clk, I know what synchronously D with respective Clk.

Now, let see what happens for the blue latch first. So, Q a is the output of the blue latch and it is a positive level trigged latch which means when Clk is 1, D will be copied to Q a and then Clk is 0, whatever the value of Q a is it will continue. So, let see this part first. So, during this part Clk is 1, whatever you will see a change in green till here is appearing in the blue way form.

But, once the clock goes off, there are changes in the green way form here which are not reflected here. So, at this point Q a is 0, it just continuing here, again when the clock comes on here, it will Q a should start following D. So, in this part is actually Q a following D, but Q a is also 0 earlier, so we do not see any transition here. But, the transition to 1 and back to 0 and 1 are capture and this transition from 1 to 0 is not capture, because at that point Clk is off. So, the latch is disable.

So, this is what happens for the latch, let us look at the positive edge triggers flip flop. So, remember there are two latches inside the Master and the Slave latch. So, in the Master in the Slave latch, so if I go and use this abstract thing, whenever there is a positive edge I will sample D and I will keep it till the next raising edge caps. So, there is a rising edge here, when this edge is raising, D is already 1. So, I am sampling 1, I will keep it till the next clock raising edge comes in when that comes in D is 0. So, I am going to keep that 0. So, this is what happens for Q b.

Q c is actually is the output of a negative edge trigger flip flop, what this is going to do is, it is going to look at whatever is D, when it is falling, when the clock is falling. So, when the clock is falling, the D input is 0, so it keeps 0. The next clock signal falling is here at that point, this is 1 is good raises to 1. So, Q b and Q c are themselves different and Q a is of course, different from Q b.

In fact Q a and the Master latch of both these two, the Q a and the Master latch of this red flip flop will have the same way forms. However, Q b is tap from the Slave latch of the D flip flop, so that is having a different way forms. And there is no direct relationship between the way form Q a and Q c, even internal signals of this flip flop will not match

the signal of Q a. So, that is the overall set up.

Hopefully, this picture explained to you, what is the difference between latches and flip flops. So, now let us move on, so I am going to show you two different kinds of circuits.

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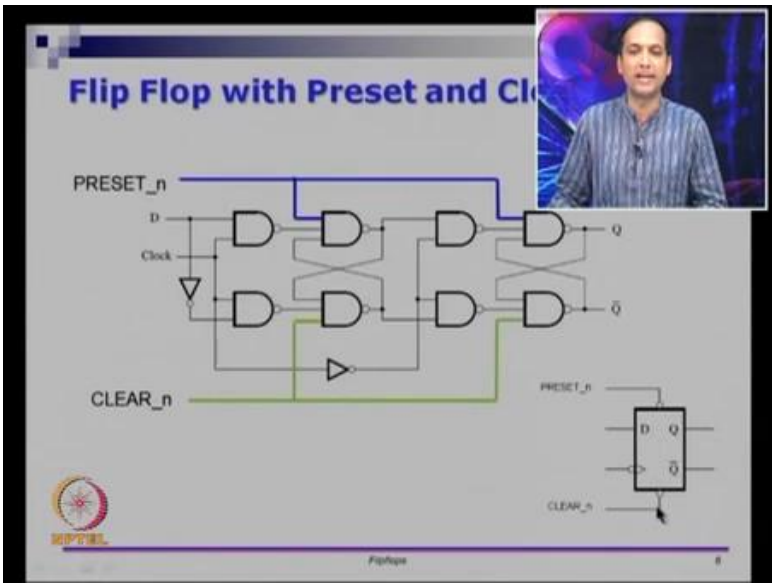

So, one of the circuits is what is called flip flop with the preset and clear. So, if you notice this part is the Slave latch and this part is the Master latch. So, forget the blue lines and the green lines now. So, this is the cross coupled S R latch and you put to gates before that and a common signal that is driving both. So, that would mean it is a gated S R latch.

So, this part is a gated S R latch, this part is also gated S R latch and before the gated S R latch, there is a common D; that is coming to both, so this part is a D latch. So, you have a D latch followed by gated S R latch here. On top of that, what we have done is, we have take in a signal call preset and we have given in to these two gates here, you have take an another signal call clear and we have given in to these two hates here.

So, the rest of it, will resemble the internal circuit for a D flip flop actually. If you go and look at it, if I remove the blue lines and if I make this, all these three input gates as 2 input gates; that is actually the internal circuit for a D flip flop implemented with NAND gates. On this flip flop, we made these four gates as 3 input AND gates and we are bringing a signal call preset here and we are bringing a signal call clear here. So, in fact this is a negative edge trigger D flip flop.

So, now, let see what the preset in clear does. So, the first think to notice is preset is not

just preset, it is marked with preset underscore n. So, what we are doing here is, what is call negative logic? So, first of all the word preset means, you want the flip flop to be one even without data input. So, this is not p reset, it is preset. So, whenever preset is on, so this is something that you do when the circuit actually comes up. You may not have any data input, you want the flip flop to have one at the output, there is no data input so far.

So, in those cases you want bring up preset. So, preset of one means the flip flop should be set to 1. When, you set preset underscore n, what we mean by that is, if this line preset n is 0, then Q should be 1, if preset n is 1, then the circuit should work as it is. Similarly, for clear, if clear is 1, Q should go to 0, if clear is 0, then the circuit would work as it is, that is the usual meaning of preset in clear.

Preset means said the value of the flip flop to 1 and clear means said the value of the flip flop to 0. Only, we put the underscore n means, we are using preset bar and clear bar. So, when preset bar is 0, it means preset is 1, we want the circuit to be preset. So, let us put a value 0 and the signal here, if I put 0, this is why are here, this 0 will go to this 3 input NAND gate will see a 1 here and the same input goes here Q will also become 1.

So, without actually looking at D or clock or anything we are able to change Q to 1 by just bringing this preset n line to 0 or preset bar to 0. So, if preset bar is 0, preset is 1, we want to circuit to be preset. Similarly, I can bring this clear n, if I bring iT is 0, no matter what D and clock are, this line will become a 1. So, if I bring this as a 0, this will be a 1, because of this NAND gate and this will be a 1, because of this NAND gate. And if Q bar is 1, Q will eventually go to 0. So, Q becomes 0, when clear becomes 1.

So, if preset is 1, Q becomes 1, if clear is 1 or clear n is 0, then Q becomes 0. So, this is the meaning of preset and clear. The only thing is both the preset and clear signals can actually be brought in without any reference to the clock itself. So, therefore, preset in clear in this circuit are actually asynchronous inputs. They can change no matter, whenever they want to, they do not actually have to align themselves with respect to the clock input.

However, D actually aligns itself is the clock input. So, if both preset and clear are off, the rest of the circuit is D flip flop and change in D will not go to Q, unless the clock signals samples it at the negative latch. So, this is called asynchronously resettable and presetable D flip flop. So, the symbol for that is follows, typically you put two different

symbol lines here and this bubbles are actually meaning that, they are negative logic.

So, if you do not have the bubbles, then if preset is 1, Q will become 1, if clear is 1, Q will become 0. So, clearly you can you do not want preset and clear both should be 1 at the same time, then there is no meaning attach toward. So, we will ensure somehow in the circuit; that are driving preset and clear, you do not drive both of them simultaneously in general.

Then, you have the clock input here which also since to be a negative edge trigger flip flop. So, this flip flop is a negative edge trigger D flip flop, which as asynchronous preset and asynchronous negative clear, so this the meaning of the logic plug.

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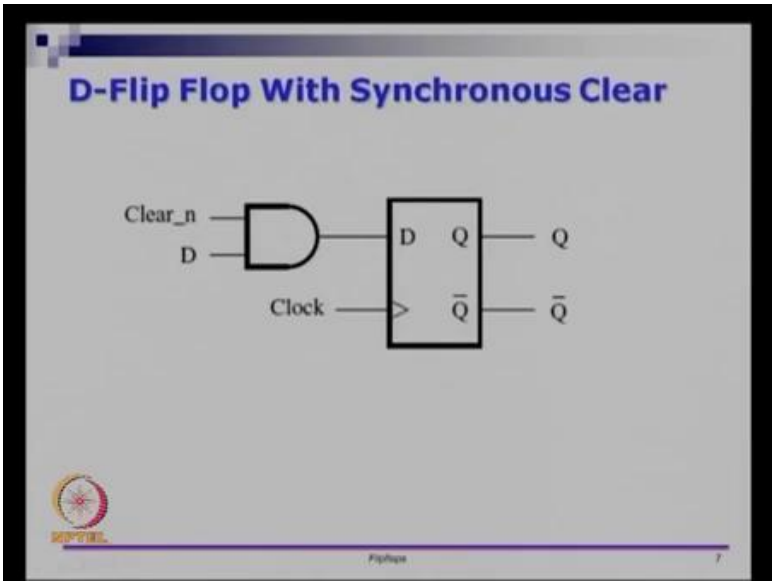

You can make the D flip flop with synchronous clear, you take the D input and put clear bar as another input to AND gate, you give that to a regular D flip flop. So, when you do that, if clear bar is 0, which means clear is 1. So, we want the Q b to be clear, if clear bar or clear n is 0, then this D input will be a 0. So, if the clock samples in correct, then Q will become 0, it does not, it completely masks the D value.

However, if clear bar is, if this is 1 or clear is 0, clear is 0 means, you do not want to clear the flip flop, if clear bar is 1, D will come us input here and that is passed on to Q, provided the flip flop catches it. So, what we have is a D flip flop with synchronous clear. So, change in clear will not change Q, unless there is a clock it that comes in samples clear also. So, D is a sample signal always for a flip flop, clear is also sampled in this example, whereas, in the previous example clear was not sample.

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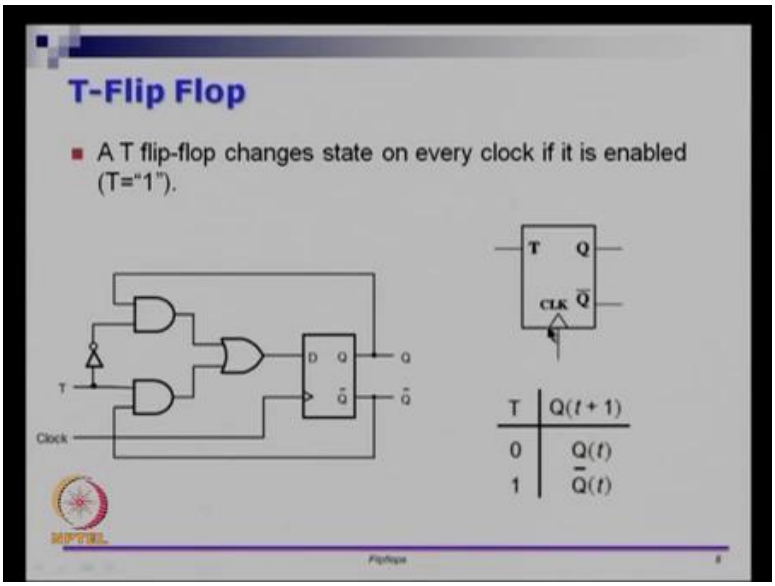

Then, let us look at a circuit called T flip flop, T flip flop is an interesting circuits. So, T flip flop is actually a minor variations of the D flip flop. So, let us look at the circuit, you have a D flip flop and there is some circuitry here, the circuitry is actually doing the function of a mux or a multiplexer. So, if you describe the output of this OR gate in terms of the inputs namely T, Q and Q bar, we can see that this OR gate is doing T bar and Q or T and Q bar.

So, that is the definition of a mux, where Q and Q bar are the input lines and T is the select line. So, if T is the select line, this circuit is actually a mux. So, this circuit is either choosing Q or Q bar, depending on what T is. So, if T is 1, then the flip flop will toggles it is current state. So, let me restate this, if T is on, then this circuit will toggles, it is output, if T is off will keep the previous value that it contain.

So, T flip flop or a toggles flip flop changes state on every clock, if the toggling is enable or if T is 1. So, let us put T equal to 1 for a while now, if T is 1, this is 0, which means, this lines will be a 0, if T is 1 and Q bar will come here. So, you have 0 or Q bar, 0 or Q bar is Q bar, Q bar both us D input. So, when the clock comes in, let say it is a positive edge trigger D flip flop.

So, when the clock comes in Q bar will be copied to Q. So, if Q was 1, Q bar would have been 0, so it will become 0. Now, if Q was 0, Q bar would have been 1, it will become 1 now either way Q toggles. However, if T is 0, then this is 1. So, you have 1 and Q that goes as Q and you have 0 and Q bar that goes as 0. So, you have Q or 0 that is Q. So, the

D input is Q, which is the previous state of the flip flop bit shape. So, the previous value was also Q.

So, when then when the flip flops rising at edge clock comes in, it takes the same value and copies it back to Q. So, in that that case when T is 1, this circuit toggles the value, if T is 0, the circuit does not talk. So, the characteristics table and the picture are shown below. So, if you mark the inside pin with T, it usually means it is a T flip flop. If you put a D, it is a D flip flop, if you put T, it is a T flip flop.

As before we are the small triangle here to say that the signal that is coming in is a first of all for a flip flop, this block is a flip flop. And the absence of bubble here says, it is a positive edge trigger T flip flop and you up to outputs Q and Q bar, the characteristics table is given here. When, T is 0, Q of t plus 1 is a same as Q of t, when T is 1 Q of t plus one is Q bar of T, this is the toggles flip flop. The toggles flip flop is quite handy, if you want to toggles some signal in every step.

So, this is the very nice and handy circuit to have and this brings us to the end of module 20. So, what we have seen so far is in this module it is a heavy duty module, we saw the basics of a D latch in the previous module. We start it from their connected them back to back and we got, what is called D flip flop and the D flip flop is Master and Slave combination.

So, the Master samples when the clock is on and the Slave samples, when the clocks is off for a negative edge triggers D flip flop. And the combination of that seems to give us think in subs in there is a intersection between these two sampling points and that sampling point is the negative edge itself. So, in summary D flip flop will sample the D input, whenever the clock goes from 1 to 0.

And in the rest of the time, it will keep it as it is. So, this is the definition of a negative edge trigger D flip flop, which we saw in the class. If you want a get a positive edge trigger D flip flop all we have to do is the Clk case signal going in to Clk 1 and Clk 2, change the inverter. Put the inverter on Clk 1 line and keep this Clk to line as it is that will be a positive edge trigger D flip flop. We also saw, how this D flip flop with additional circuit tree we can become what is called D flip flop.

So, I suggest that again you go back and review the video once more, if something is not clear and also go and check whether the way form that are all drawn, whether you able understand in the reproduced. So, circuit that I gave that Q a, Q b and Q c; see if you can

actually draw your own wave form for D and see, whether Q a, Q b and Q c are with respect to the understand in that to have for each of those circuits. So, that brings to the end of module 20, I will see you a module 21.

Thank you very much.