Digital Circuits and Systems
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Module - 19
Gated Latches

Welcome to module 19, so this is the second module for this week, and in the last module, we looked at the notion of latches. So, we started with memory elements and we looked at the notion of latches. In this module, we look at what are called Gated Latches. So, the word gated is useness specific meaning here. So, when we say something is gated, we mean that the circuit is not going to run under it is own, there is going to be some control which will let it behave in a specific manner.

So, when something is gated, it is not supposed to work in the mannerators and if it is not gated, it is supposed to work freely as the original intentions, as we discuss things will become clear. So, let us take, what is called a gated SR latch to begin with.

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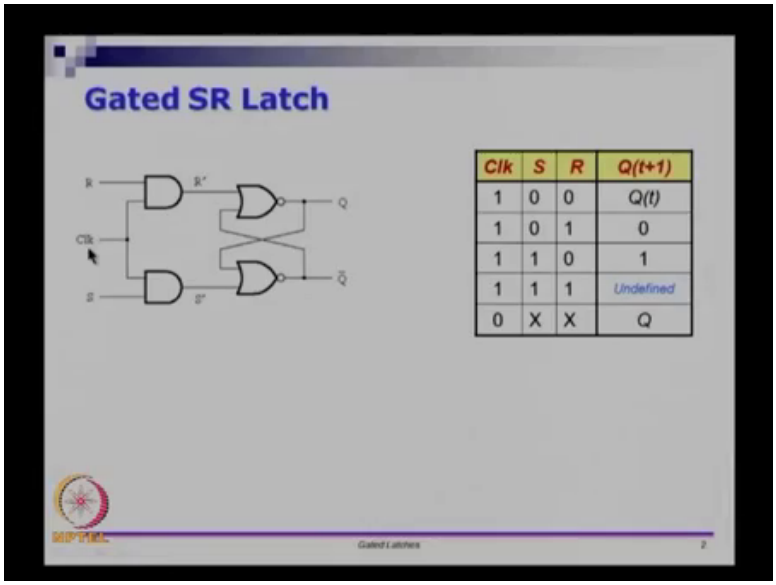

So, let us look at the SR latch. So, if you look at this blob of the circuits, just this part of the circuit, then we have the cross couple NOR gate. So, let us just split in for a while that R dash and S dash are actually the original R and S inputs for now. Let us split in

that, then what we have added to that circuit is 2 AND gates, the two AND gates gets something interesting.

So, there is R, which is coming from here, which is handed with a signal called Clk and this Clk is also handed with S here to give S dash. So, this R dash and S dash are not complements of R and S, so they are just named dash. So, maybe I should avoided that, but they are just R dash and S dash, they are not complements of R and S, the signals are named R dash and S dash.

If you look at a circuit like this, then there is something interesting about this circuit. So, when we looked at latches, the cross coupled SR latch, we had this small issue that this 1 1, the case where both S and R are 1 was actually undesirable. Because, when 1 1 goes to 0 0, there was a specific problem. So, we will see how to cure that problem, but before doing that we will see this little thing.

So, what we have done now is, we have put an AND gate before R and S reaches this R dash S dash. So, the key thing is, if we put Clk equals 0, if Clk is 0, no matter what R and S are, R dash and S dash will be 0. And if you remember the table for SR latch, if both R and S are 0, then the latch will retain the previous values, so that is a good thing and the circuit will work look like a regular latch, if Clk is 1, then we are going to, this part of the circuit, if Clk is 1, whatever R is R and 1 will be R itself and similarly 1 and S will be S itself.

So, you will have whatever the original inputs R and S are, they will be reflecting as R dash and S dash and now, the circuit will work as though is a regular SR latch. So, let us look at the table now. If Clk is 0, no matter what S and R are, if Clk is 0, both R and S will be 0's. So, from this latches point of view, it should just keep the old value of Q, so this Q is Q of t by the way.

And however, if Clk is 1, then we have the top half of the table. In the top of the table, when Clk is 1, the latches now transparent as in, it can see the changes in R and S. We will use the word transparent for that. So, the changes in R and S will go and change the value of Q and Q dash and this is the manner. So, if we ignore the 1 here, then so for while, if you know that Q Clk is 1, it is supposed to work like a latch and these three columns, so this part of the table is as what we saw for the regular latch.

What we got now is this extra notion of what is called gating; the Clk signal is a gating signal for R and S. If it allows the values to be passed through, Clk must be on. If it wants to prohibit what should go in to the latch, then Clk can be off. So, Clk is a control signal which controls, whether R and S are actually passed on to the regular latch. So, this is called a gated SR latch. So, you have a latch which is the cross couple NOR circuit and it has a gated input coming in. So, the input R here is coming as gated input R dash and the input S here is coming as gated input S dash and Clk is in some sense, the enable for this latch.

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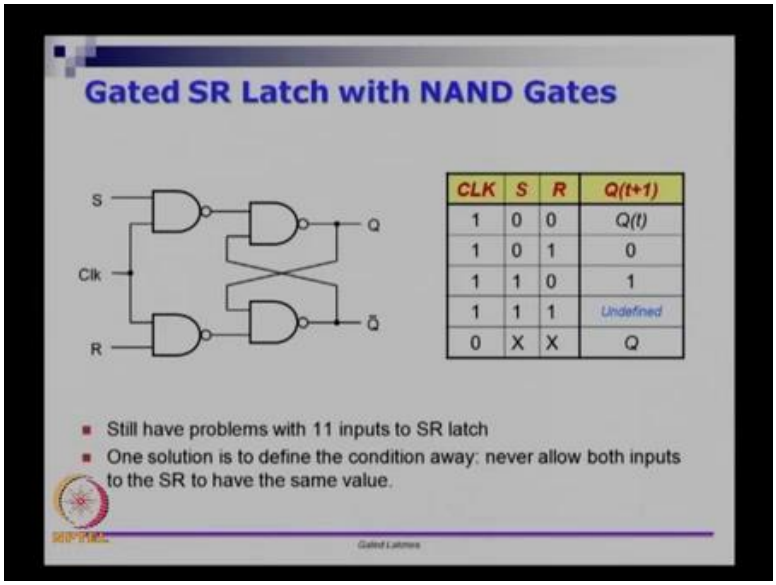

Similarly, you can build a gated SR latch with NAND gates. So, here we have a cross coupled NAND gate. And what we have done here is, we have taken Clk and given it to the 2 NAND gate to 2 AND gates as before. Except that, in this case, we are actually using NAND, instead of AND. Let us see the meaning of this, if Clk is 0, then both S and R will be masked, so you cannot see the value of S and R. Because, if Clk is 0, this line will become 1 and this line will become 1 and both lines will essentially be 1.

However, if Clk is 1, then S will be passed in it is complemented value here and R will be passed in it is complemented value here, so that is what happens in this. So, essentially, it is a cross coupled NAND circuit with the additional gating circuitry added before and this circuitry works according to this table. So, if Clk is 1, it works as though

it is a regular latch, if it is 0, then both these are 1 and if both these are 1, then we know that this part of the latch will retain the old values, so which is Q of t itself.

So, as a black box if you think, there are 3 inputs S, Clk and R, forget the internal details, the black box is S, Clk and R and the output is Q and Q bar. What we want is, when Clk is 1 and if S comes on, we want the Q of t plus 1 to be 1. If Clk is 1 and if R is turned on and S is off, we want the latch to be reset, we want Q of t plus 1 to be 0. If Clk is turned on and if both S and R are 0, then we want to retain the old value.

So, that is this top line and if Clk is turned off, this is like disabling the latch, you do not want to make any changes to the memory to the memory element. So, if Clk is turned off, no matter what S and R are, Q and Q bar should retain it is old value. So, that is in the last row, if Clk is 0, no matter what S and R are, then you have Q of t is 0, so this Q is again Q of t.

So, again you can see a case, where you have 2 x is here, so it is actually meaning do not care. So, even if you have this gated circuit, there is still a shuttle problem, the shuttle problem is that if Clk is 1 and if S and R are both 1, then it can have the same problem that we talk about earlier. So, if Clk is 1, then S and R will go and complemented form here and if both of them are 1, if this is 1 and this is 1, then this will be 0 and this will be 0 and that can lead into a problematic case and the outputs can go undefined.

So, the key thing that is happening is that we are allowing S and R to change at the same time. So, if you go back and remember the timing background that I showed earlier, we saw this two time slots t 9 and t 10 in the previous module. When we went from t 9 to t 10, the S and R where both simultaneously changing to 0 from 1 1 that was happening, that is a problem and the previous inputs Q a and Q b, where both 0's also. So, this, what I called a perfect stom, those conditions could happen.

So, by putting a gate here, a Clk here, it is not changing that as long as the Clk is 1, the same conditions can happen with respect to S and R now. So, this 1 1 case is still in undesirable case, if Clk is 1 and if S and R are 1, it is still undesirable, because when this 1 1 changes to 0 0 here simultaneously, this can upset the way the flip flop works and the flip flop can go into a oscillating situation.

So, what we want is somehow get rid of the condition that both S and R are changing at the same time to the same value, we do not want that. Even though 0 0 is okay, changing from 1 1 to 0 0 was a problem. Somehow, if I prevented S and R from taking the same values, then that is a good thing to have, we are going to do exactly that in the gated D latch.

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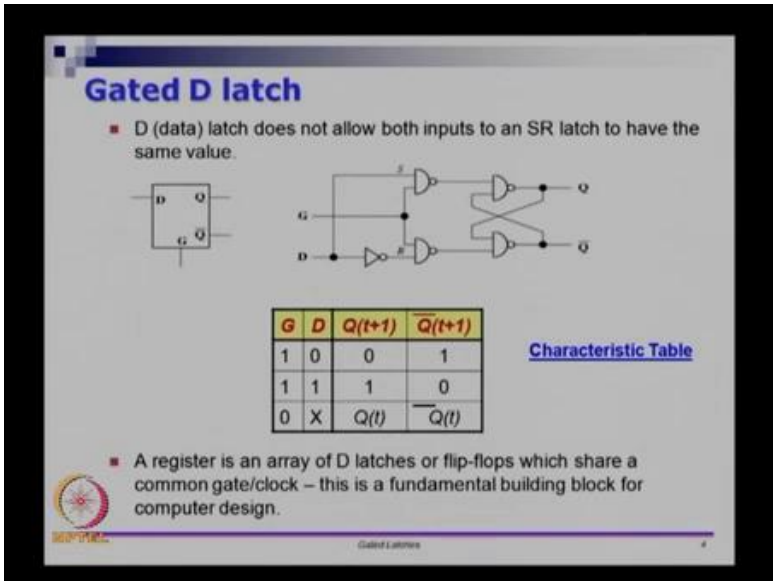

So, let us see this circuit now, what you have here is a basic SR latch and if you take up to this point, it looks like it is a gated SR latch. If I start from here and if I look right side, it is like a gated SR latch. The only thing that is done is, the S and R inputs are not two different inputs, we want to avoid the condition that S and R should not take the same value. One way in which we can ensure that is, we take a signal called D, we give the value as it is to S and we give it is complement to R.

Now, if I look at it from S and R points of view, S and R can never be the same, you see the point. So, if S is 0, R should be 1, if S is 1, R should be 0, we will never have the case 1 1 coming into this gated D latch. So, if we take a gated SR latch which is this part starting from here to the right, that is a gated SR latch and to the SR inputs, if you add this extra piece of circuit or you take a single D input, it goes as uncomplemented and complemented inputs to S and R, then you will never have the condition when both S and R are 1 simultaneously.

In fact they cannot even be both 0's simultaneously, so these are interesting case and this is going to be called a gated D latch. The symbol we use for a gated D latch is just as follows. So, D is a single input that comes in, there are 2 outputs Q and Q bar and there is a single gate signal called G.

So, the G will control, so G is going to be the gating logic for this latch. If G is on, then D input is registered or in some sense, the Q and Q bar can change with respect to D, if G is on. If G is off, the change in D will not reflect in as changes in Q or Q bar. So, let us see the table if G is 0, no matter what D is, Q of t plus 1 will be the same as Q of t and Q bar of t plus 1 will be the same as Q bar of t. So, Q is being retained from the past, so it is kept as it is.

However, if G is 1, if D is 0, Q of t plus 1 is 1 and if D is 1, Q of t plus 1 is 1, if D is 0, Q of t plus 1 is 0 and if D is 1, Q of t plus 1 is 1. So, what it is doing is, Q of t plus 1, the English way to say this is, Q of t plus 1 follows D, when G is 1 and Q of t plus 1 retains the old value, when G is 0; that is a way to say this in English. So, the nice thing about this is, you can see that whatever data you are getting in, so if you put a 0 here, Q becomes 0, if you put a 1 here, Q comes 1.

So, this D, you can think of it as a data input and G, you can think of it as an enable, if enable is on, data is copied to Q, if enable is off, Q retains the old value of Q. So, this is nice way to put, what D latches supposed to be. So, this is a very useful thing, because so if there is any input change here, if the enable is off, then Q will still not change, only when the enable is on, the change in D will reflect as change in Q. So, this is a very useful thing and we have that so called characteristic table of the gated D latch here.

And you can actually take an array of these D latches which share a common gate signal or a clock signal and we will call this a register. You look at registers in a little while later. But, so far what we have is, we have a gated D latch and this avoids the explicit condition that 1 1 being undesirable, we got rid of this completely.

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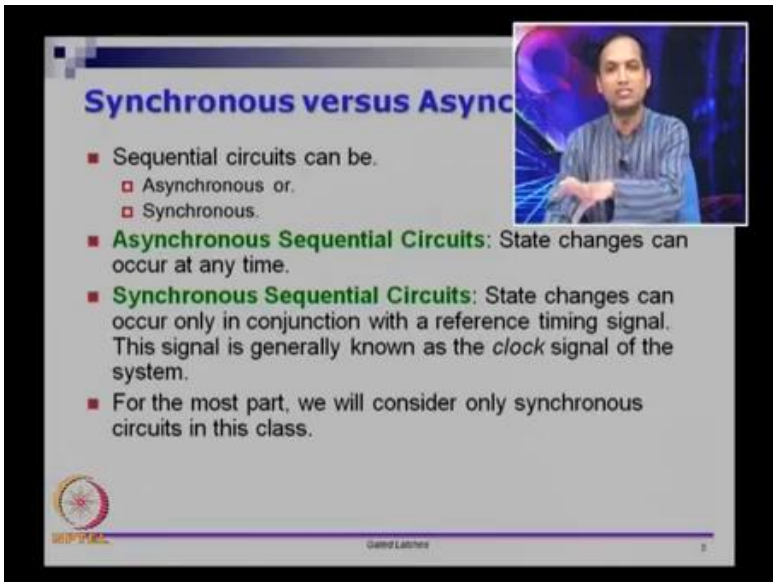

So, now, I want to talk about different kinds of circuits. So, already in circuits, we made this distinction, there are these so called combinational circuits, where the current output is dependent only on the current input, not on what the previous values of the outputs are or any history and so on. So, combination circuits do not have memory, sequential circuits have memory, so this is the first classification I made.

Sequential circuits have memory, in some sense, they have a feedback parts somewhere, because of it is able to remember the value and it is useful for designing circuits, where you have to do some actions depending on something that happened in the past. Within sequential circuits itself, there is a further classification, there is a circuit which are called asynchronous circuits and there are things which are called synchronous circuits.

So, in an asynchronous circuits, the change in the output of the circuits can happen at any point of time. So, there is memory, but the change that you see in the circuits can happen at any point of time, whereas in a synchronous circuit the changes can happen only at some pre defined intervals. So, you have some reference signal, which we usually called the clock and the clock signal, only when the clock signal has a particular value or if there is something which is defined by the clock signal, we use that as a reference point and then you have your circuitry operating.

So, an interesting way to think about this, so I will give you a quick example, for example, let us say, we are going to classes and in schools and in colleges, we sometimes

here the bell ringing. So, the bell ringing at 8'o clock, saying that the class at 8'o clock is starting and 8:50 the class ends. Again, we see a bell ringing at 9 and then bell at 9:50 and so on. So, that is way to actually synchronize things, a single bell is heard by all the class rooms. So, a teacher, who is teaching the class, if he or she hears the bell, it means that the class time is over and the class is supposed to stop.

So, all the activities in the class will get over once the bell rings. Similarly, so maybe I am in one class room I am teaching the class, then I need to walk to another class room in another building. So, I walk and then I go to another class, I takes sometimes settle down and so on. Students are also walking in from another classes, again the starting bell rings, so that is again a synchronization signal which says, now the class can start. Let us say if these two are not there, then we need to look at our particular watches.

So, I will look at my own watch see that the time is 9:50, then I will stop my lecture, then I walk to another class room, I see that in my watch, the time is 10'o clock, I start. But, this watch that I have here maybe out of sync with your watches, the student watches that can happen. And if there happens, maybe I am thinking that the time is 10'o clock, but the time is actually 9:55 and I started the class already, so this can be a problem.

So, many times we want to synchronize things, in real life also we want to synchronize things and we have signal which tell us synchronization. For example, even days of the week or hours and so on are actually just synchronization points at some level. Then, there are time points at which we want think to be things to be asynchronous. So, when that happens, there is something that is coming in a reference, but the activities can happen no matter where the reference is.

So, clearly classes cannot be thought asynchronously. So, you have to be there, I have to be there to teach a class. But, let us say I have recorded a video and I post it online, then my recording of the video is done at some point of time and you watching the video can happen at some other point of time and each one in the class can also watch the video at any point of time. It is not a single broad cast that I am making, so that can be treated as asynchronous.

So, the communication between you and me in the video recording set up would be asynchronous. So, for example, if I am sitting and chatting with you, then we go back and forth, whereas if I send an email to you that is again asynchronous. Because, the

moment I type something and I send it, you may take a day or you may take an hour or you may immediately see the email or you are probably away from email, you do not may even see it for some time, so all those are asynchronous events.

Whereas, when we sit and in some sense, long steps do something that would be synchronous. So, synchronous sequential circuits are those circuits, where in some sense, there is something called clock. There is a global clock that is seen by all circuits, all parts of the circuits and all parts of the circuit function, when this particular clock signal comes on.

And they do, what is called clock latching in the memory, the actually works slightly differently. So, when the clock comes in, they work and when the clock is not there, they do something different. So, there is the notion of what is called asynchronous sequential circuit and synchronous sequential circuit. If the output of a circuit block can change without any reference to the input, so called clock signal will call them asynchronous circuits.

If the functionality of a circuit, if the output of a circuit is defined with respect to the reference at which the clock came in, then we will call them synchronous sequence. So, keep this in mind and we will see this as we go long.

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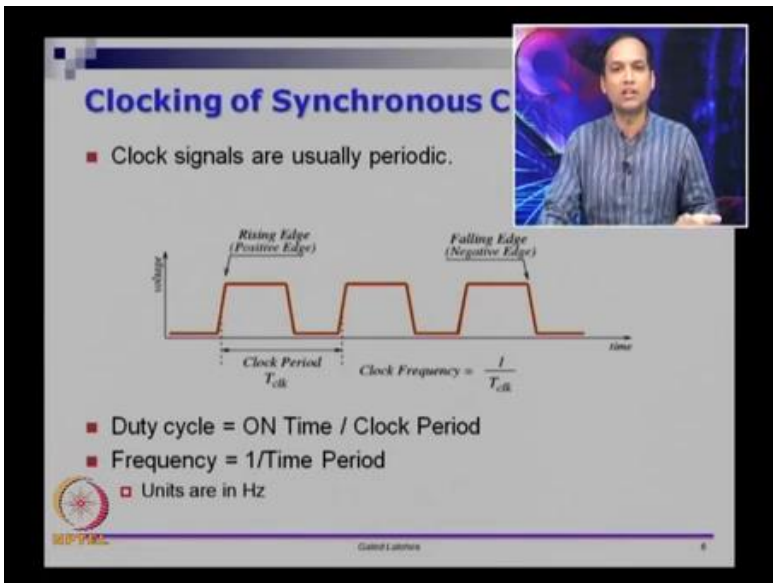

So, let us see quick example, let us say I have a clock signal that comes in periodically, for example, ringing the bell is a periodic thing. At 8 o clock will ring at 9 o clock will ring at 10 o clock will ring and so on, so that is a periodic signal. So, in the real world the clock signal is also another signal and this signal has voltage levels. So, it could be a voltage level 0 or it could be a at voltage level 1.

When, it is at voltage level 0 will call that level 0 and when is at voltage level VDD, we will call that level 1. And in real world this going from level 0 to level 1 is not instantaneous, it is not the magically there is a signal which goes from 0 to 1. So, typically there is some charging and discharging are something that may happen in other parts of the circuit, which will require some non 0 time to go from 0 to 1 or 1 to 0.

For a clock signal, it is usually coming from a quads, it is a physical entity, which is oscillating at a certain frequency and those, when you tap the oscillator and when you bring it into the chip, it is that takes some finite amount of time also. So, switching from level 0 to level 1 is not an instantaneous. Similarly, switching from level 1 to level 0 is also not an instantaneous.

Nevertheless, the first thing is that, usually the clock signals are periodic, what we mean by that is, there is frequency at which this clock is going to take. So, this clock signal here this way form here for instance goes from 0 to 1 and , goes back to 0 at some point again goes from 0 to 1 at let us say at time period t away. So, this happens at let us say 0 time units and this happens at let us say t time units.

The next time the same thing will happen will be a 2 t, next time that will happen will be at 3 t and so on, so that is called a periodic signal. So, the time difference between two successive events of the same type is the clock period. So, anything that rises has to fall down on before it rises again. So, clearly there is a fall in between, you can ever measure the time period between the two falls and that should also t clock.

So, will call this edge going from level 0 to level 1, has the rising edge and the edge that goes from 1 to 0 will call that the falling edge. So, we have rising edge and falling edge. So, every clock period will have one rising edge and one falling edge. So, the clock period could start with one rising edge, somewhere in the middle it has one falling edge and then just before the beginning of the nest next rising edge.

So, that is a clock period or if you measure from the negative edge or the falling edge, it is starts with just the beginning of the falling edge, then the level is 0. Then, goes to one rising edge and then just before beginning of the next following edge, so even that is called a clock period. So, the clock period essentially says how frequently this reference signal is coming.

So, for example, in the class room example I give 8 o clock, 9 o clock, 10 o clock means, there is a clock signal every 1 hour. Whereas, if I had let us say class, which is only half hour, then I will have bell at 8:30, bell at 9 o clock and so on. So, by clock rate is different in that case. So, frequency or the clock rate is defined as 1 1 over time period. So, remember time period is measured in units of seconds, it could be in nano seconds, milli seconds, micro seconds, whatever and frequencies one over time period or this is the rate at which the clock is coming in and the units are in hertz.

So, hertz is always return with capital H and Small case z, there is also relevant definition call the duty cycle. So, if you notice this, there is a small period at which is rising and there is for significant amount of time, it is at level 1. And then it falls to 0 and then for some amount of time, it is kept at 0. So, duty cycle is defined as the on time or the time at which it is level 1, divided by the clock period.

So, in this example, the on time is slightly bigger than the off time. So, I would expect that the duty cycle is greater than 50 percent. But, if the length of the on period is exactly the same as the length of the off period, then the duty cycle would be on time divided by on time plus off time, if the both are the same, then it is 50 percent. So, this definition of duty cycle is also useful.

But, just remembers this for while, we will need this in the later classes. Now, it is specified here, so that is a definition, it is all in one place. So, we have seen, what is a clock edge, what are the levels, what is a positive and what is negative edge and we have seen, what is called a duty cycle.

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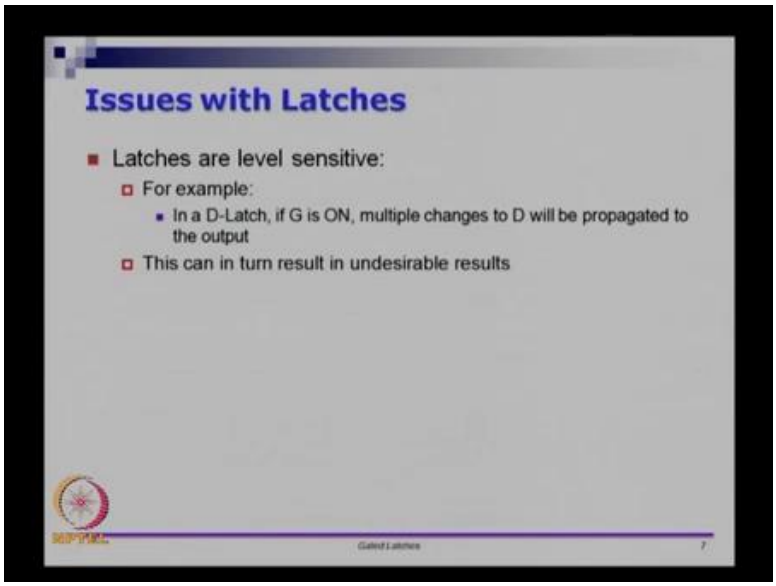

And let us now go back to the latches. So, latches we call them level sensitive, because the output of a latch can change. If there is any change in input as long as the level at which the gating signal is there is on. So, no matter when D changes as long as G is on, even if D changes many, many times, you will see an effect of that on Q in the case of a D latches.

So, D latches called a latch. So, the circuit I should earlier is called a latch, because as long as G is on, even multiple changes in D will be propagated to the output Q. And this is for in some cases, but in many cases actually undesirable, we do not want changes in D to be propagated to Q, whenever G is on. So, we will see, why this is a case as when we build an examples.

But, this is an issue in practical circuits, so what we will do is, we will go and look at what are call edge sensitive's circuit instance. So, edge sensitive circuits are those which are not depended on the level, but they are going to depend on the rising or the falling edge. So, if you go back to this, usually what happens is ((Refer Time: 26:16)) a clock signal takes very little time to some amount of time to go from 0 to 1 and from 1 to 0.

But, this time is much lesser than the time period, when it is kept at 1 and when it is kept at 0. So, usually the rise time and fall time are much, much lesser compare to the time at which it is on, the time at which is off. So, I just want to you know that and we will do

what are called edge sensitive circuits, where some action or the reference point comes from either this edge or this edge and not based on the level.

So, at this point, what I would like you to do is, go back and look at the circuit and go and check, if you keep the G signal or the clock signal on in the gated circuits that you seen so far. Try and change the D signal in the D gate, so the D latch go and change D, keep G at on, change D, see what happens to the change in Q, see if Q changes at all or not, you will notice that in a gated D latch Q will in fact, change.

So, we are going to design a circuit later which actually does something different and will get to that in the next module. So, this means to end of module 19 and I takes some time to go and Review materials from both module 18 and book module 19. Because, you will need a lot of that for module 20, so revise them before you go to module 20.

Thank you.