VLSI Technology
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Lecture - 35
I 2 L Circuits + Transistors in ECL Circuits

So, we have been discussing about the basic I-square L circuit that is the integrated injection logic, in which we use both pnp and npn transistor. The pnp transistor is used as the current source. We use a lateral pnp for this application and we have an npn transistor, we use a vertical npn transistor. The difference in this I-square L npn transistor is that it is operating in an inverted mode. That is at the top surface we have the collector and the substrate is the emitter. So, this npn transistor is operating in an inverted mode and we have already seen that we can either add an n plus collar to this I-square L circuit, if we want to facilitate hole injection in the direction of the npn transistor and we can replace this n plus collar with an oxide isolation also. The oxide isolation will have the advantage of space saving, but at the same time we have to provide multiple base contacts if we want to avoid the problem of the unequal drives.

So, with this background, let us now concentrate on a more advanced I-square L technology, where we use oxide isolation, yes; we use multiple base contacts, yes and we align the base contacts automatically. Thus the name self-aligned process; we have a self-aligned process, whereby the base contacts are aligned automatically with respect to the n plus collectors and we will see that in doing so, in developing this self-aligned I-square L technology, we take the help of various sophisticated technological steps, for example ion implantation, for example dry etching, for example chemical vapour deposition. So, this advanced self-aligned I-square L technology is possible or was first made possible because of the advent of these technologies.

Let us now take a look at this self-aligned I-square L structure.

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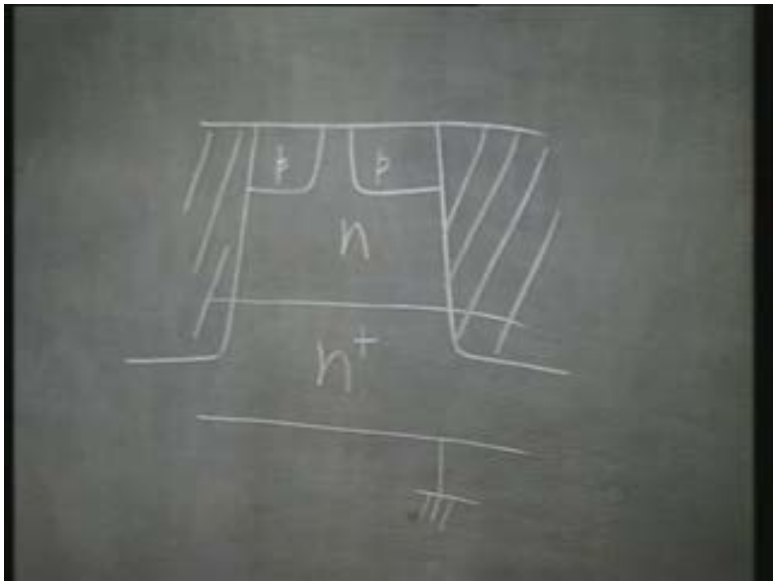

You know that in the I-square L structure, we started off with the n on n plus substrate. This is permanently grounded and we have oxide isolation. The devices will be housed here, so we will have a p region here and another p region here, right. This is going to be my pnp transistor and in here I will diffuse in and we will have the npn transistor. Now, in the self-aligned I-square L technology also, up to this the process steps are exactly similar, exactly the same.

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So, what we have is ….. Then, we grow a thin oxide over this. This is thinner than this oxide, but it is not very thin; it is thick enough to mask. In the next step, we deposit; we do not dope, we do not diffuse, we deposit arsenic doped polysilicon over the p-type region topped with CVD silicon dioxide and pattern it. That is to say I have actually skipped one intermediate step. You first deposit this arsenic doped poly all over the region, then you top it up with CVD SiO 2 and then you pattern it, so that it is retained only over these regions. So, this arsenic doped poly is going to act as the collectors of the npn transistor.

Now, you see, my next job is going to be to find out where I should put my base contacts. You know that I should have multiple base contacts that is I should have one base contact here, one base contact here, like that, yes; at the same time, you know that the base contact should not be in touch with the collector, should not be in touch with the collector, it will short. In that case, I will have the base collector short. So, I must put the base contacts properly. How do I do that? In doing this, we take the help of another CVD layer of silicon dioxide that is to say we deposit another silicon dioxide layer by chemical vapour deposition.

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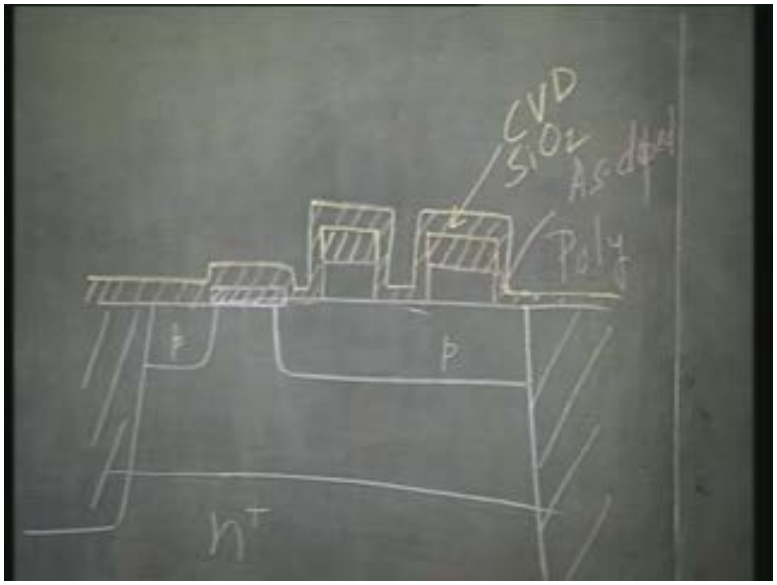

So, I have two layers of CVD SiO 2. The first CVD layer was put on top of the arsenic doped poly and patterned, so that only the poly region has a cap of CVD SiO 2. In the next step, I have deposited another layer of CVD SiO 2 all over the place, right; fine. Now, my next step is to anisotropically etch part of this CVD SiO 2 layer. When I say anisotropically etch, I mean that the etching is only going to be in this direction, in the vertical direction. I can do that by using the dry etching technique, by suitably adjusting the etching conditions and I partly etch that is I etch only this much. So, what is going to happen?

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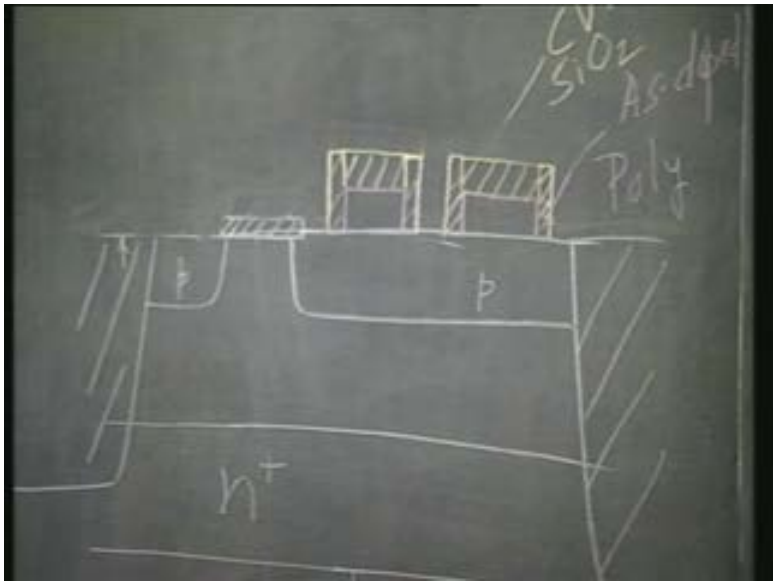

This is going to be removed from all these portions, but going to be retained at the side walls and at the top. So, you see, now, in addition to having the top capping layer of CVD SiO 2, I have also added a side wall of CVD SiO 2 to my n plus poly regions, agreed.

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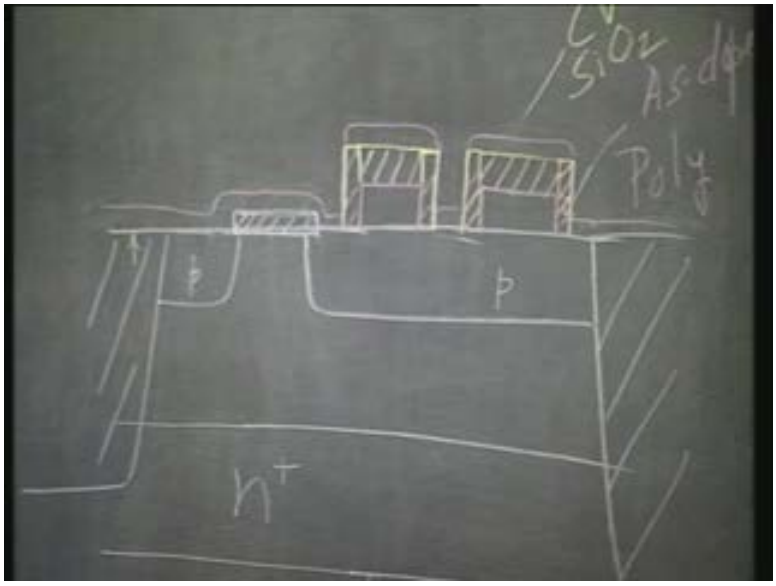

Now, all I have to do is to deposit the metal, aluminium, right and I etch this aluminium, this is a non-critical etching, from certain regions.

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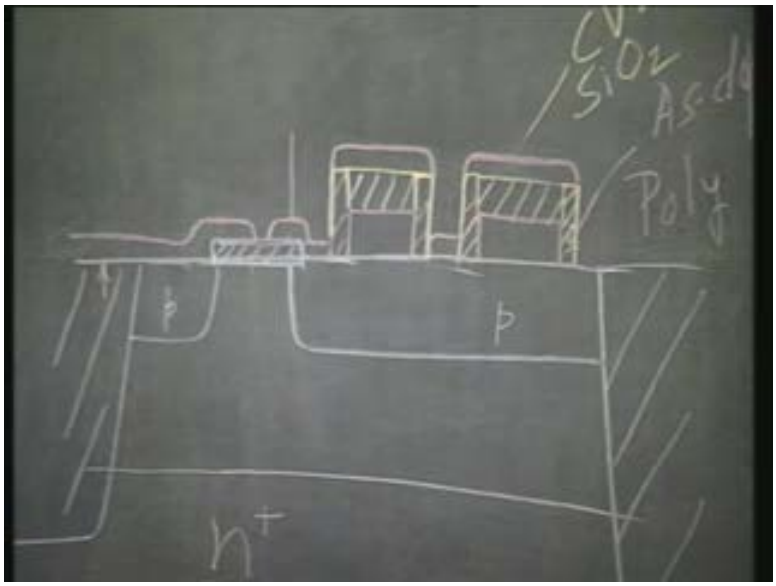

So, you see, in one shot you have provided all the base contacts, multiple base contacts, right. So, this is the self-aligned I-square L technology, in which you make use of the more advanced etching technology that is the dry etching, the anisotropic etching,

whereby you retain the side walls of CVD SiO 2 and remove silicon dioxide from everywhere else and this side walls of silicon dioxide actually provides the self-aligned technique, right. It protects the collector regions from getting shorted with the base metal contact. So, this is the self-aligned I-square L technology.

You know, I told you previously that all the transistors we have discussed so far, the bipolar junction transistors, they are, so to speak, more or less general transistors, general npn transistors. We have not been very specific as to what their performances are. I-square L of course is a different story; because of its particular circuit configuration, you need to realize both a pnp and npn transistor and it is a merged transistor logic. So, we have discussed the particular building block of an I-square L in detail. But, nowadays as we are going for faster and faster circuits, you know bipolar junction transistors are faster circuits compared to MOS. We say that bipolar junction transistors are high speed and MOS are high density. So, when we are going for high speed transistors, we talk about bipolar junction transistors. We use bipolar junction transistors in ECL, emitter coupled logic. These are the fastest circuits.

Now, when I want to have such a high speed transistor, what are the specific requirements of these transistors? Specific requirements of this transistor will be, first of all we must have a low base resistance. What do I mean that we must have a low base resistance? That means the extrinsic base must be highly doped and the extrinsic base must be aligned to the emitter.

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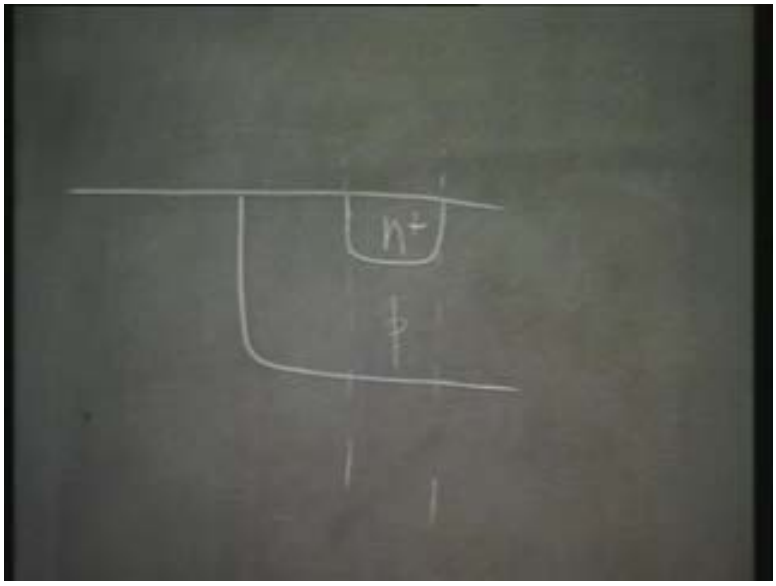

That is to say, if this is the base and this is the emitter, this is the base; your active transistor is here. So, this base doping is automatically fixed by the gain of the transistor, but you want to make these regions highly doped which are extrinsic base. At the same time, notice that the extrinsic base must be separated from the emitter, otherwise we will have an n plus p plus junction there, right. So, again you see, you need to have the extrinsic base self-aligned to the emitter. So, for high speed transistor, one of the major requirements is to have the extrinsic base self-aligned to emitter and of course, for any high speed circuits, you must have low capacitances, right; low collector base junction capacitance, low emitter base junction capacitance and if I want to have low emitter base junction capacitance, it is found that as the device dimensions become smaller, as the emitter size gets reduced, okay, let me redraw this.

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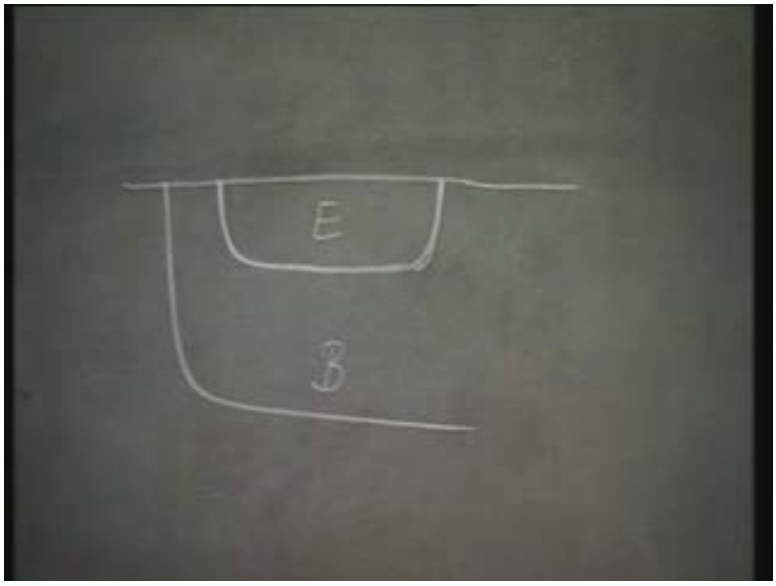

This is emitter, this is base. You see, the emitter base junction capacitance will have two parts. One is the planar capacitance that is determined by the size, the length of the emitter and the other is the peripheral or the side wall capacitance. So, the emitter base junction capacitance will have two parts.

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One is the planar part and the other is the side wall or the peripheral part and as we reduce the emitter dimensions, you see, increasingly the peripheral capacitance or the side wall capacitance become the dominating factor. As the emitter size reduces, the speed does not really become increased to that extent, because now, the peripheral capacitance is dominating instead of the planar capacitance and you have not done anything to the peripheral capacitance. How can you reduce the peripheral capacitance? By making the junctions shallower; not just reducing the emitter size, but also reducing the junction depth. So, for high speed transistors, it is very important that you have shallow junctions in addition to having smaller dimension.

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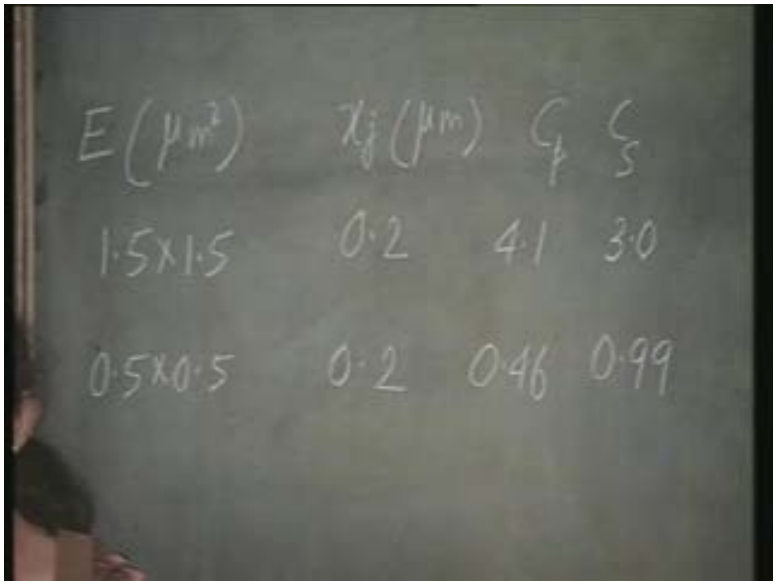

I just wanted to give you some example; for example, if the emitter area in micrometer square is 1.5 into 1.5 and if the junction depth, the emitter base junction depth, if that is 0.2 micron, then you have C planar and C side wall, let me call it C p and C s, C planar and C side wall, then these two are, okay, C planar is 4.1 and this is 3.0 in femto farads, 10 power minus 15 farads femto farads; one is 4.1 femto farads and C s that is the side wall or the peripheral capacitance is 3 femto farads. On the other hand, if I reduce the emitter area to 0.5 into 0.5 and keep the junction depth the same as 0.2, then planar capacitance goes down to 0.46 femto farads, but the side wall capacitance is about 1

femto farads. So, you see, as you reduce the emitter size, for the same junction depth the side wall capacitance starts to dominate, when the emitter size is smaller.

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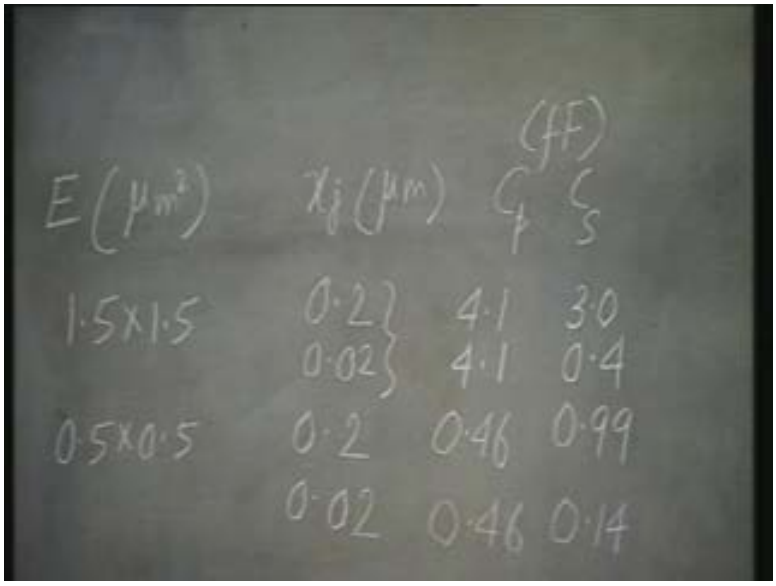

If we go for shallower junctions, like if we make it 0.02, nothing happens to the planar value of the capacitance, but this reduces and here also. So, you see, this becomes very important when the emitter size is reduced. For smaller device dimensions, it is very important that not merely you reduce the device dimensions, because that is finally not going to determine the speed, it is the peripheral capacitance or the side wall capacitance and that can be reduced only if you reduce the junction depth, which brings us to the important requirement of a high speed transistor - I must have shallow junctions. But you see, we have already stated that it is technologically difficult to realize shallow junctions; technologically it is going to be difficult. The shallower the junction is technologically if you ….. to diffusion or implantation, it is going to be difficult.

The other point is from the transistor performance itself.

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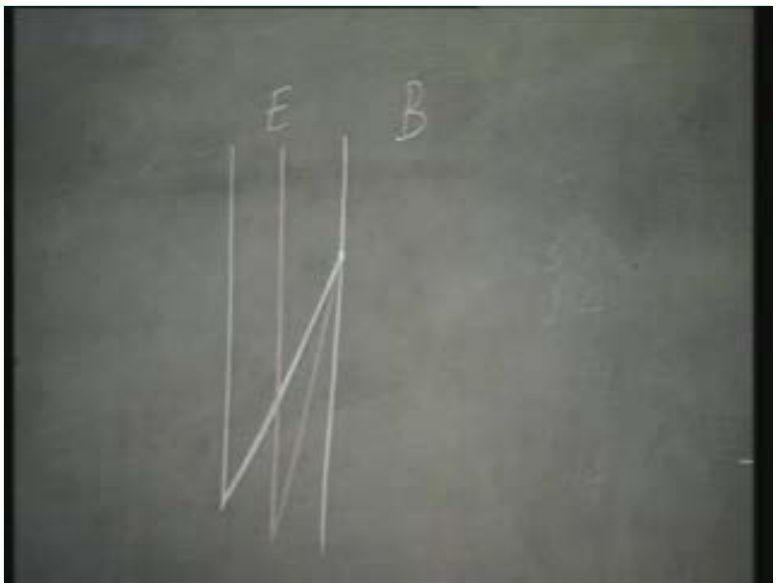

Suppose I have emitter and the base and here I have certain p concentration, then it must fall to zero and it is almost a linear fall and the slope of this line determines the gain of the transistor. Now, if I have a shallower emitter base junction that is if I have a smaller emitter region, I have the same hole concentration and now it must go to zero here. That means I have a steeper slope if I want to have a narrower emitter, if I want to have a shallower emitter base junction and if I have a steeper slope that means the gain of the transistor is going to fall. So, if I want to have very shallow junctions, the gain of the transistor is going to be affected adversely. So, apart from the technological difficulty, it is also going to be detrimental to the transistor performance if we want to have a shallow emitter base junction.

So, what we do is this. We use a poly emitter transistor; we use a poly emitter transistor. What is the significant of having a poly emitter transistor? That is you have, you deposit a poly layer; you implant it n plus and from that n plus you have, by thermal anneal you have a shallow junction. So, your emitter basically has two parts. One is in the poly, the other is the shallow doped region in the crystalline silicon. Now, what is the situation going to be?

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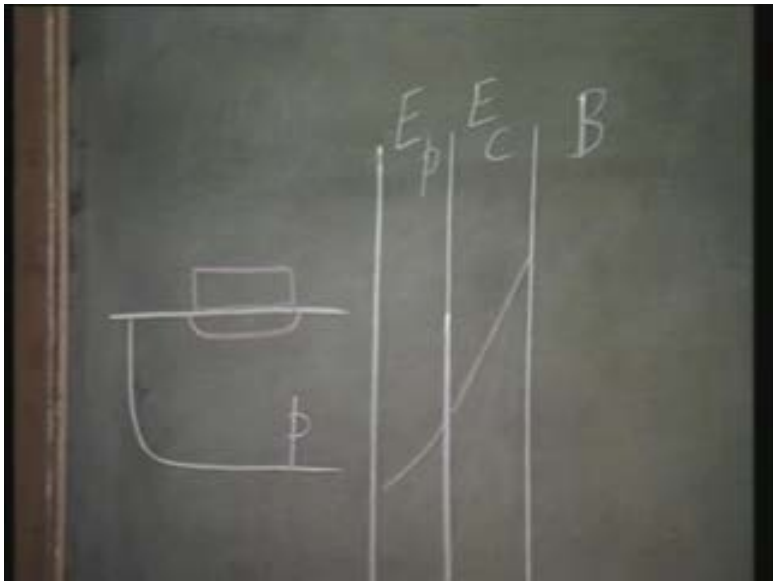

I have realized a shallow emitter junction, but I have an emitter in poly too. So, my emitter basically is having two parts - emitter in the crystalline silicon and emitter in the polysilicon. Now, if you want to look at how the hole concentration should fall, you know, it should actually does not have to go to zero here; it can come like this and then fall like this. I can keep the poly layer as thick as I want; does not matter, because it is not going to affect my peripheral capacitance at all. The peripheral capacitance will be determined only by the junction depth which is the depth of E C. That means what I am trying to say is this.

I have the p region here for the base and I have deposited a poly here from which ….. So, the side wall capacitance is only determined by this region which is very shallow, but the entire region is working as my emitter and therefore, the slope of this curve does not have to be very steep; it does not affect the gain of the transistor. In fact, in poly emitter transistor the gain is increased. The poly emitter transistors have a lot of gain and the gain will be even more improved. Basically the gain improves because, hole injection is suppressed in this poly and crystalline interface and it can be further suppressed if you put a thin interfacial region here, thin oxide region here, thin interfacial oxide, then the

injection of holes will be suppressed to a larger extent. The gain of transistor will become much higher.

Now the point is, so we have underlined the basic strategy. What are our requirements? First of all, the extrinsic base must be self-aligned to the emitter and the other thing is that, in order to realize a shallow emitter without having to sacrifice the gain of the transistor, we must use a poly emitter. So, this is the strategy behind a high speed transistor in integrated circuit; high speed transistor as it is seen in ECL. All ECL transistors are fabricated in this manner. So, let me try to outline the steps in this ECL transistor.

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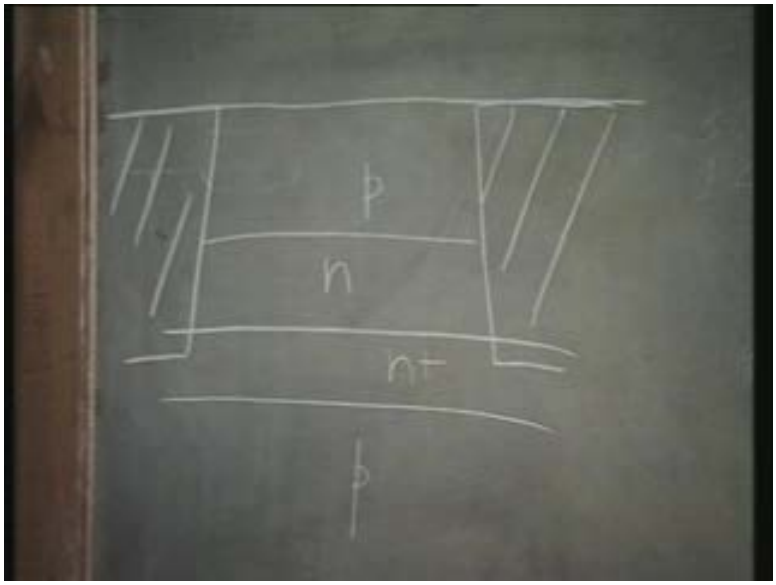

You remember, in a conventional transistor we started out with a p-type substrate. We had an n plus buried layer and then, we had an n epitaxial layer and we have done LOCOS. This is actually my n region and then I have the p region for the base. I have the n epitaxial region and then I have doped p. So far so good; so far nothing has changed, so far my ECL transistor looks exactly the same as the conventional transistor you have already discussed. Now, my first step is to define the extrinsic base, right. I have doped the intrinsic base. This doping is determined by the gain considerations, by the Gummel

number; you have decided how much total charge to put in the base, fine. Now, next step is how to obtain the extrinsic base and how to have it self-aligned with the emitter.

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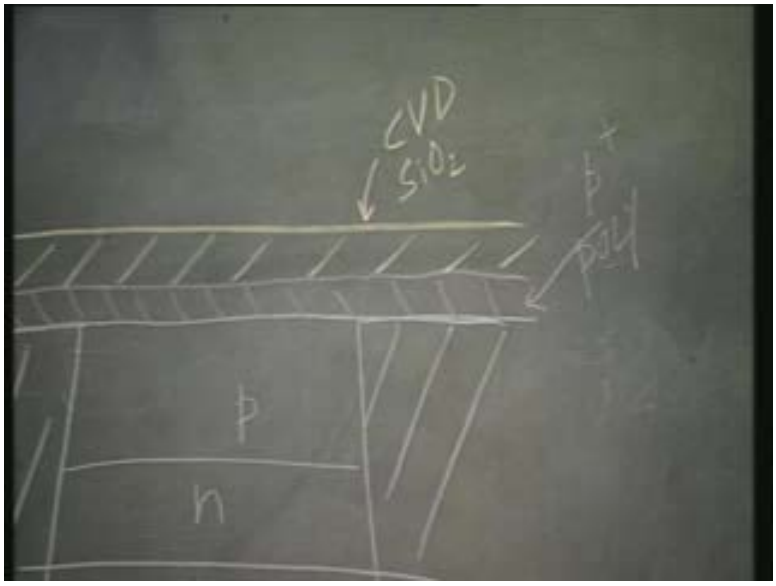

So as the first step you are going to deposit p plus poly and top it up with, top it up with CVD SiO 2. So, the yellow layer is …. Next, you remove it from certain portions.

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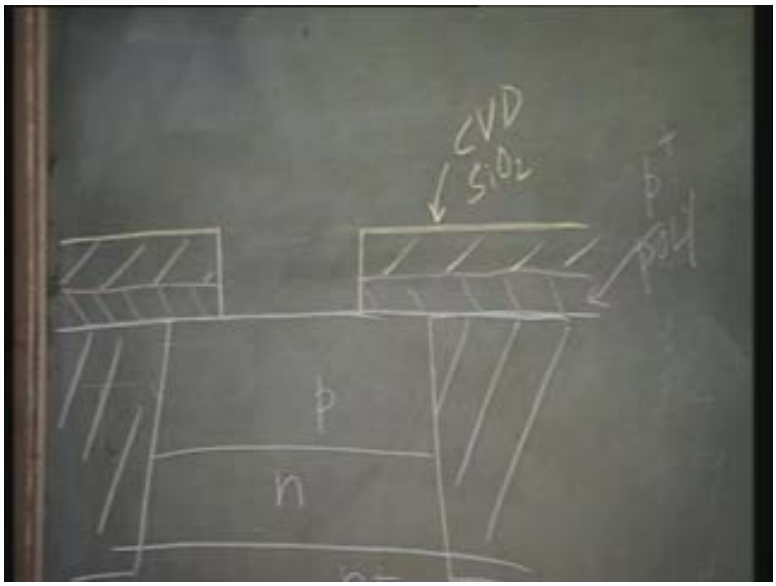

Fine; I have removed it from certain portions. What should I do next?

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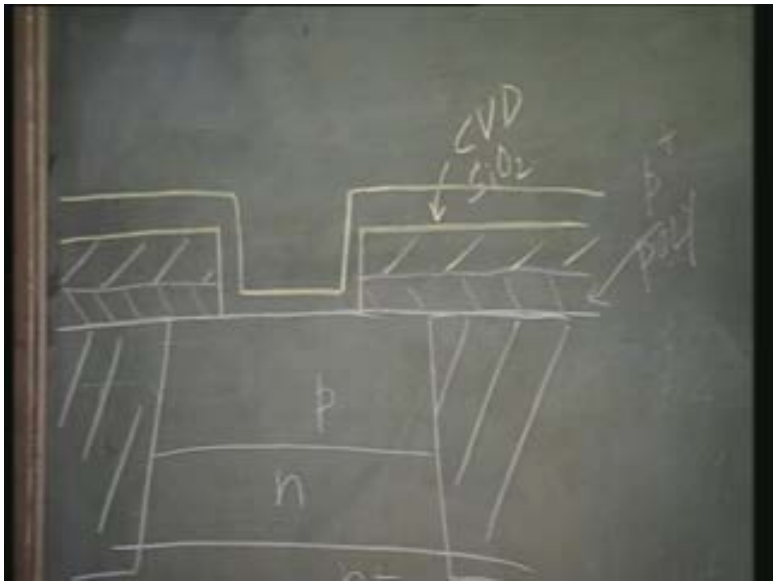

I should deposit another, a second layer of CVD SiO 2 and I do an anisotropic etching to partially remove the CVD SiO 2 layer. So, what do I have? I want to remove it from here.

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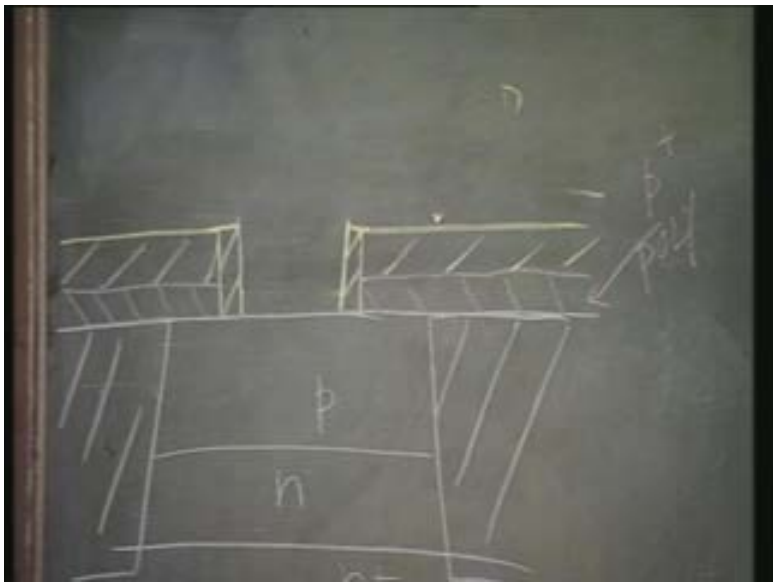

However, the side walls are retained and I remove it from here. In a way analogous to my self-aligned I-square L design, I have retained the side walls of the CVD SiO 2 and removed it from everywhere else. That is the second layer of CVD SiO 2 is retained only at the side walls and removed from everywhere else, agreed.

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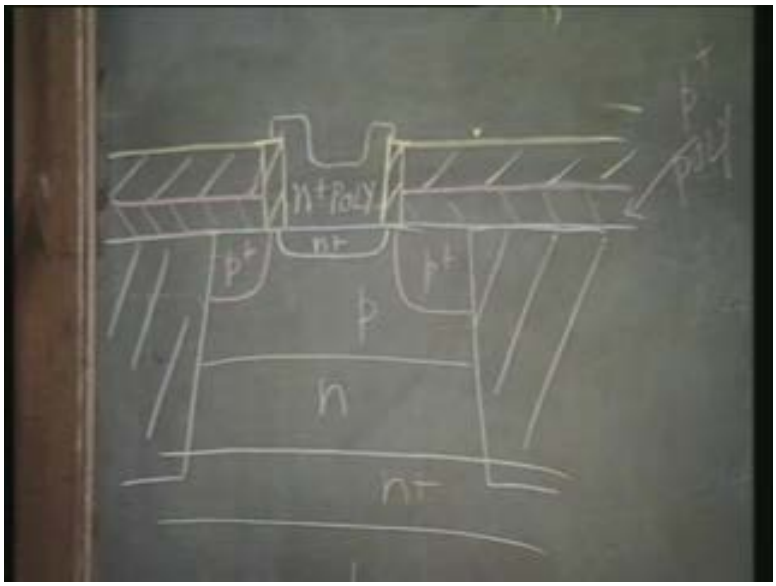

Now, all I have to do is to deposit n plus poly all over and then remove it from certain region, so that it is retained only here. What do I do next? A thermal annealing and then, what do I have? We have …. This is my emitter; I am using a poly emitter. I have a shallow junction and also I retain the n plus poly. So, this composite layer can be used as my emitter and you see, look at the p plus extrinsic base. They are self-aligned to the emitter, separated by this spacer layer. Without this spacer layer, now you understand the importance of the spacer, without the spacer, I should have a p plus n plus junction.

This spacer layer actually gives me an extrinsic base self-aligned to the emitter. This is the self-aligned poly emitter transistor with poly extrinsic base and you can take your base contact anywhere from this poly line. You do not have to have separate space for base contact; you can take it directly from this line, take it out somewhere there, right. You do not need …., this is automatically aligned to your extrinsic base, this poly layer.

So, this p plus poly layer itself is going to serve as your base contact. Considerable area saving, you have all your requirements - you have reduced the extrinsic base resistance, you have aligned, self-aligned the extrinsic base to the emitter, you have realized your poly emitter transistor.

The crucial step in this self-aligned technology is realization of this spacer. This spacer must be thick enough, wide enough so as to separate the emitter and the extrinsic base. At the same time, it should not be too wide. In that case you are going to have an increase in the base resistance. So, you have to control the width of this spacer layer; the spacer layer, the side wall, the spacer side wall you have to control it very accurately. That is the most critical step. So, you can also have a variation of the same theme, you know. ….. you could do is, in this case we had deposited CVD silicon dioxide. Instead of that, you could have an undoped poly layer deposited, so that your spacer is not made of CVD SiO 2, but it is made of undoped poly and later on, you could oxidize this undoped poly.

What are the advantages? You know that when silicon is oxidized, its width actually increases. So, you could actually have a very thin layer of poly spacer that would increase 2.2 times to give you the spacer layer, the adequate spacer layer. So, that actually offers you better control on the spacer layer thickness. Here you have to control the CVD SiO 2 thickness. There you were simply controlling the CVD poly thickness which can be made very thin and then when you oxidize it, it expands and gives you adequate spacer layer thickness. Second advantage is in this particular case, you see, your surface it has CVD SiO 2. CVD SiO 2 is not as good in quality as thermal oxide. If on the other hand, you deposit undoped poly and later on oxidize it, you are going to have a better quality thermal oxide protecting the surface. So, these are the two possible variations of the same theme. In order to have high speed transistors, you could use that. So many other variations are possible. In addition to this, you know, even for the intrinsic base you could use poly base.

Now, the most important, most interesting aspect of this discussion - I have two figures here on the board.

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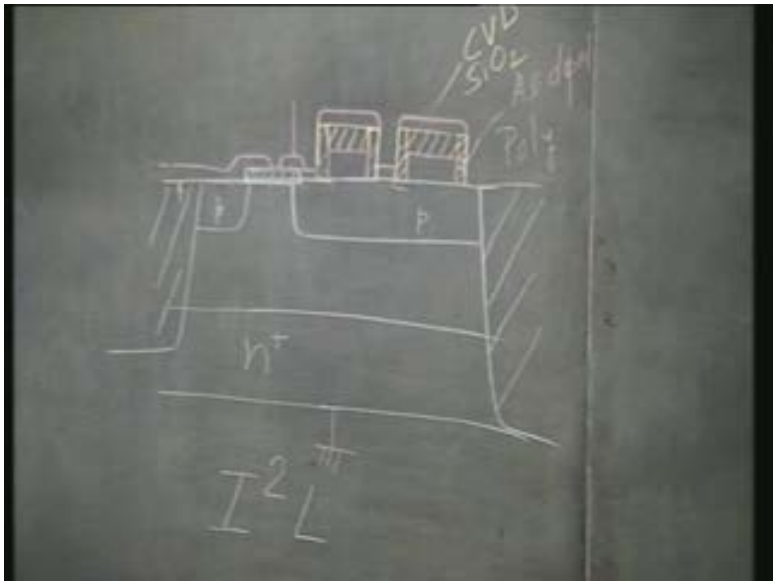

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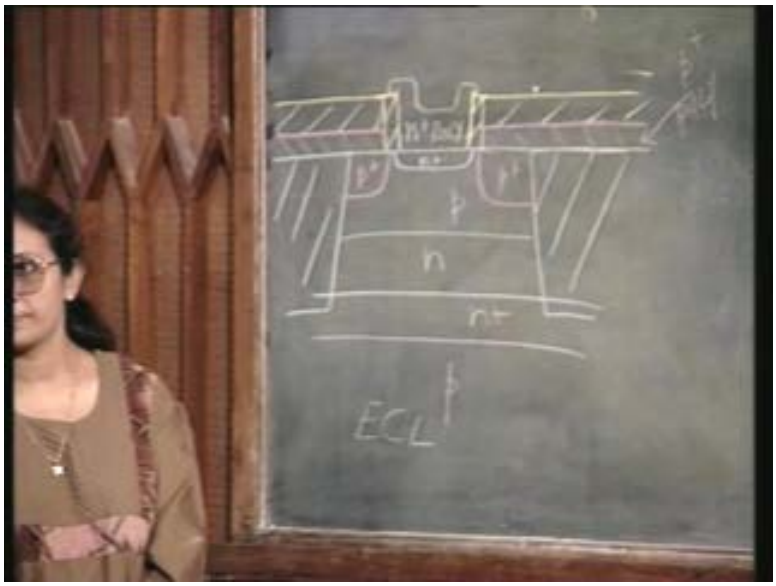

One is the self-aligned I-square L and the other is a transistor suitable for ECL applications. Look carefully. Don't you see that they share a number of steps? For example, this side wall spacer layer. I have a very similar step here, when I wanted to protect the n collectors from the base contact; same thing I had to do actually. This base p actually could be shared with these p's; they can be done in the same process steps. I could use this portion of the circuit in order to realize my I-square L, yes?

What I am trying to drive at is this. That therefore, I can think of a process flow which will incorporate both ECL and I-square L circuits in the same chip, because you can see that the self-aligned I-square L has a lot of steps in common with the high speed transistor, high speed poly emitter transistor. Many of the steps, you see for example, this poly deposition could be shared with this poly deposition, right. So, now you can think of a circuit which can house both I-square L and ECL. What is the advantage? See, ECL circuits are high speed, high speed circuits; I-square L is high density. So, you can have a circuit in which you can try to achieve a combination of both. You see, you do not want, you may not need the entire circuit to be very fast. You only want to hasten up certain bottle necks. So, in those bottle necks you put ECL, which will speed up. In the other portions, you probable do not need such high speed, you need high density; you use I-square L circuit for that. So, this is actually a very important technical, technological approach today. That is instead of having a particular type of logic circuit, ECL or I-square L, we can have a combination, so as to suit the various needs of my circuitry, right.

As the circuit becomes more and more complex, you have, you would see that certain regions is holding up the operation. I need high speed blocks for those certain regions. Other regions I need to have high density, low power dissipation. I-square L will answer admirably for that. So, more and more the approach is like this, if we can combine more than one technology in the same chip and that reaches its culminations when we can combine both the bipolar junction transistor and a MOS transistor, as happens in a biMOS technology. That is the final merger when we can combine both the bipolar junction transistor as well as MOS technology. Here what we are doing is we are trying to combine two bipolar logic - I-square L and ECL and we see that that is possible.

Next, we will go on to MOS technology. We will see how with more and more demands on the MOS technology, the MOS technology begins to approach the bipolar junction process that is a number of steps in a CMOS process flow is identical to what we normally we need for bipolar junction transistor and then thereby we bring about a merger of the two technologies which is the biMOS technology or biCMOS technology.

So, this is as much as I am going to discuss right now, about the bipolar junction transistor technology. In the next class we start with the MOS technology. First we take up NMOS technology, because NMOS was the prevalent MOS technology sometime back, till sometime back, 10 - 15 years back and now it is CMOS technology which has taken over from NMOS, because primarily of its low power dissipation and also because of the newer CMOS logic, the domino CMOS logic, whereby we can increase the packing density of CMOS also to a large extent. Previously CMOS used to suffer a little in comparison with NMOS, because you needed both PMOS and NMOS and as many p mass as there are NMOS.

The packing density used to suffer a bit, but now using the domino CMOS logic, we have changed all that, right. Still you need PMOS and NMOS, but not in equivalent numbers, right. So, the packing density has improved a lot and CMOS of course, it always holds the trump card that its power dissipation is the minimum. That is because in a CMOS technology, one of the transistors is always OFF; whether it is in logic zero state or in logic one state, one of the transistors is always OFF. So, at steady state, power dissipation is nil. Only when the transition is occurring from 0 to 1 or 1 to 0, only in that case, momentarily for a very short time, both the transistors will be ON and we will have power dissipation. So, the power dissipation of a CMOS circuit is actually its secret of success. You can put in a large number of transistors in a chip without having to bother about the power dissipation problem. That is what we are going to do next. We are going to discuss the NMOS technology, then the CMOS technology; then, we will see how CMOS technology is gradually approaching the bipolar junction transistor technology and how we can pack both in the same chip.