Digital VLSI System Design

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Lecture - 29

Synthesis Tool

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We were looking at ModelSim simulator and we were on the last leg of the same. We have been seeing, how to save the format of the waveforms that we have already created and in fact, we encountered it with little difficulty. I also mentioned that, it must have been saved elsewhere other than the current folder where we were working.

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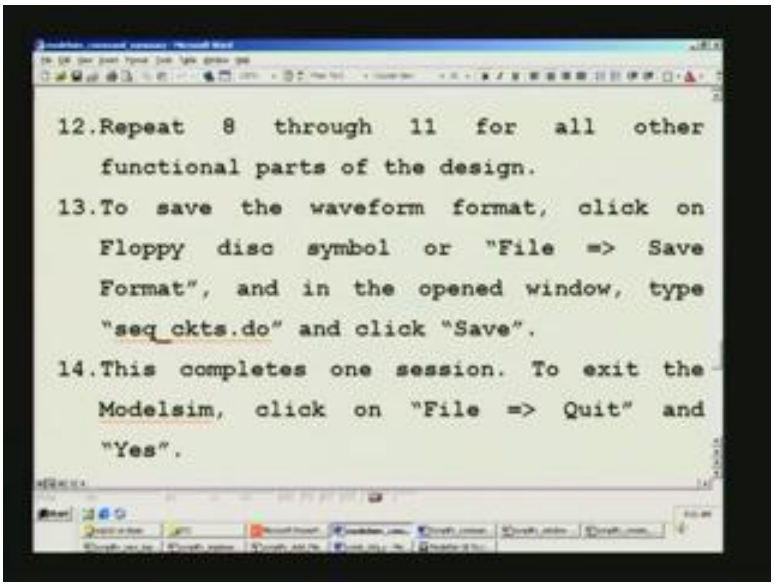

Let us complete that task before we proceed to synthesis. We were at this step 13: To save the waveform format, click on Floppy disc symbol or file, save format and in the opened window, type sequential circuits dot do and click save. So, it can be sequential circuit or any other design. Let us see what do we want to have?

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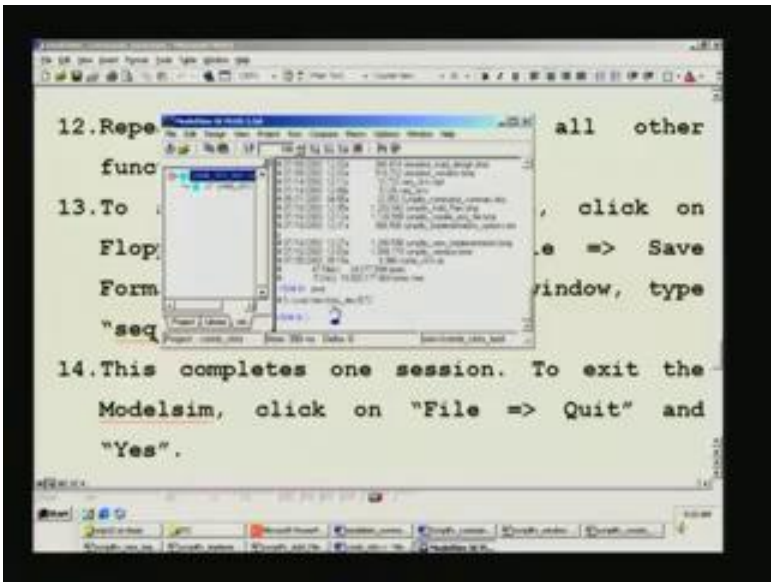

The ModelSim window is already opened and let us type pwd to see where we were. We were in d user rom dvlsi ETC folder and the files that you have here can be displayed by a command called directory, which you are already familiar. You can have a look, though it may be difficult for you to look here. These sequential circuits and combinational circuits are elsewhere. We will have to wade through this listing and it is here. We should make sure that, we are in library work directory. Let us first open a waveform.

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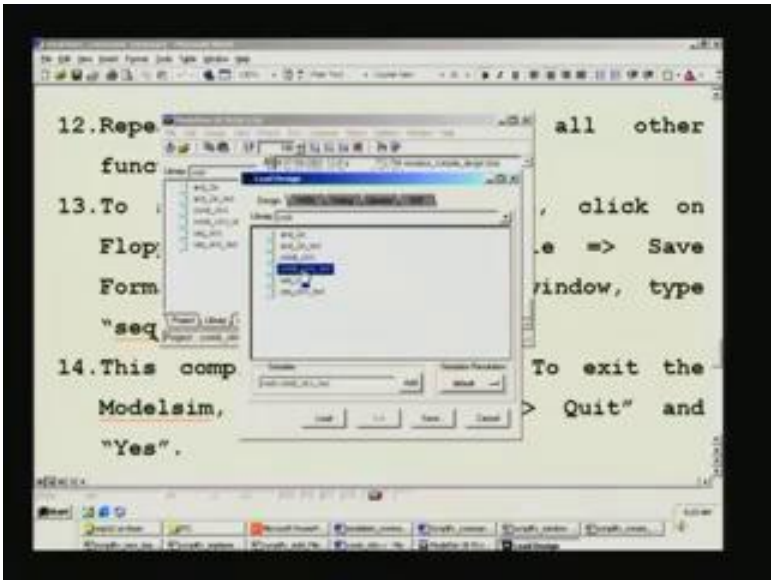

Before we open a waveform let us load the design. So, we see here a list of all the files that we desire. Being a simulator, we need to load the test bench as such and let us say, we want to load combinational circuits test bench. Double click on this and then press load and the design is loaded without any problem. The next step is to… we did not compile because, we have done it earlier. What all we have done is load design because, this is preparatory for saving the file in the desired format that you want and then to retrieve it at the next session to continue again after a break. We are precisely in that status now.

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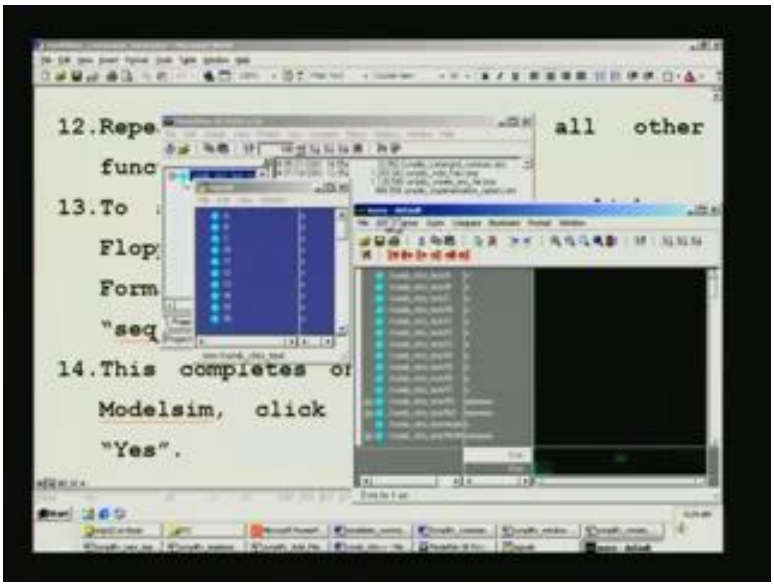

Now let us see what we have to do, we have to first invoke the waveform, use view then signals and all the signals are listed there and once again, view, wave, then the last thing of the menu, the signals in design will have to be clicked. A waveform opens and we no longer require these signals so we dismiss it off and we just drag it like that along with the partition. You see all the signals listed here and its corresponding status to a cursor position is displayed here and this is the cursor that you see here.

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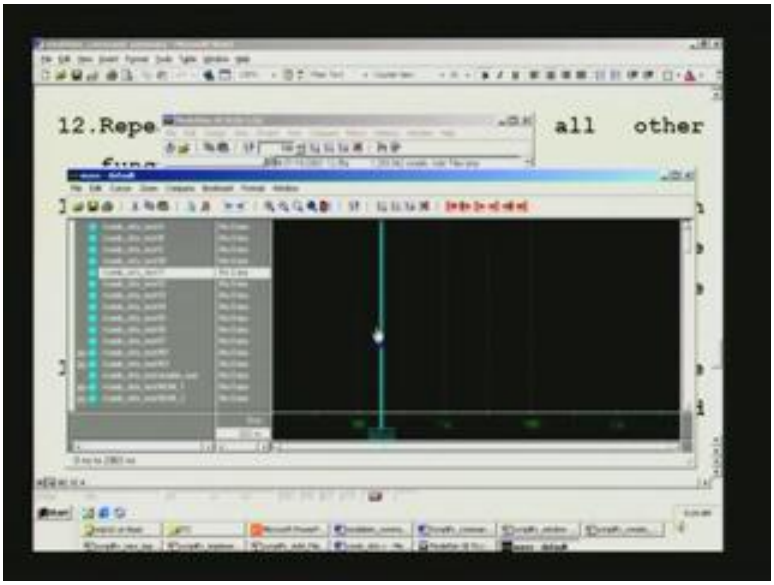

Let us see how to run, once again. This is run all command. If you do that it has run and displayed all the waveforms. It has also opened its source file which is combinational circuits test dot v and we do not require this as such, so we dismiss it off and we can zoom this waveform. We are trying to save this waveform but, before we save the waveform, we will just enhance this, make the signals apart from each other. For this you need, what is called format height and then you have 17 pixels which is the spacing of each of the signals and we will make it as 50 pixels and apply then and give ok. Nothing has happened because, I forgot to select some of the signals, let us select these signals, for example: a b c then i0 up to i2. I can use shift and then click and these signals are selected and to these signals, we are going to apply the format, which is height and enter 50 here and apply. Give ok.

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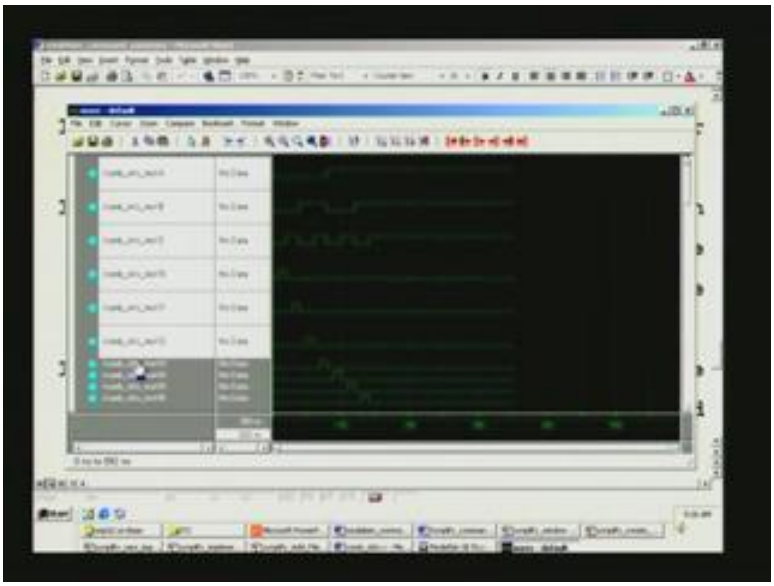

So, immediately you have you see that all those signals under question have been made different. Their spacing is different here; the highlighted signals alone and rest of the signals continue to be what they are. If you just drag this bar here, you can see all other signals below because there are innumerable signals in the design. You see a quite a lot of them and what we are going to do is just save this file and when you discontinue now and resume it after a day or two or even a week, you can always get back to the point where you had left earlier and that is what we are trying to do now. Up to a b c i0 through i2 only we have increased the spacing and the rest of it are all crowded.

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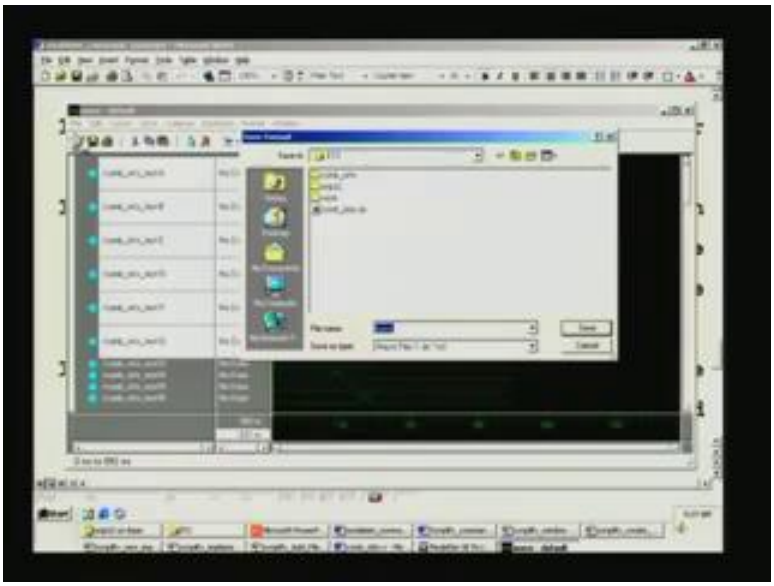

Let us save this file. I just pressed this floppy here or you can say file and save and it opens the same folder that we were in. Let us name this file as combinational circuits since we are working on that design. We also had to distinguish that it is a wave file and for which the nomenclature is dot do and it might take automatically since there are two options available called do and tcl, this tcl is normally meaning timing closure normally used in ASIC design. We are not talking of any platform such as FPGA or ASIC and let us save this as combinational circuit dot do. Remember we are saving in etc folder. See what happens, it says this combinational circuit do already exists. It asks: Do you want to replace it, if we had given some other name; it would not have asked this question since we gave the name which was already listed here. We just want to make sure that, we really want to overwrite it; otherwise the previous waveform that you had stored will vanish from sight. We are not interested in the previous waveform and it is only for a demonstration as such and we will just say yes. We have saved this waveform as combinational circuits dot do in etc folder and the job is done and we want to wind up the present session.

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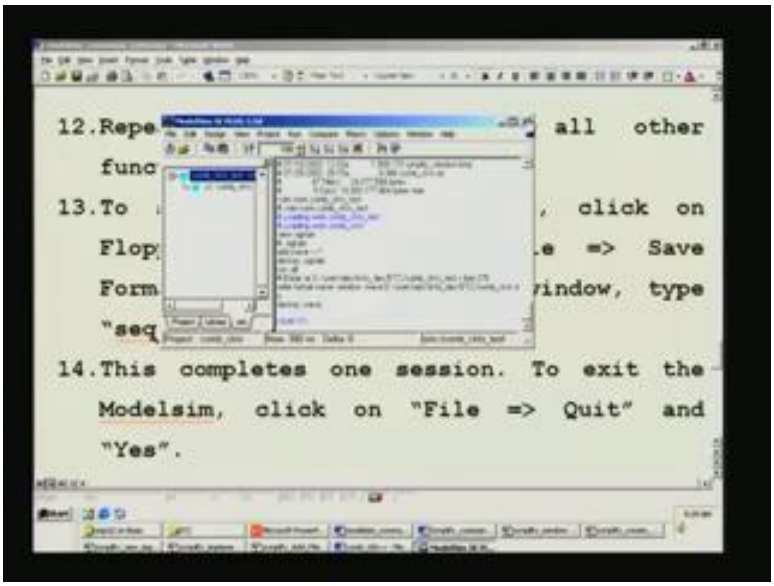

We just dismiss the wave and the ModelSim and see whether you are sure to quit. If sure, say yes here and as in step 13, save the waveform format click on floppy disc symbol or file save format and in the opened window type combinational circuits dot do and click save in this case.

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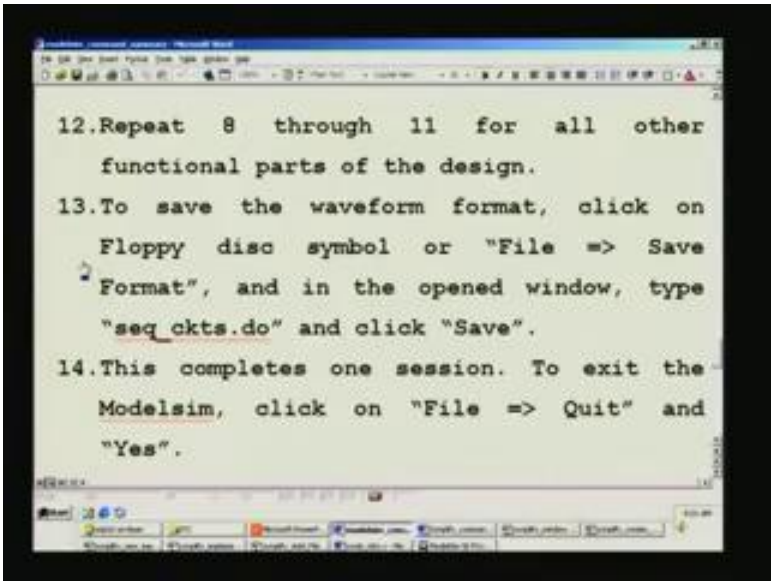

So, this completes one session. To exit the ModelSim, click on file quit and say yes. In fact, we have bypassed that and we simply pressed x and dismissed it off at one stroke.

Now next time, if you want to log in, use the same ModelSim simulator, you had to start with 15 and this can be after any period of gap.

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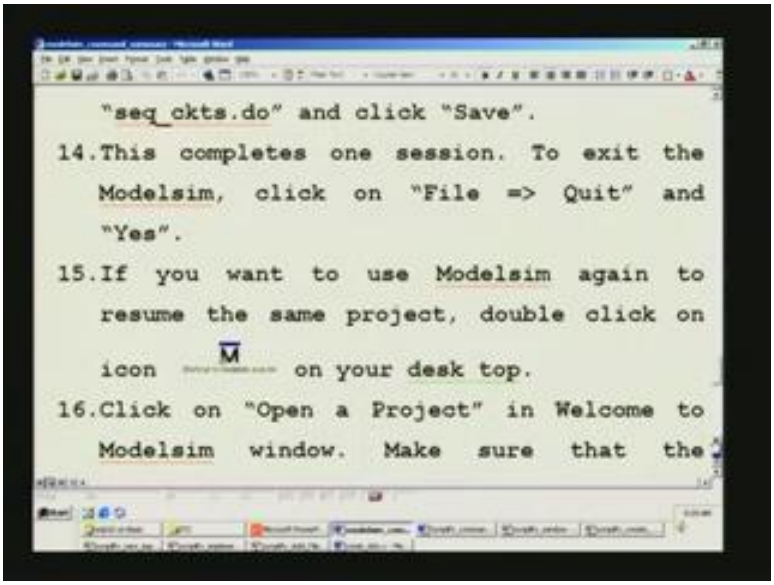

If you want to use the ModelSim again to resume the same project, double click on icon this is what you have already seen on your desktop.

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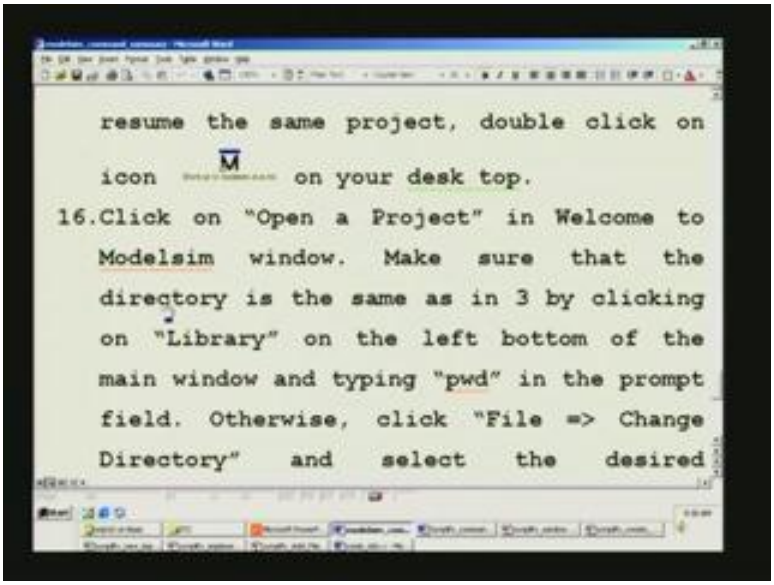

Then click on, open a Project in, Welcome window. Make sure that the directory is the same as in 3 by clicking on library on the left bottom of the main window and typing pwd, this also seen in the prompt field.

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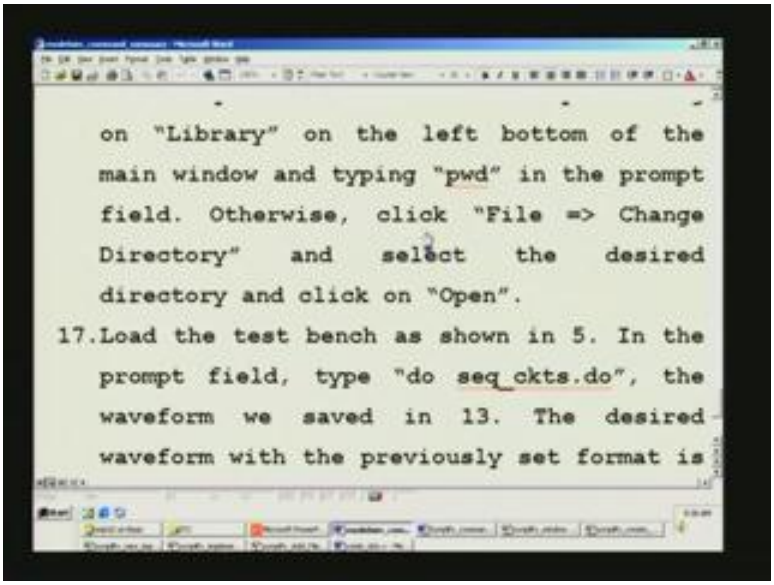

Otherwise click file change directory and select the desired directory and click on open. In order to change from one directory to another, suppose you are working in a particular directory earlier and if we wish to move on to some other directory, you can use that change of directory.

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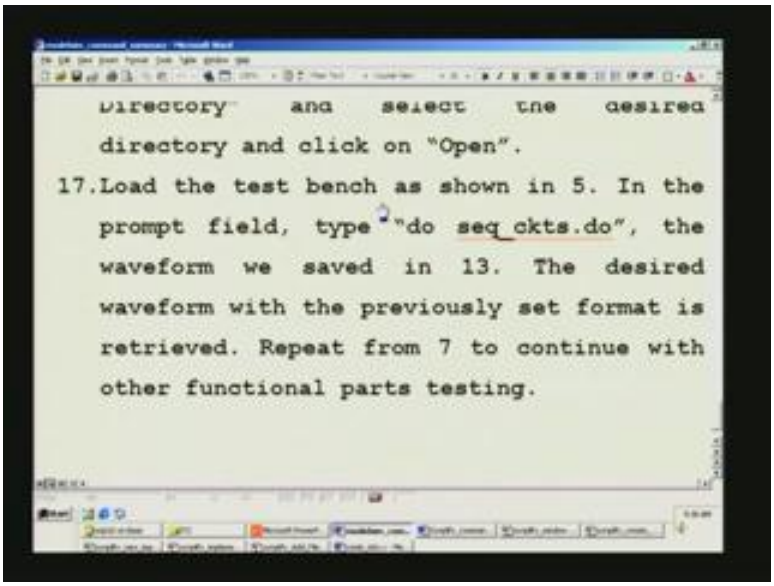

The next step is load the test bench as shown in 5. The goal here is to retrieve what we have saved earlier. For that, this 17th step is necessary. In 5, what we have is load design, which is the last step of the simulator and in the prompt field type after loading the test bench, say combinational circuits in this case, you have to say do combinational circuits dot do. This will load the waveform which was previously saved in 13. The desired waveform with the previously set format is retrieved. Repeat from 7 to continue with other functional parts testing. We could not do all the testing at one stroke in one session. So, it will have to be spread over several sessions and therefore you need to have a break periodically and then once you resume at any point of time, you can go through these steps. Let us see the real working of ModelSim, and now we see that there are no ModelSim because, we have already closed that window and we need to open that.

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We will dismiss off all the windows by this symbol and then click on ModelSim in order to initiate the ModelSim. So, that is the icon there. So it has opened ModelSim here and then say, Open a project. It says d users etc combinational circuits and say okay here and click on library and you have a work directory here and I will make this little bigger and you see that combinational circuits, its test bench and sequential circuits and its test bench are all listed here.

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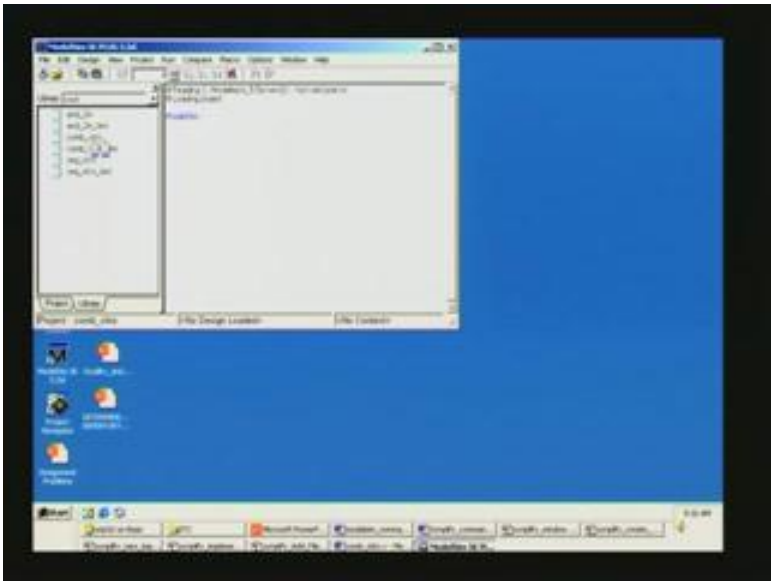

What that 17th step says is that, we need to load the design first, because without loading the design there is no meaning for loading a waveform. We will have to first do loading of the actual design. The design here is not really the design but, it is the test bench because we are using simulator. The top levels are always the test bench and not the design. As you are already familiar with loading the design, just click on load design and then double click on combinational circuits test and then say load and it has successfully loaded once again. Now at this step, let us print this directory to make sure whether the file we had saved is there are not. The combinational circuits dot do is saved earlier and this 7. 25. 2003, 9:28 and now it is 9:33. Just 5 minutes ago, we have saved this and that is reported here. We are now sure that when we invoke this should come. We have already loaded the test bench and now what we are doing is trying to retrieve the waveform intact. What we need to give is, combinational circuits dot do and if you just enter and see it opened the waveform as expected. Let us see, whether it has preserved what we have done earlier. Before you see that let me make it bigger, so that you can get a feel.

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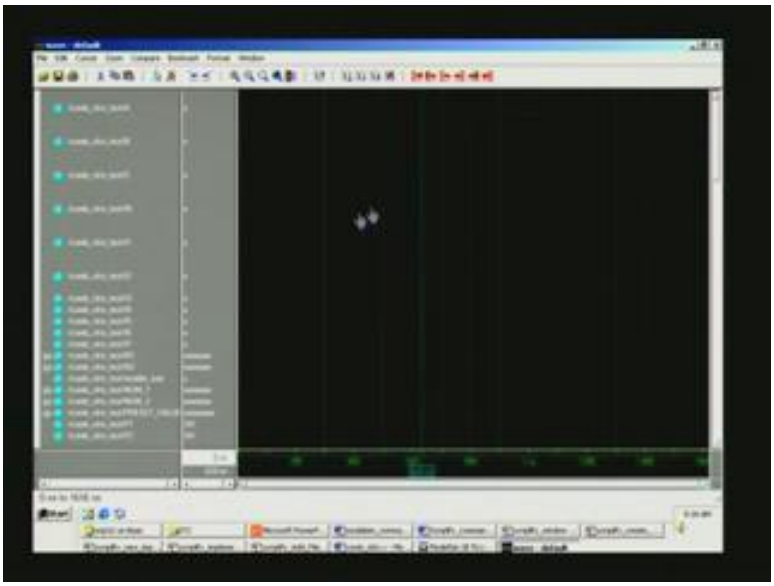

What you will be actually seeing on TV monitor is not the details but only the spacing. You can notice that a b c, I0, I1, I2. I asked you to remember up to I2, we had changed the waveform heights that is spacing rather and the height may be a misnomer and

probably must have mentioned it as spacing rather than height as such. Here you see I3 beyond are all very closely knit with each other and all other signals only here it is apart. That means only here we have retrieved what we have saved earlier and this will be a boon for people who cannot do all at one stroke from time to time and they may have to have a break. You have to resume again and therefore this will be very handy for you if you make it a habit to preserve this waveforms and continue from where you left. Next time when you start all over again for a new functionality testing.

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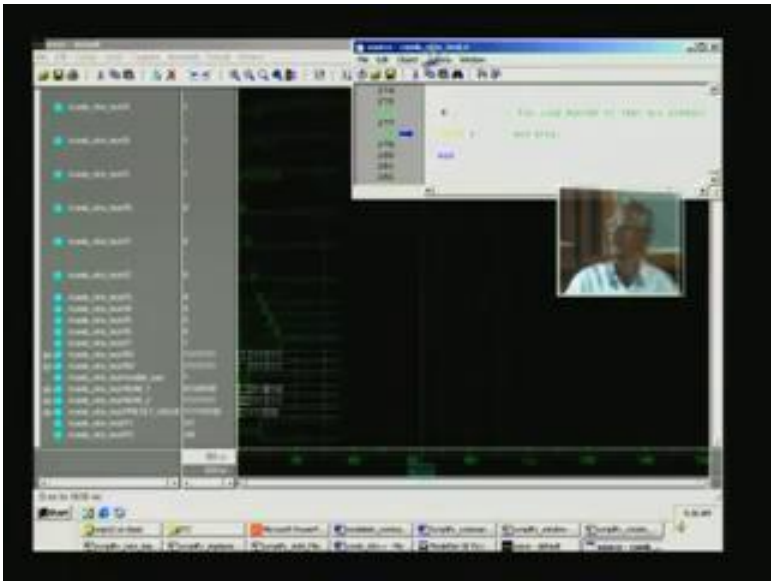

Now, let us run this here and all the waveforms have come and you can also see the source file invoked and it has stopped at the statement called dollar stop that is precisely what we wanted. It has just obeyed our commands and you do not need this any longer. We can just zoom in here and can see more details. All these waveforms are spaced and you can at least see this spacing here. These waveforms are all very crowded and you can see that it will be easier to see this spacing. Thus, we complete the ModelSim with this and we will go on to next tool called synthesis. Synthesis is being done here in this course by using Synplify tool and we will dismiss off this ModelSim first.

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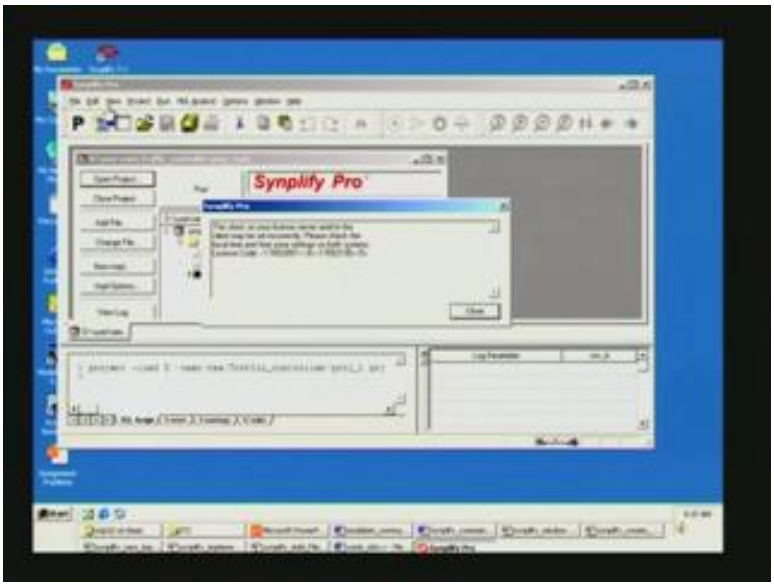

Here we have a Synplify pro and an icon which we need to double click in order to open the Synplify pro. It gives some complaints about setting because; the server is in some other building, not in this studio and we need not take special note of this. Some slight time difference is there. You see a window opened, total window. We will have a painted zoomed version of this and there is a window here where you can see and read this Synplify pro and perhaps run, some open project, close project add project add file, change file. All these details will go on step by step and finally, view log and there are more commands below, you will be seeing next. Before that, we will just see that this is the basic Synplify window is this and I will just zoom here. Once again this being paint, it looks so real that one may be tempted to click here, but it has no meaning. If I click here what I will get is only a line because, I have copied that window in paint, as I had done before in the waveform. It will work right on that periphery, this is the actual paint window and those commands will work using view here, then I will zoom, say custom and select 200 %. If I say OK, it will zoom in that particular window and the whole window is zoomed here so that it is convenient for you to have a look.

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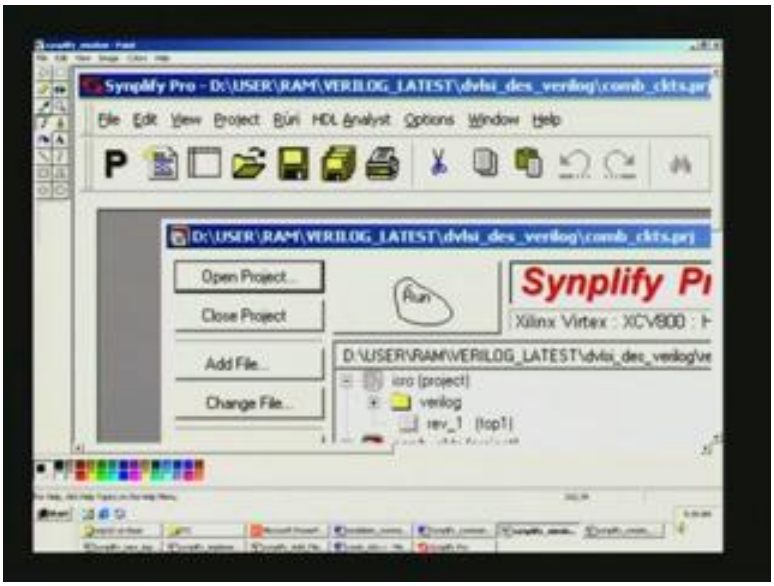

You can see file, edit, view, and project, we will see one after another later on. P stands for the project and this is saved like any other windows format and scissors here for cut and so on and you also see here a directory.

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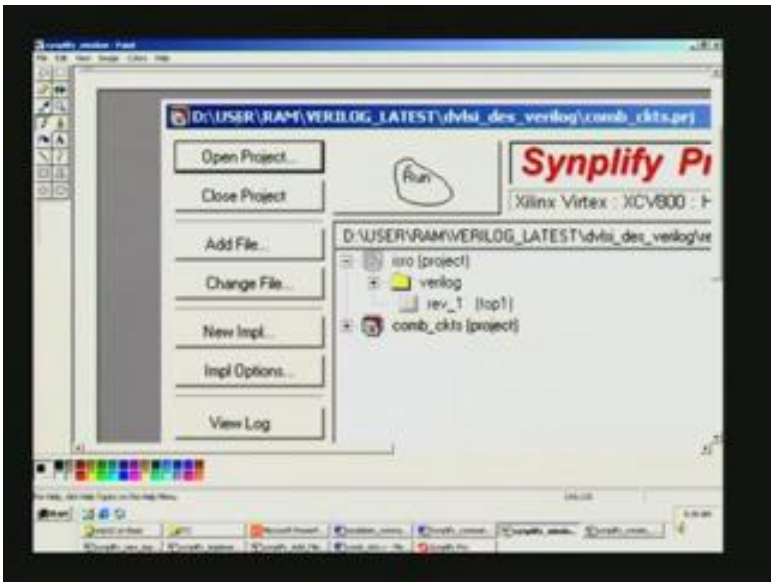

We had to deal with what are known as projects and we had to name a project, as we have done earlier in ModelSim. You can open a project through this or close it, add all

the files belonging to a particular design by using add file and you can change the project file if you wish. Suppose you want to change from one device to another, once we say it is Synplify, we are not in the realms of ASIC design, but only in FPGA design. This Synplify supports all the devices in the world; we will shortly see the devices that it supports. We also have some log file which will report what is happening during compilation, during mapping on to a particular device and so on.

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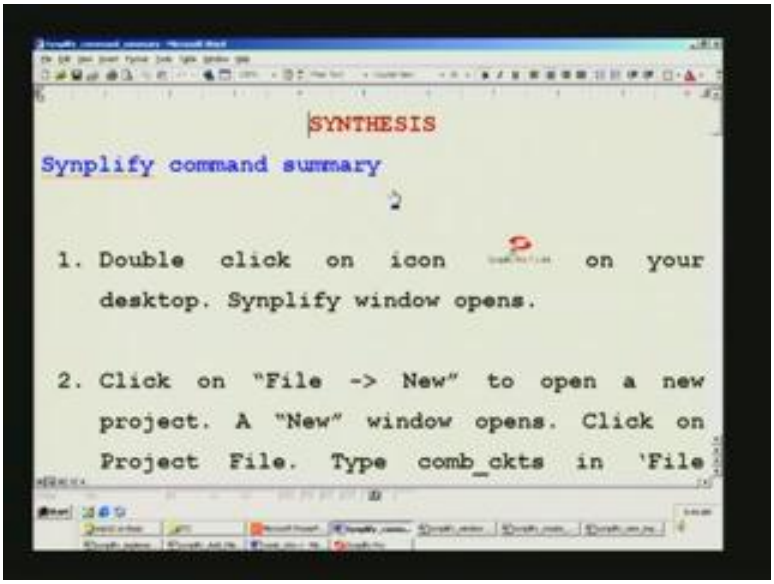

We will first see that the Synplify invocation as such, with a double click on icon Synplify pro on your desk top and then Synplify window opens. This is what we have already seen and window has opened. Next step is, click on file and new to open a new project and a new window opens, click on project file type combinational circuits in file name field and also type the desired file location where, you wish the new project to reside. Click on okay and the project window opens and let us see zoomed version of the window which we have been actually seeing and that is what we have here.

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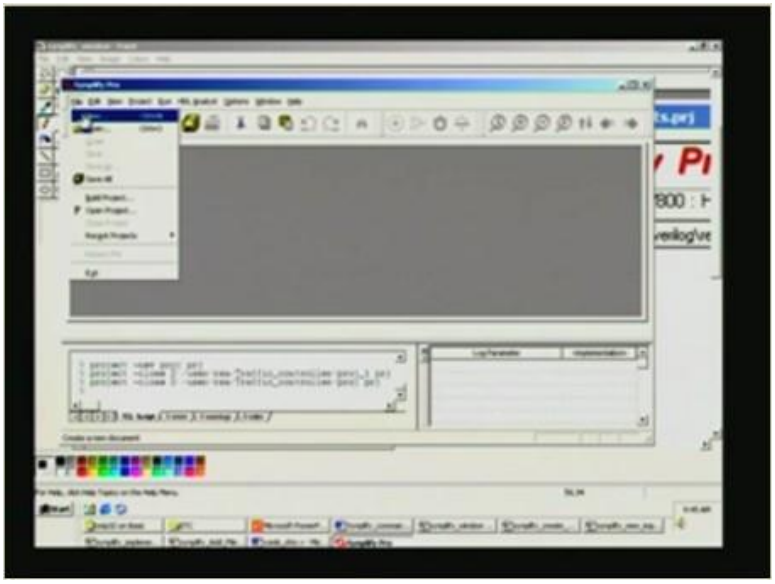

If you click on this file here, it will open a new window and we will actually see how it does. Now see a file here, there is a new menu and let us click on this. It opens a project file and let us click here. For this also, I have a separate window zoomed and let us have a look at that.

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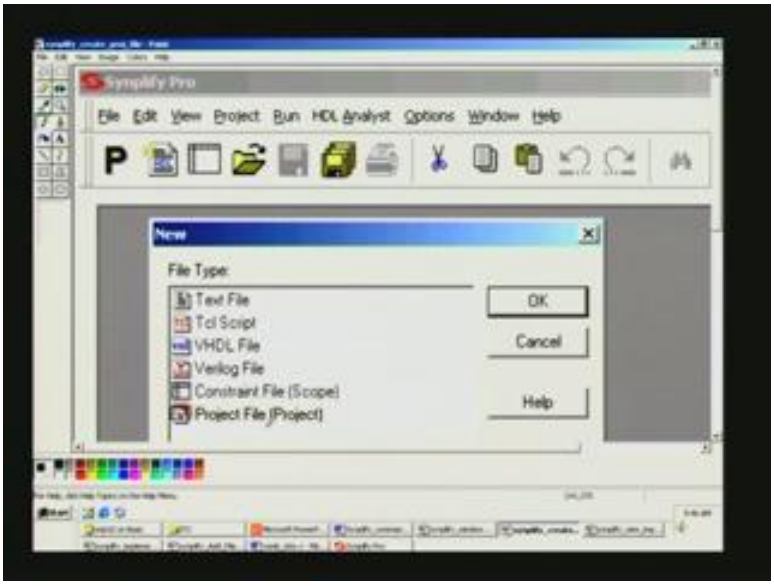

The zoomed window is here and this is the actual a Synplify window and within that there is another window here called the new because we wanted a new project to be

opened. It is already clicked and it is highlighted and once you click here, you can put the project name you want to give, for example this is a combinational circuits.

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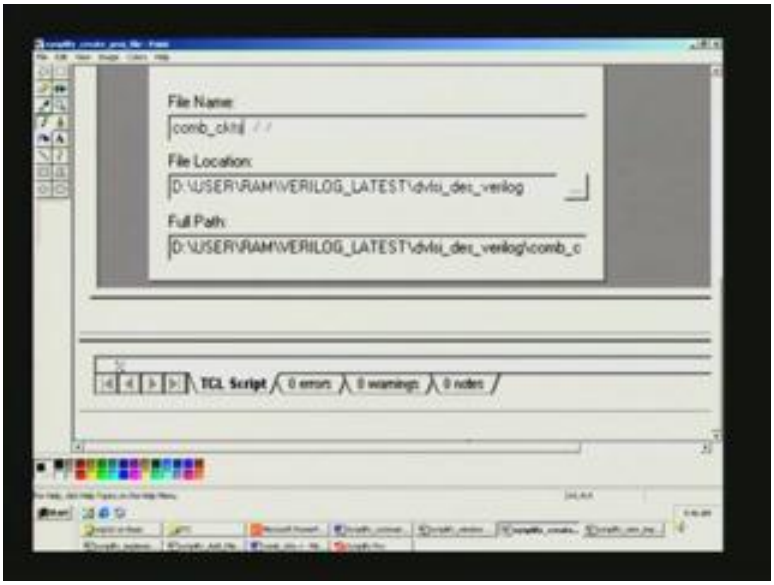

So, you give a combinational circuits typed and the location where this should be located can also be given. This is in one of the places here and you can change that if you want by clicking on this. The entire path plus the combinational circuits appear and you can see that combinational circuits are here. So, this is the window for new project and this is the actual Synplify pro, this is the project file and we will just type prompt circuits.

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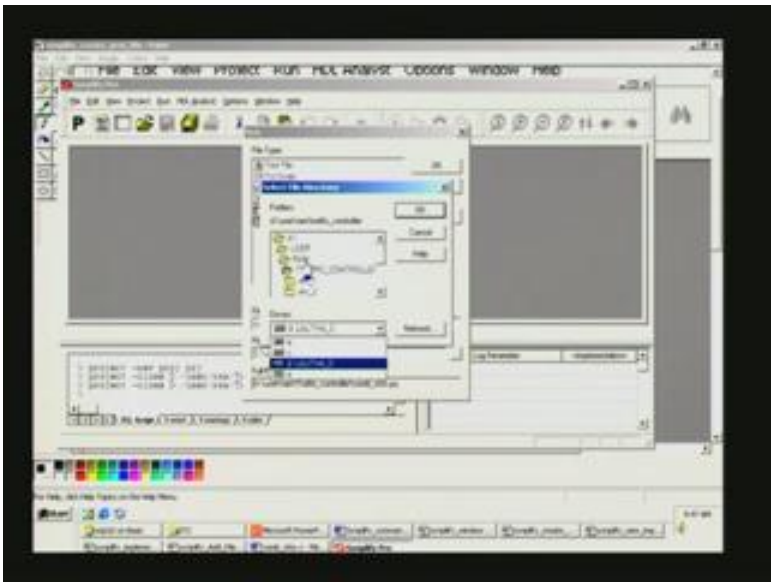

If we do not want this directory, let us change the directory we are interested in. We will locate our files in etc and now it will open that there. You see that, the etc path is shown and file name you have already given there is reflected and the entire file name with a full path is mentioned here. Note that the combinational circuits automatically put an extension dot prj and to indicate it is a project and all these things are to our requirement, we just say ok. Now you see a window opened here and you see some other menu here and we will just stick on to our outlined summary here.

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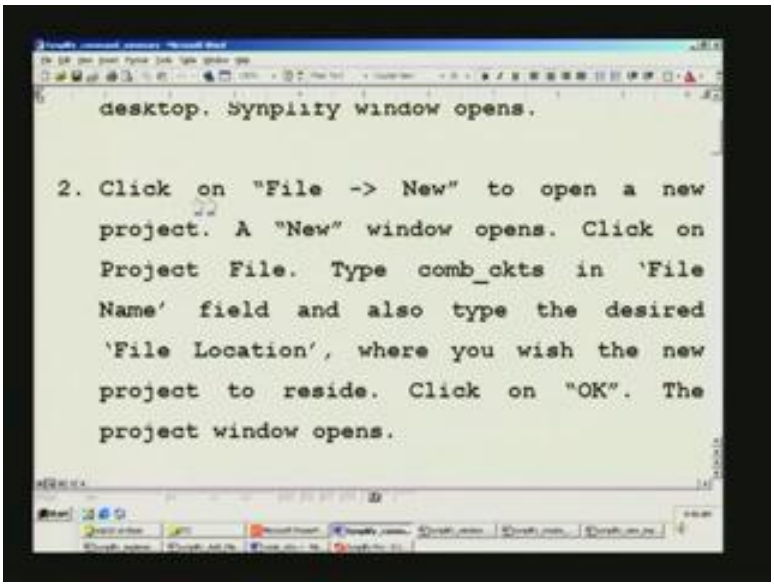

So, what we have to do is click on file new to open a new project, a new window opens. Click on project file. Type combinational circuits in file name, field and also type the desired file location where you wish the new project to reside and click on ok. The project window opens and that is what we have done.

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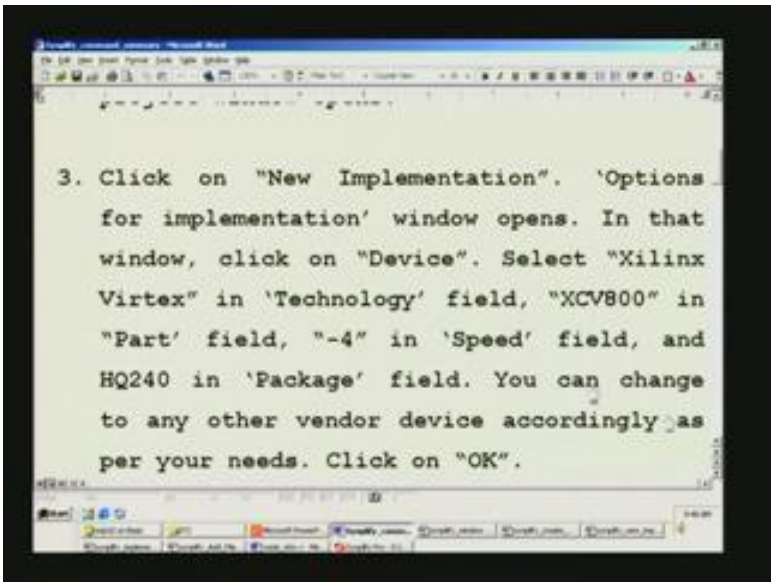

The next step is we will go to a new implementation. Let us go to this real window and see what it says is it is in etc and it also gives a revision number. Notice that, each time we are working on the same project but perhaps on a different device change from one vendor device to another. In that case what we need is to keep track of the revision number. Otherwise your previous results will be overwritten. This tool is very handy which takes care of this and by each time it gives a new revision number. Prior to going through Synplify pro, let us see what features it has. We are looking at the revision one, emphasizing the need for keeping track of different revisions so that, we do not overwrite the same results by mistake that we have already gathered. Before we go into the details of Synplify pro, we will first see what its features are. Here, we have already mentioned that, we are using a Synplify for Synthesis.

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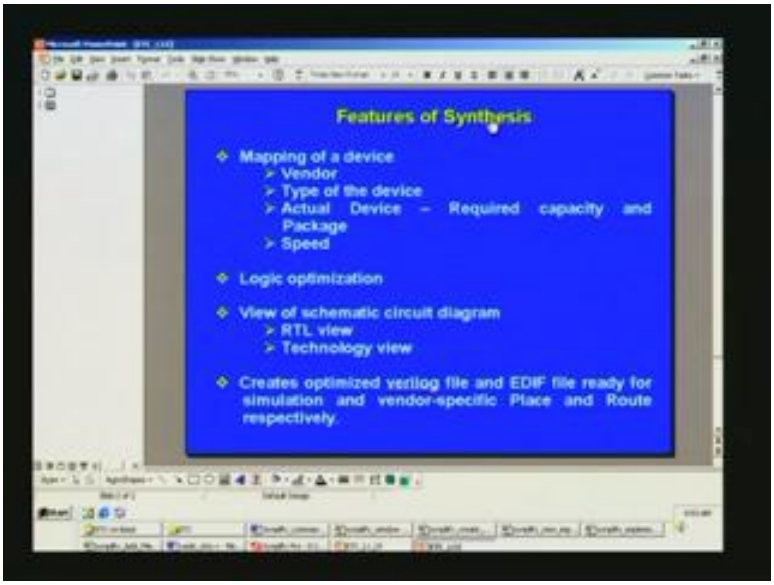

Let us have a look at what Synthesis is and what it can do for you and then let us have a look at all the features of Synthesis. In fact, this is applicable for any Synthesis tool, whether it is Synplify here for FPGA or ASIC field and we need synopsis and so on. This is the listing for the Synplify, making use of FPGAs. All these are the salient features for Synplify tool or any other Synthesis tool such as Leonardo spectrum as well. To start with, what we can do with this Synthesis tool is that we can map it on to a particular device. Once again there may be so many vendors then you may have to choose the

vendor. In this particular tool, there is no specific selection for the vendor but, there is only a direct selection of the devices of all the vendors and the devices that they support. In FPGA device, there are so many devices and the types of them you can select here and within this type, there may again be several devices and each device may have a certain capacity. Some of them may be 5000 gates; some may be 50,000 gates, some of them 1 million and some others, 3.6 million gates and so on.

So, depending on the capacity, they have a different device and it carries a certain device number by the vendor. These are all the vendor specific, required capacity and the package can also be selected in the sense just like you have ttl packages, dip packages and you have so many other packages as well. Many other packages and many pin configurations each of which will have specific name or some symbol to identify and we will see how they are identified. Basically, they give the number of pins as well for the package and these are all the things that you can select from the menu of the synthesis tool especially that of Synplify. Once you have selected the device, there may be several categories of speeds available for the same device and it may go under an extension of the number say dash 4, dash 8, and dash 1 and so on. That indicates the speed of the device that we are handling. In one vendor platform one may mean the highest speed and in another vendors' platform it may mean the reverse. That is the lower speed. We have to look into the vendor specification sheet in order to ascertain what that particular number means. This is the first step that we have in a synthesis tool and next very important thing is logic optimization. So, this is what you have already done manually by using k map, Queen Mccluskey method and computer aided algorithm and the number of variables are beyond 6 or 7. They are also (30:55) algorithms and using cat tools, logic has been optimized (31:05).

Similar such things happen in synthesis tool as well. Once you have optimised, you can have a view of that schematic circuit diagram. There are two views as such; one is called the RTL view which you are already familiar. It stands for register transfer level and we have seen earlier guidelines for the same and that is normally the RTL view that you will have and another important thing in this is that, we need to know beforehand what we really want. See for example: I want details of the actual primitive cells used and then

you may have to go for next view called technology view. We will see all this in detail as we go on. You can study the schematic circuit diagrams, we will go into details of all this and then see whether it has really done the optimization and whether it has mapped it on to the desired device with the requisite capacity or speed and so on. Also it creates optimized verilog file and once you have optimized, what is the guarantee that your design is not over optimised in the sense that, it has not sacrificed some of your signals or the functionality. There is no guarantee. The proof of the pudding is in its eating and here you had not only view and analyze and also create a source file which is once again the verilog file, after optimization is done. So, this synthesis tool automatically creates optimised verilog file and it also creates an output file called EDIF file this is an electronic data information format. This is a standard format, which third party vendor will always stick on to some standards. This file can be exported to next tool which is normally from a different vendor.

For example: you can use this EDIF file created here using the synthesis, corresponding to your design and that can be transported to the place and route platform. For example: you can go for Xilinx place and route in the next step that you will be taking in future. These are all the two vital things that we need and this EDIF file will contain information about the actual technology cell used in the FPGAs and which was mapped by the synthesis tool. It creates optimized verilog file and EDIF file ready for simulation. Notice this verilog file what we had created after optimization, can be taken once again to the ModelSim simulation and verify whether the functionality is intact or not. That is what we meant earlier here and this is the way to guarantee that, your basic design has not changed functionally although the tool has optimized your file. Only the optimized file will go on to the next stage of place and route such as Xilinx place and route via this EDIF file which will be created along, when you synthesize. We see that it creates optimized verilog file and EDIF file is ready for simulation and vendor has a specific place and route respectively. So, this EDIF file is for the vendor specific place and route, as we have already seen, such as Xilinx.

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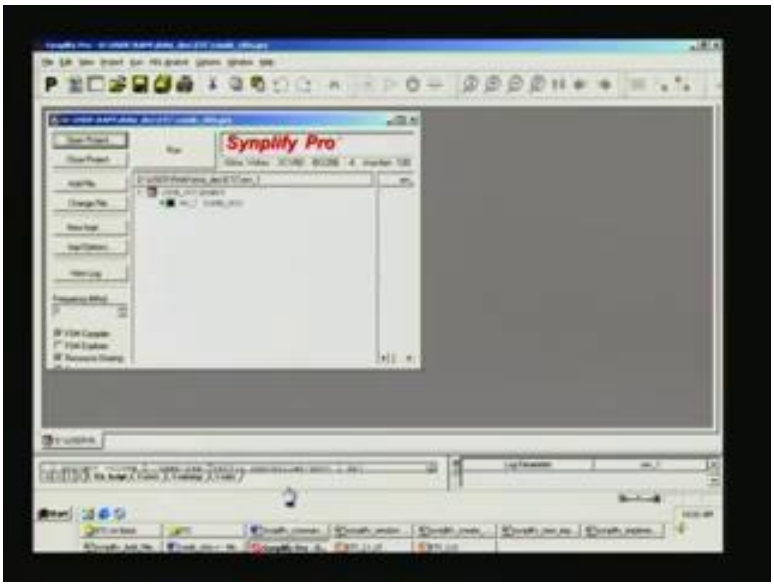

We will go back to the Synplify pro and resume from where we left. We have created combinational circuit project and it is ready for the very first synthesis and it is reporting revision 1 as a combinational circuit which is your design. We will once again go into the actual command summary of Synplify to invoke the synthesis.

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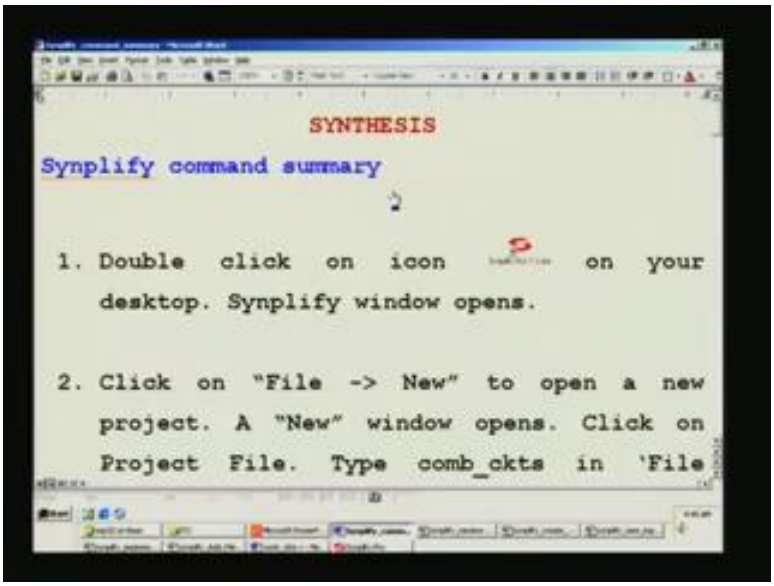

This is the Synplify command summary.

We invoke by double clicking on the icon and then we moved on to creating a project file. Now, we are on the step 3, which says that: In the new implementation, we can select a specific vendor, device, speed and so on that is precisely what we are going to deal right now.

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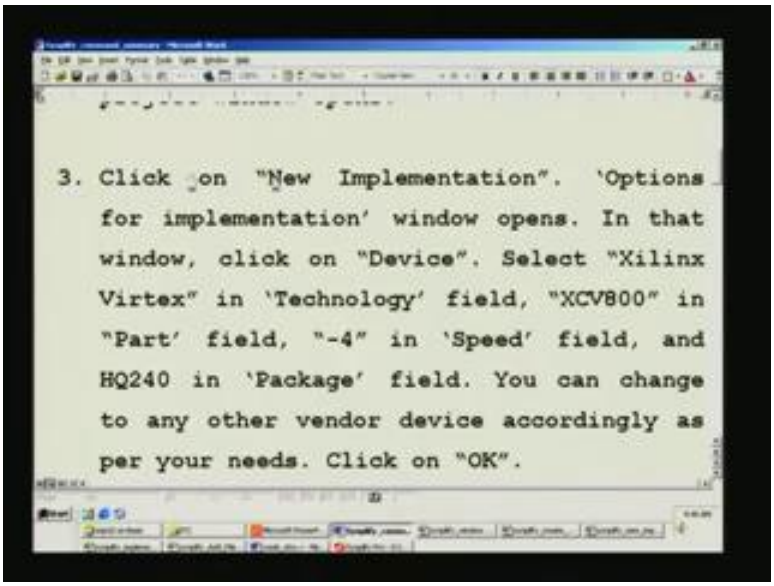

So, let us read on this and then look at the corresponding windows. Click on new implementation, options for implementation window opens. In that window click on device and this is what we meant by device selection and it has whole list of all the devices and categorized under different vendors. By looking at the device, you can easily make it out who the vendor is and let us say, we want Xilinx vertex, this is the latest in Xilinx vertex and you can choose if you wish, select Xilinx vertex in technology field and this is the actual device xcv 800 stands for x for Xilinx and v stands for the vertex c I am not sure may be a commercial device or whatever, 800 stands for 800,000 gates that means, in one FPGA you have total of 800,000 gates plus and some more rams are also available in addition to this. We also said, we need to specify the speed and there may be several speeds. Let us if say dash 4, it may mean a particular speed and what exact speed it is we will have to infer only from the vendors data specification sheet. We also said that we can select the actual package.

Here, hq is one of the packages and it has 240 pins totally, all ios then ground vcc all those pins clock and rest of it all put together is 240 pins. So, we need to select the package that is what written here in package field and you can change to any other vendor device accordingly as per your needs. Depending up on your actual requirement, your customer requirement, you will have to select that particular vendor device, speed and specific device. Once you do this, just click on okay and let us see how it is. So we are in new implementation so let us open a new implementation window here and we will zoom this.

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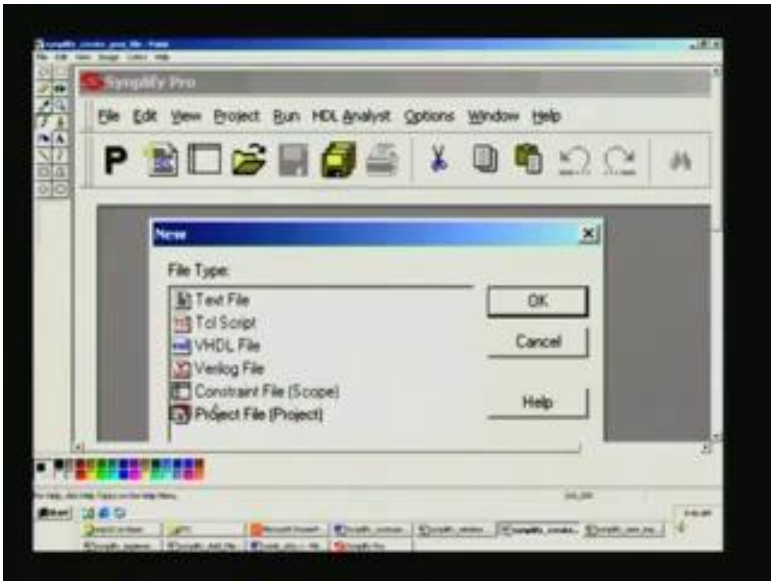

Once again you see the Synplify pro window and there is another window. This is the actual internal main menu and to add files and so on and the window of interest is this: options for implementation.

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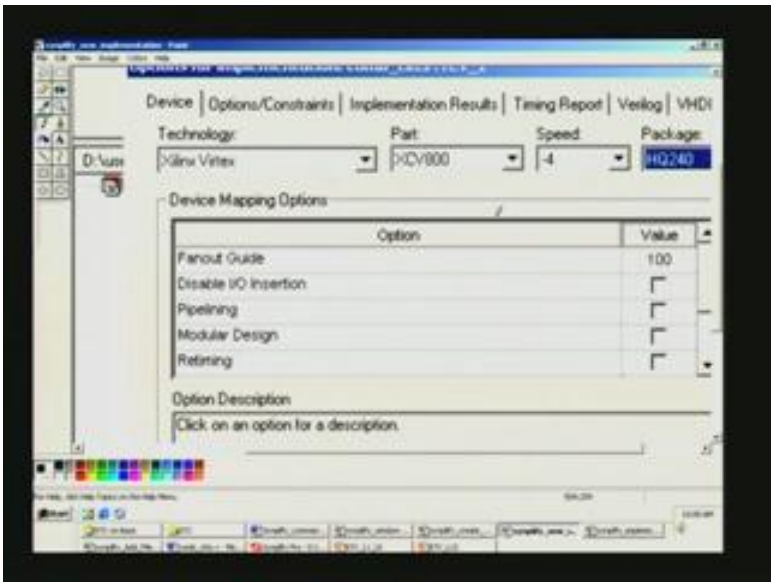

You see that, there is a technology menu here and if you click on this, you will get all the mean vendor devices here listed. Once you select particular device and that will appear and here in this case it is Xilinx vertex that have been selected and so that is reported here. In this we need to go for a specific device, let us say xcv 800 as we have seen before. So, once again, if you click here, it will list all the devices under this type and you can choose any of the devices that you really want. If you do not select anything, the tool itself will put some xcv 50 as a default and later on for small designs that 50,000 gates would be adequate and for bigger designs you may have to move on for even several million gates here.

Depending upon the application, as we progress, we will see how many gates a particular design has taken later on. Once again for speed you have, you can click on this arrow here and it will list all the speeds available for this particular device and you select only that and then again you have a package here. You can use this arrow click and get an assortment of packages available for that particular device and also the speed where you can select from one of them. There are more here for the time being we will not ignore this .So, this is the option for implementation and we had clicked on new implementation and we selected all the package, speed and so on. Before we go on to next step, this is

fourth step where in you add your design files. Before we go on to that, let us execute what we have already learnt in the previous step.

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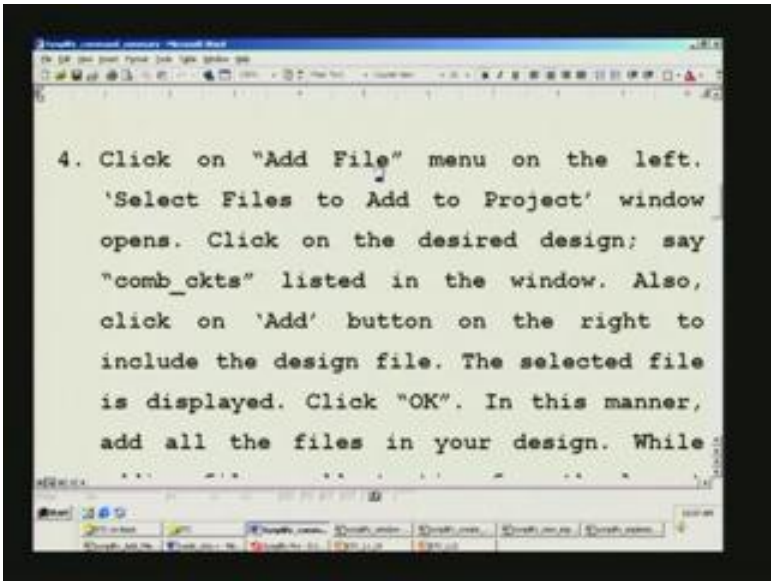

So what we did is we have already selected the project file and we need to select a new device. For example: as a default it has selected Xilinx vertex xcv 50 and package is bg 256 and dash 4 for the speed and maximum fan out also it gives. Fan out you know from your ttl fundas and that it is number of ttl loads which it can collect to an output of a gate. Here, in this case fan out refers to not a ttl gate but, the gates pertaining to this particular FPGA primitives or what you call cells.

Now, let us say, we want to change to some other device. Let us click on new implementation here and once you click on the same window, it has opened and you see Xilinx vertex here. You can see quite a big list. In fact, it is almost an exhaustive list of all the vendors in the world. So, for example it says: actel, which is an FPGA manufacturer, ultra and then Xilinx, so first it lists all actel here and within this one type of device is also listed here, for example: 3200 and 40 mx and so on act 1 act 2 act 3 and actel ex pa, all these are applicable for actel. Each of this series will have in turn a number of devices, as we have already explained earlier will also have to be configured here.

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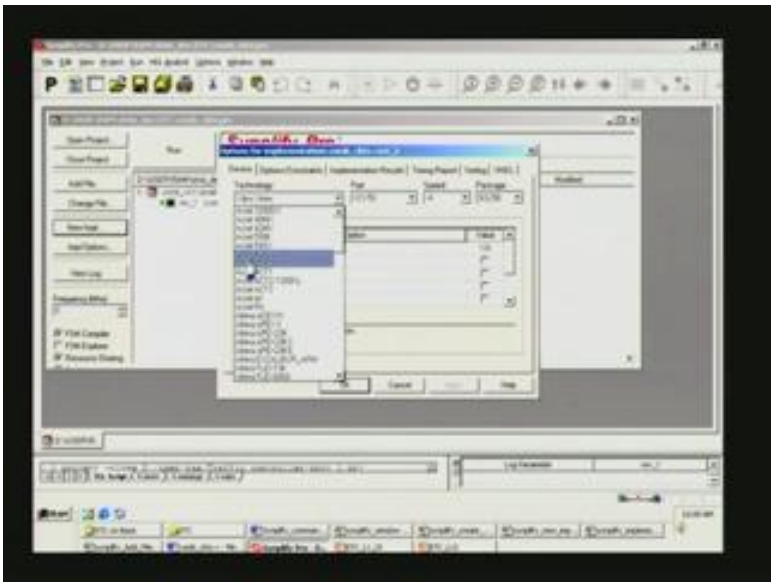

So, what we are right now doing is primarily selecting the vendors type number and if you go on to next vendor, say you have ultra here some apex 20 k and flex 10 k and flex 8000, 6000, 3000, 7000, 9000, and so many series they have. You have another vendor called atmel and atmel 40 k series which is of course short listed. They have only just three of them. You have another vendor called syprus and they have again four such entries and each of this stands for the type number of the device not the actual device. Within the type number there may be many more devices depending up on the capacity that is gate count. In addition to that another vendor called lattice which may be loosened technologies arcas series then you have one more vendor. There are over a dozen varieties of types they have in lattice. There may be a ten numbers available here. All the different type numbers are there and then later on trison some 2 are there. Finally Xilinx, you have a quite a plenty here, major types are Spartan series and its varieties. We have already seen Xilinx vertex here and there is one vertex 2 and 2 p also. The latest one is vertex c and there are other Xilinx versions say xc 3000, 4000 series and so on. Normally, these are all lower capacities. So, then you have 5200 series then 9500 series up to that it is quite a long list in Xilinx. Let us say, we select the highest speed which is the Xilinx vertex e, we will click on this vertex. Earlier it was Xilinx vertex and now we have clicked on to Xilinx vertex e and we have selected the particular type of the specific vendor Xilinx.

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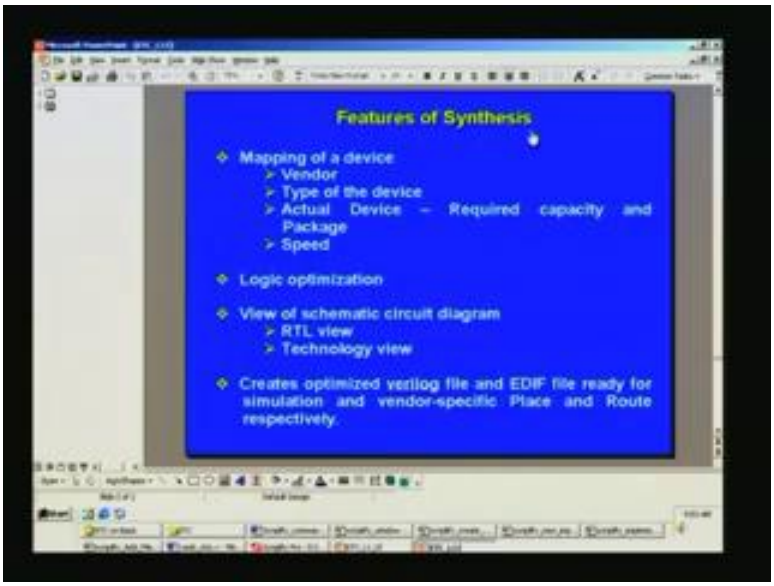

We saw that vendor and type of actual device, the package and then speed. The next one is to select the particular device. Once again, if you click here, you will see a list here which is xcv 50 then 100. 50 stands for 50,000 gates and plus RAM will also be available here. From 200,300,400 and so on it goes right up to 3,200 here, vertex e has 3200 device currently. In future higher density is sure to come for that matter for any other vendor. Perhaps Xilinx has the highest capacity and speed and closely followed by ultera. There are so many devices which you can select. This design does not demand much. So, we can select either 50,000 itself is very high at random and we select 600. There is no compulsion that we should select only 600.

Now, we move on to the selection of the speed that is listed here and right now it is shown as minus 8. Let us see what other are there and here you have 8676. I think in, Xilinx a higher number stands for the higher speed and perhaps this is inverse notation employed in ultera which is probably higher number lower the speed. The best thing is to verify by referring to the data sheet of the specific vendor for that particular device. If you do not look at the vendor data sheet, we can get by running the synthesis tool and looking at the report and see how much speed it has offered. From that also you can make it out this is higher speed. So, let us for the time being map it on to minus 8 and then comes the package and you see bg 432 here. It has once again a number of them here and

we select just 240 pins because, we do not have very many ios and let us remain content with just 240 pins. You can notice that 900 pins are also available here and many other pins 4 32 and so on. Let us select hq 240. What we have done is select vendor and its type number, the specific device, the speed and the package. Once you have done this you can just say ok. Once you did that one because, we selected it, earlier it was there in revision 1, it has automatically gone to revision 2 because, you had used this revision one earlier which would be overwritten by the new device that you have selected .That is the reason why it safe guarded your investment by having a separate revision as such. What we have seen is zoomed version here, where you have seen this modified Xilinx vertex. It has been selected dash e and then the device selected is 600 there. Again, I think dash 8 and the package is precisely the same.

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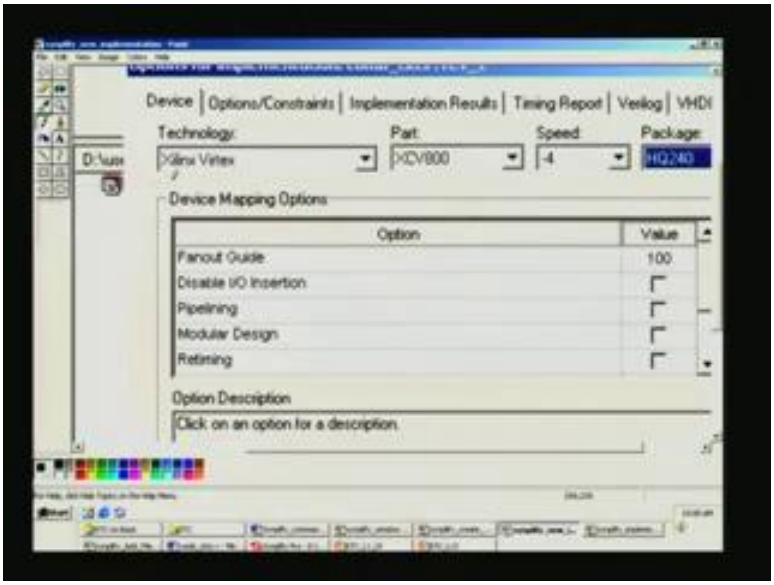

So, we have seen options for new window. Similarly, you can have another window which is precisely the same here.

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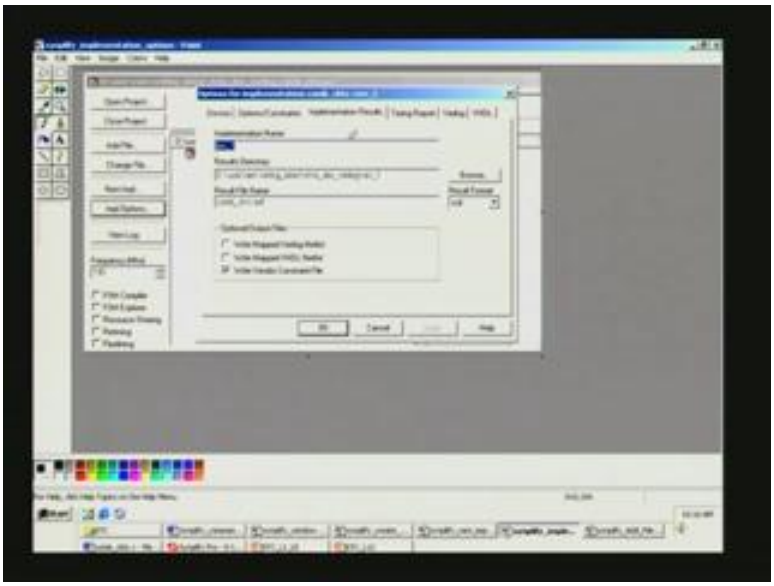

You had gone for implementation options instead of new implementation and you would have got the very same thing here. So far what we have seen is, Click on new implementation options. The implementation window opens, in that window, click on device select Xilinx vertex in technology field, xcv 800 in part field, then dash 4 in speed field and hq 240 in package field. You can change to any other vendor device accordingly as per your needs which we have seen already and then finally we click ok. Then it has accepted that and formed a new revision as such and we will continue with this in our next class.

Summary of Lecture 29

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Next lecture

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