Digital VLSI System Design

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Lecture - 27

Analysis of Waveforms Using Modelsim (Continued)

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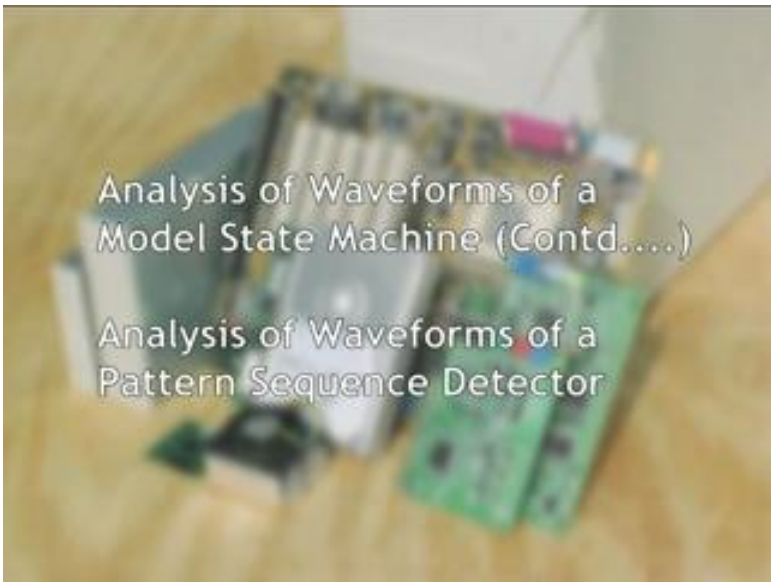

We were analyzing waveforms for state machine earlier and we had also seen parallel to serial converter in which we had missed two of the waveforms.

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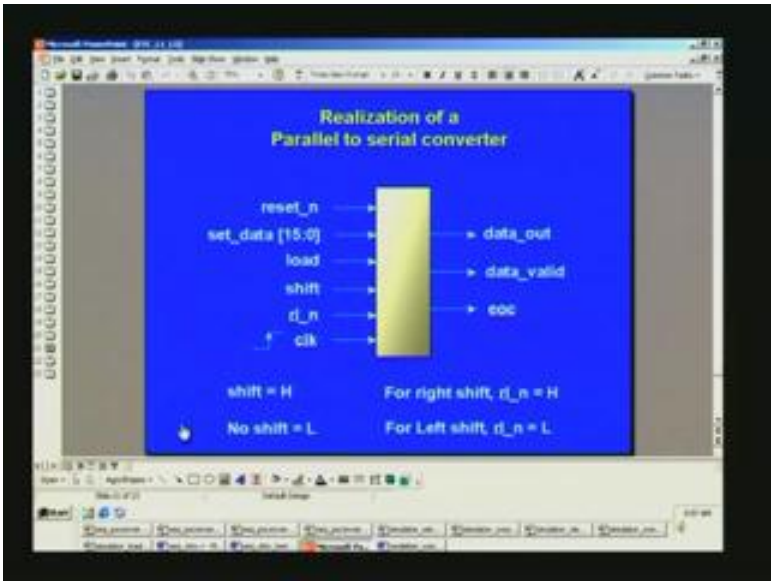

First we will cover that before we resume state machine. Just to recollect what parallel to serial converter is, we have a reset, you can set data through this and asserting load; thereafter, you can give a shift control and this shift can be either left shift or right shift,

this being one for right. It is being reckoned at the positive edge of the clock. You have an output corresponding to the serial stream, bit stream as such, right at data out and when it is valid will be indicated by this data valid signal and once all the 16 bits are sent out serially over this, an end of conversion will be generated.

Looking at this waveform, we have already looked into this. I will explain here and then zoom.

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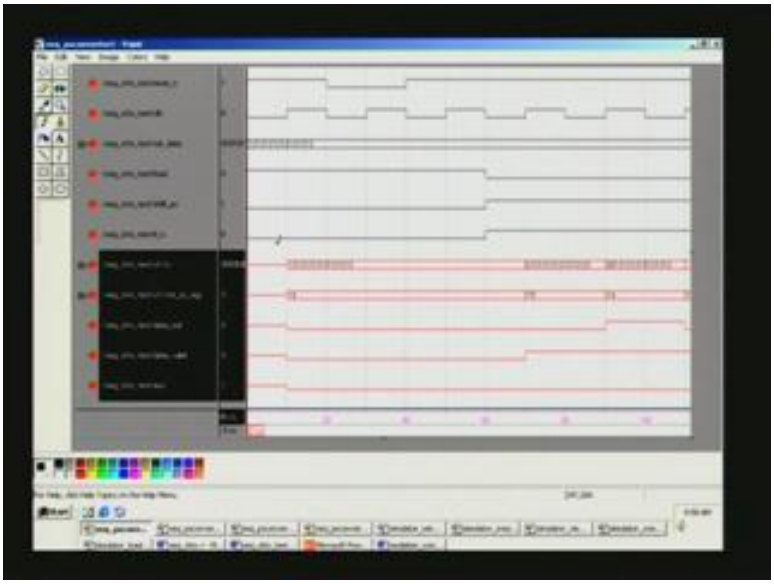

We mentioned that it is basically shift register which has been loaded with 1 0 1 0 prior to that. It is right here with the set data being put over here with load asserted, you can see that load is high here. Shifting starts right at this point once the load is complete. Simultaneously you also assert say right here, (Refer slide Time: 03:36) what happens after this, this is 1 0 1 0 pattern shift register, which will be shifted one bit per cycle at positive edge of the clock. That is here and you can see there is also a counter which will keep track of the number of bits sent over the serial channel. We start with 16 here and then it starts decrementing every time a bit has been sent and the first bit that is being sent here is, say, 1 0 1 0, it becomes 0 1 0 1; that means this has been right shifted. The very first bit on the LSB will go out as data out. That is what you have here.

Let us have a look where this is a right shift. If it is right shift, the first data out is 0, not 1 as I mentioned. The first bit you would see is, I will zoom, see this is the shift register, this is the counter and data out, data valid and end of conversion respectively here. All of them are 0, and right here you get the very first bit is for this, and that is the first bit here. The next bit is 1 and that is what is here I have told you wrong. The data out is this right here.

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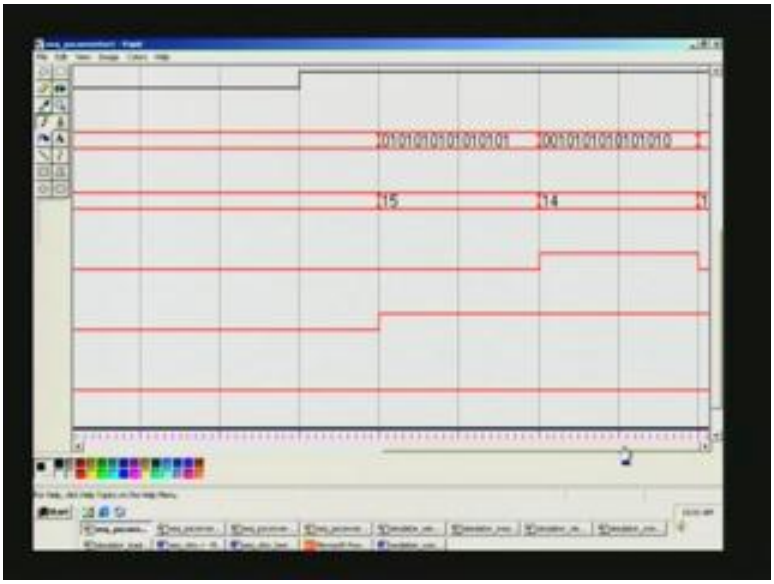

0 is first here, then 1 here. Hereafter, it should be 0 1 and so on, in a toggling mode. This is the very first waveform we already had a look into. The second one which we did not have last time is this and this is towards the end of the right shift.

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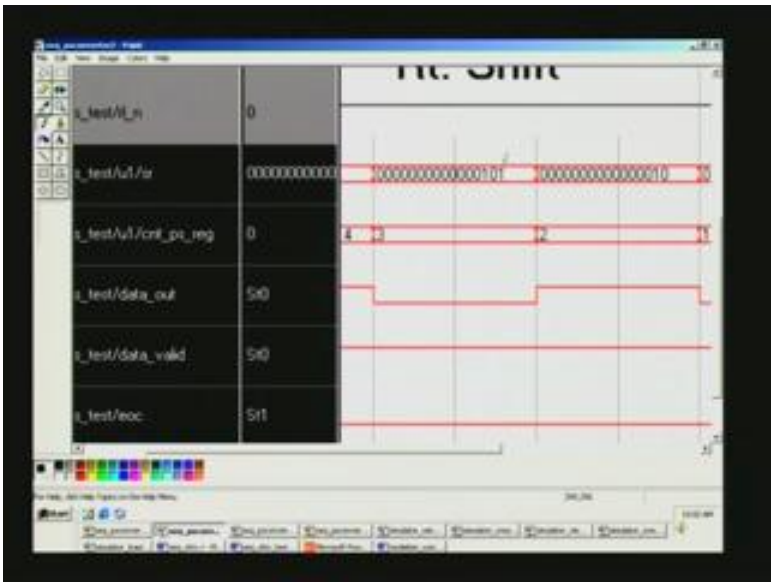

The set data is this and this right shift is still high and shift has been asserted and this counter has come down to 4 here, 3, 2, 1 and so on. You can still see that some of the patterns are still here, 1 0 1 here and once you right shift this, this one gets dropped. 1 0 here and you can see that data out is going alternatively low and high. All through data valid is high and end of conversion is 0 because all the bits are not serialized. Now coming to this end, 1 0 1, then 1 0 is the shift register and then comes 1 because 0 gets dropped. Finally, 1 also gets dropped. Ultimately it will be zero here, we started with 1 0 1 0 so the last bit will be the MSB. Naturally that should be the 1 here.

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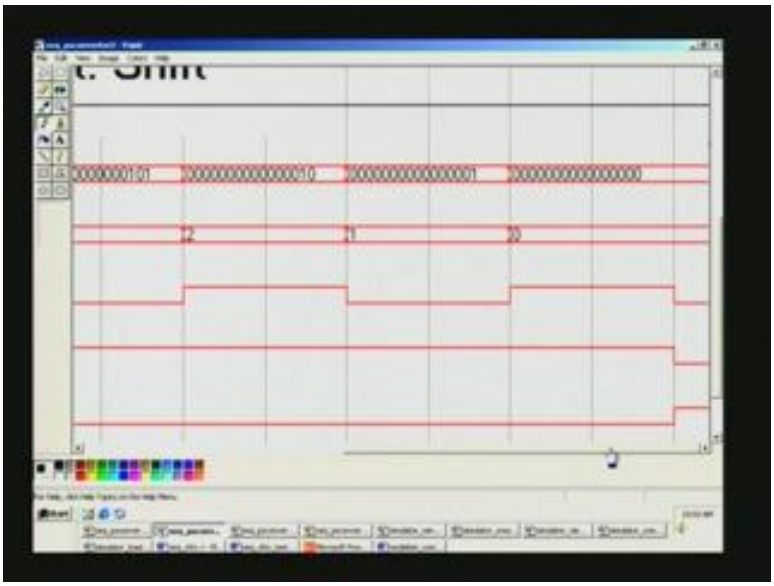

Now you can see after this is over that all these transactions are taking place at the positive edge of the clock. You can just see here. It happens every time, as you can see the positive edge here and positive edge here. Finally, an end of conversion is asserted here. This is the last for the data therefore data valid goes low.

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The last two are data out here and corresponding data valid, end of conversion. This is for the right shift. Similarly, we can have the left shift here. Straight away we will go into the waveforms of interest and this is once again shift register here. Before this I will just show where the loading is. Now this time we are not loading, this is data loaded as you can see set data, and what we load now is 0 1 0, the opposite of the previous content. This is the load asserted and shift starts being active right from here the moment it is loaded.

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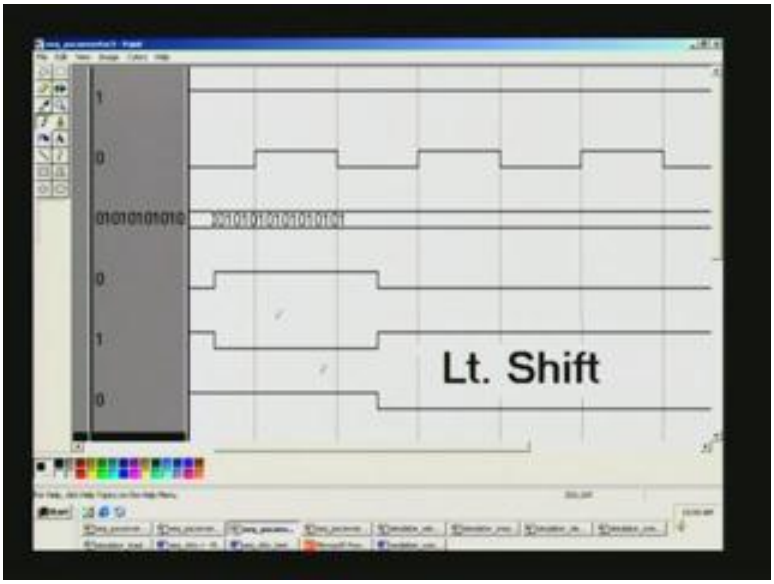

Shift register must start with this value. You can see same 0 1 0 pattern here. Once again this is the previous end of conversion which we had processed. The moment you load fresh data, that is reset. You have to add all intricate details with care, while designing systems and data valid was de-asserted in the earlier cycle, so it will have to be asserted here the moment data starts flowing out and once again the parallel to serial conversion takes place but this time it is left shift as it is here.

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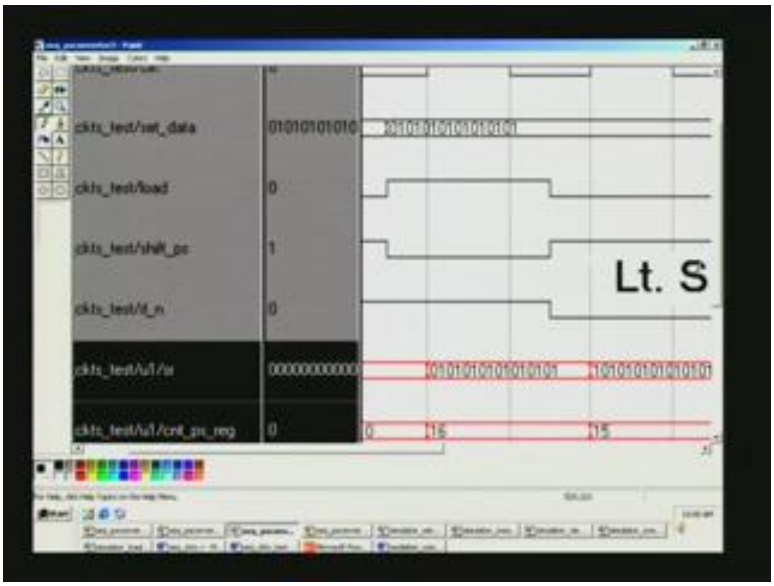

It was 1 here for the earlier thing and it becomes 0 here, implying it is a left shift. If it is left shift, 0 must go through this first here. Data out is here so 0 is there and data valid is asserted here. The count keeps on decreasing and you can once again see 0 1 0 1 again, same bit pattern and it keeps going. Finally, we will have one more waveform where you see the end of this left shift.

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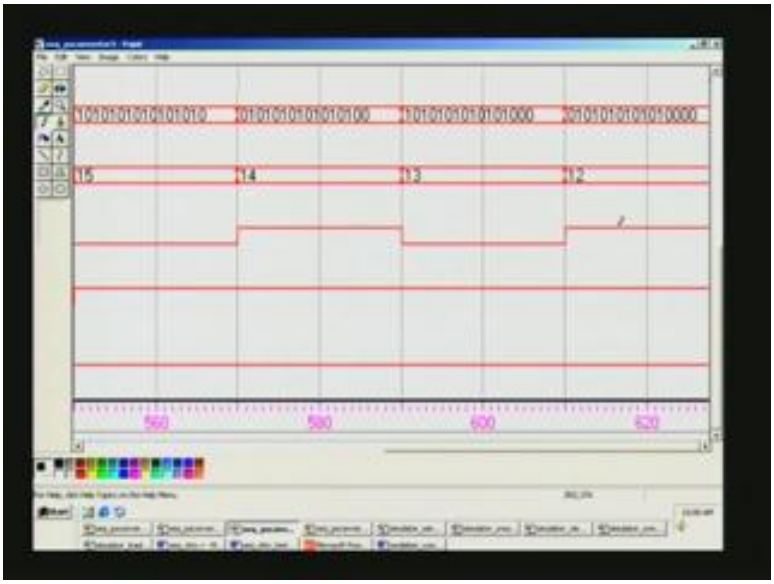

You can see again it was at 4 so it is a left shift. What you have is 1, now it should shift in this fashion. 1 must get dropped and also go through the output, because shift happens here but will get reflected only at the positive edge of the next clock. It goes this 0 1. All the vacated bits are all filled with 0s. Then, again, this one will go through to the MSB and again you can see the data out toggling. Finally, it ends up at 0 here.

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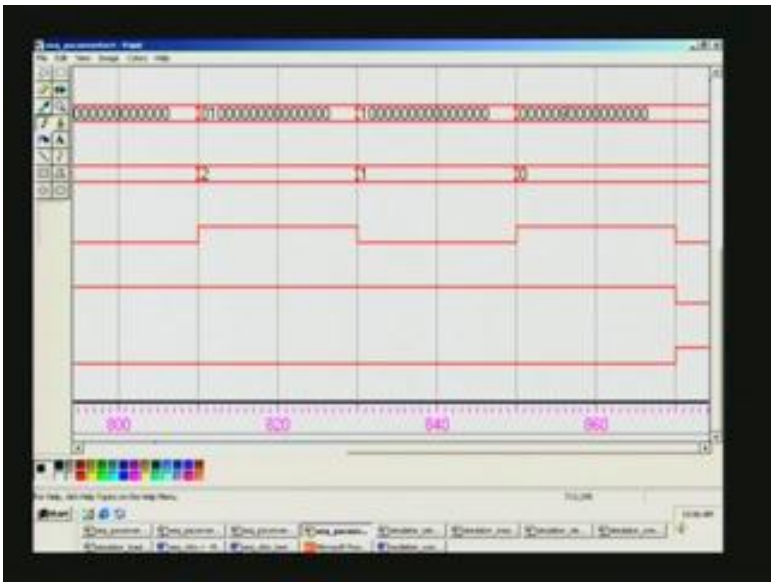

We started with 0 1 0 1 etc. so the very last must be 1 because it is a left shift; 0 1 0 1 0 1, so the last bit will be 1 and after it shifts here and once again data valid goes low and end of conversion is activated here. This completes the parallel to serial converter and will go on to state machine.

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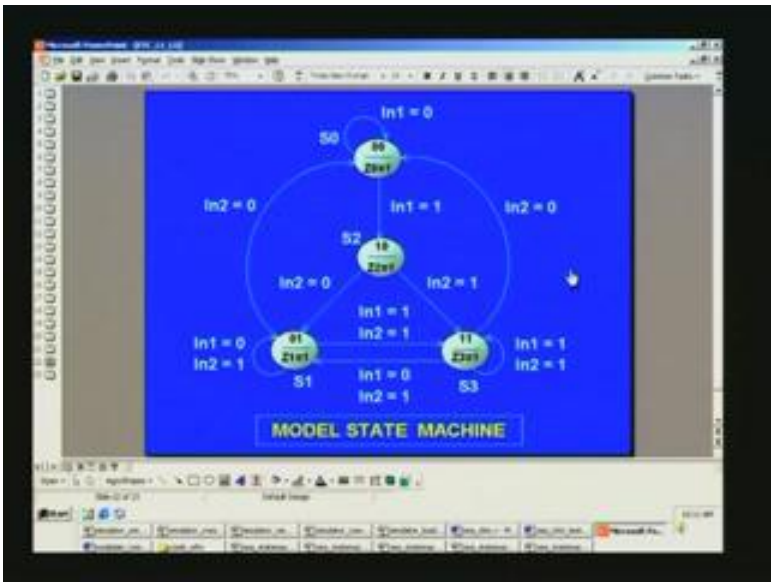

We are now looking at the waveforms for state machine. In this we have four states S_0 to S_3, and there are two inputs based on which there will be a transition made right from one state to another. For example, if it is in 0, it remains at the same state and for each of the states, Z_0, Z_3 are mere lamp indicator. The actual state is 0 0 1 0 and so on. Looking at the waveform for this, we have actually looked at this S_0 state earlier, and we will just quickly go through that. Here what you see is the initialization phase. When reset is applied and inputs are here, and these are all the state outputs. Actual state itself is here. This is a plain reset state.

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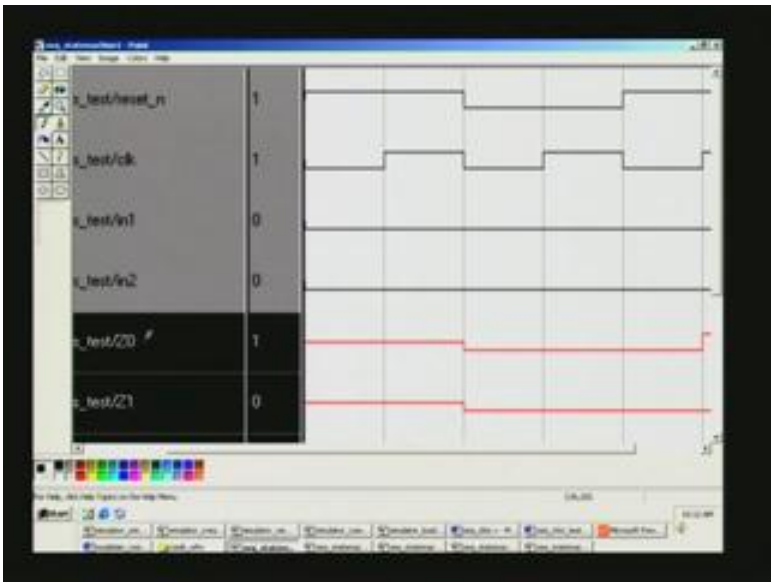

There is nothing much to convey except that all the lamps are 0 and at this point of time, the real S_0 state comes into play because reset is removed and following positive edge of the clock only starts getting activated. Right at that time, it enters the S_0 state and activates Z_0 there. As long as In1 is 0, it continues to be in S_0 state. In fact, that is what we have already seen and from this it can go to the next state provided In1 is 1. That is, it goes to S_2 state and in this case you can just see here this is S_0 here and it is going to S_2 state here. Although, in the S_2 state it enters the state right at this positive edge of the clock, actual lamp output will go only at the next positive edge of clock right here. You can see this is S_2 here. This corresponds to S_2 state and so on it goes. We will have a look at the actual state. In S_0, you can go out to S_2 state provided In1 is 1.

Let us examine In1 so it is 1 and irrespective of In2 being any value and it takes you to the next state S_2 here and this lamp corresponding lamp also lights up here. Now let us see what happens here. At this point of time you can see some other Z_1 going high, let us verify whether that is right.

In this case what we have is In1 and In2; there is a change of state here. Earlier it was 1 now In1 goes to 0; let us see what happens here. If it is 0 and In2 goes high, 0 1 we have to consider in 0 1 state. Right here Z_2 is 1 here and so In1 is 1 here and at this point of

time it is 1 and 0. Let us find out what it is, if In2 is 1, in S_2 state, if In2 is 0 it will take you to S_1 state. Otherwise it will take to S_3 state. I think it is better if you can slightly compare the two, this may be pretty difficult to remember.

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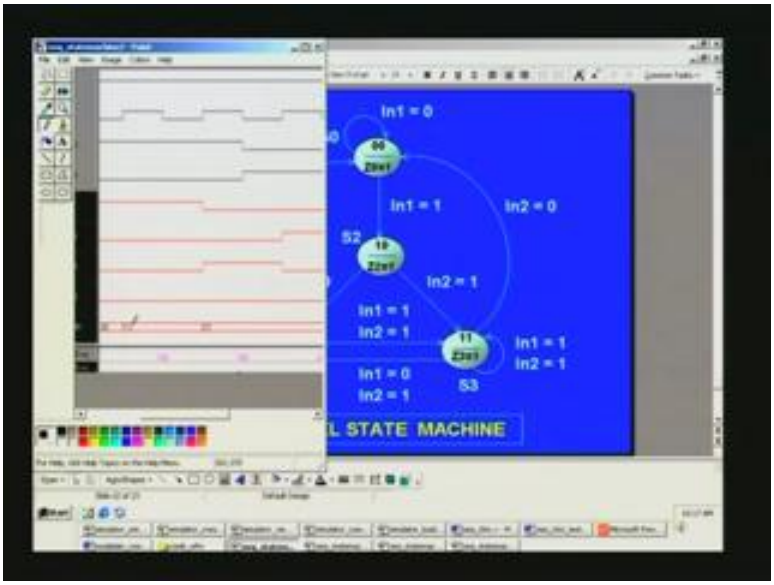

We are in state 1 0 here and corresponding in out are this two are in out, if you see this In is 0 here.

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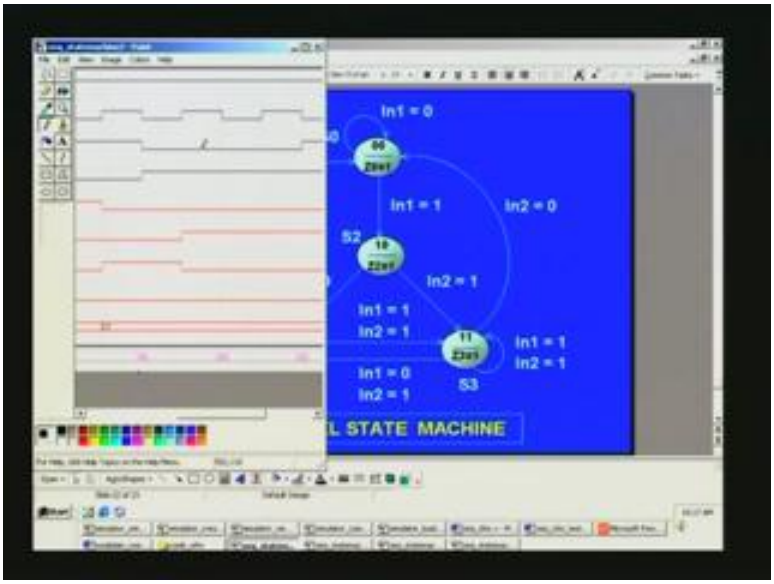

We are now looking at the S_1 state. We are at the looking at the wrong state so we must have a look here. S_2 is the next state here. In this state so what is in In1 is 1 and this is 0, In1 is 1 In2 is 0 in S_2 state. We will go rather slowly because it is quite intricate and only by doing this will you understand it. We are in S_2 state. What matters is only In2. Here, In2 is this one so it is in 0. In2 is this, so it should take you to S_1 state. That is what it is right and here you are able to see this waveform.

Next will go from 0 1 state and in this these are In1 and In2. In S_1 state, In1 is 0, this is 1. As long as it is in 0 1 it continues to be in 0 1 state as per this. See in 0 1 so long as it is 0 1 here it continues to be in S_1 state. On the other hand if In2 is 0, let us see what really has been put. This part you have, it continues to be in 0 1 state and here it is going to 1 1 state. Let us see the corresponding IOS. IOS are these two. It is 1 0. In this state, these two are in S_1 state. This is 1 and this, I read as 1 0. It is actually 1. For 1 1 automatically this is satisfied so S_1 to S_3 it goes to, and this is what you see here. In the next continuing waveform, 1 1 and now corresponding In1, In2 is so once again will just reduce this.

We are in S_3 state now and that is this one and corresponding inputs are now changed inputs 0 here and this 1 is 1. If it is 0 1 it should take you back to S_1. That is what you see here. From 1 1, it takes back to 0 1 state. Then at 0 1 now again input here is 1, it is 0 1.

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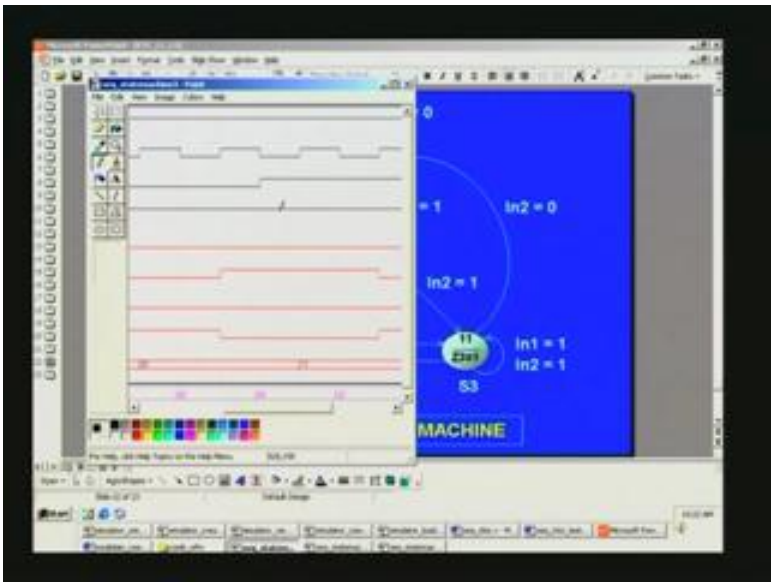

0 1 would mean continuing the same state here and next 0 1 once again, these inputs are changing to 1 1 1, it will take you back to S_3. We are just going to and fro and we will now move forward. In 1 1 state, let us see what happens. Here there is a change and go to this state, both are 0 0, what matters is only In2 being 0 here. If In 2 is 0 you go back to state 0 right here. What we have seen is this, here, here and then to and fro, we then go back here. What we are to see is this part, that alone remains the same.

Let us move onto the next one. We had to look at S_1 and S_3, so that means we have to analyze the S_0 condition. I think this 1 is here, the fourth waveform. In S_0 state, both are 1. What is of interest actually is In0 being 1. We are now going back to S_2 here, so In1 alone matters now and from here it has to necessarily go through this state. It has to go to S_2 state here and that is what is happening here. In S_2 state, both are 1 here. Since both are 1 it is going to S_3 state and that is what is happening here. It continues to remain in S_3 state so long as the inputs are same and in fact, it is same right up to this and then finally it goes to 0 1. That is for 0 1 transition. Let us see that.

We were here, 0 1 would take you to S_1 state. I hope you have kept track of all the LEDs for Z_0 through Z_3, in fact I forgot to mention but you can see one of them and you can verify here.

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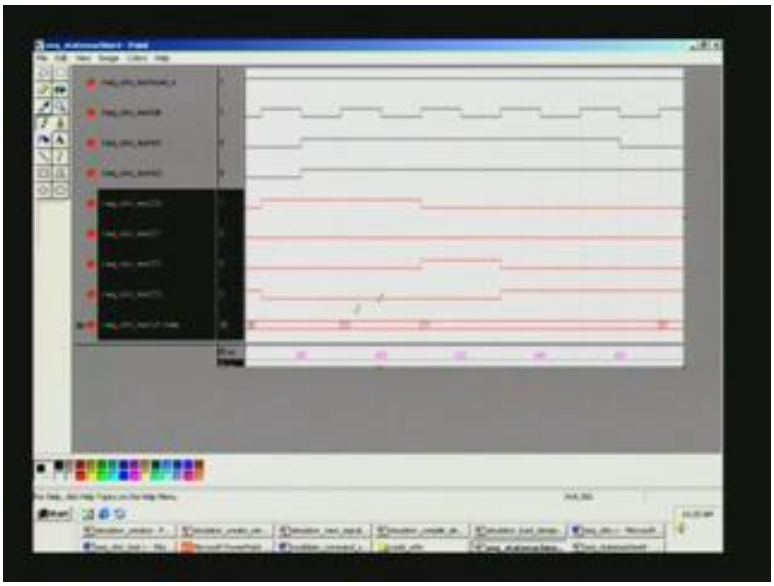

For 1 0 state it is the same. You should get here Z_2 and it must go, so 1 0 is 2 so Z_2 must go high, so this verifies at random and finally we have one more waveform in this state machine. I think this is the path we have not covered and let us see whether it is so.

Let us say from S_1 to S_1 state and then from there it is returning to 0 state and let us see the condition here. What is this here, it is 1 1 and so input is 0 1 here. In 1 1 state 0 1 we have to look into this. If it is 1 1 it will go to S_3. We are in 1 1 state, which is 0 1. In the 1 1 state it is 0 1 and 1 1 is this state not this with 0 1. It takes you to S_1 state and that is what it is right. In S_1 state again it is continuing to be same and therefore it will remain in the same state and once again at this point of time there is a change in inputs. It is here 0 0 so if it is 0 0 it should naturally take you to 0 0 state. Earlier it was 1 1 here so the Z_3 output is set here and it will change state for this state only at the following positive edge. This is why it is always delayed by a clock pulse and earlier for S_1 state for that corresponding Z_1 is let so you can always see that it takes effect only at the following edge because only after entering this state this output can be set.

Transition is happening from this state to this state only here, so naturally it is that state output that must get reflected only at the positive edge of the clock and that is why this is there. Any sequential machine will have this and it is always delayed by a clock. This is not a handicap because we always have a very high frequency for the clock and no user can notice the difference. No erroneous operation can take place because the whole thing is asynchronous as such. From S_1 to 0 0, provided inputs are 0, you can see that here and in fact what is of interest is only In2 being 0. In S_1, if In2 is 0 it will automatically take you here. We have seen all the paths, only thing we went to and fro that is why it has confused us a bit. Otherwise we have verified that the whole functionality is intact. The next one we will consider is pattern sequence detector.

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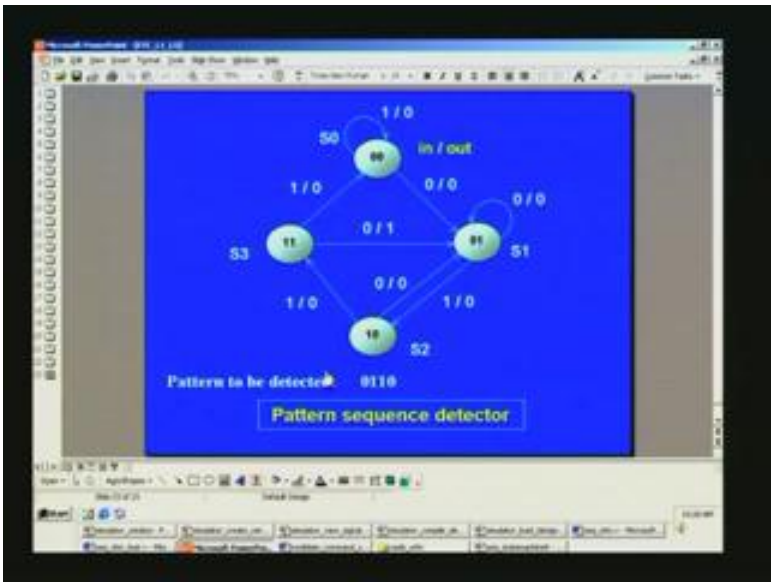

In this detector we have, once again, four states and we have this as input and the corresponding output is this. We need to detect a pattern 0 1 1 0. We will start with this and suppose if it is 0 it will go to this state so because it is 0 in this state and then, as per this, we will be going through it. We will once again go through the waveforms for this.

We will have a look at the pattern sequence detector waveforms now and this is what we have already seen. In the very first waveform here, we have very few signals. There is a reset clock as usual and this is the input pattern that we apply and final output pattern emerges from out. In what state it is, is indicated by this PSD underscore state. To start with we initialize to 0 and the pattern here, we had deliberately put it as 1.

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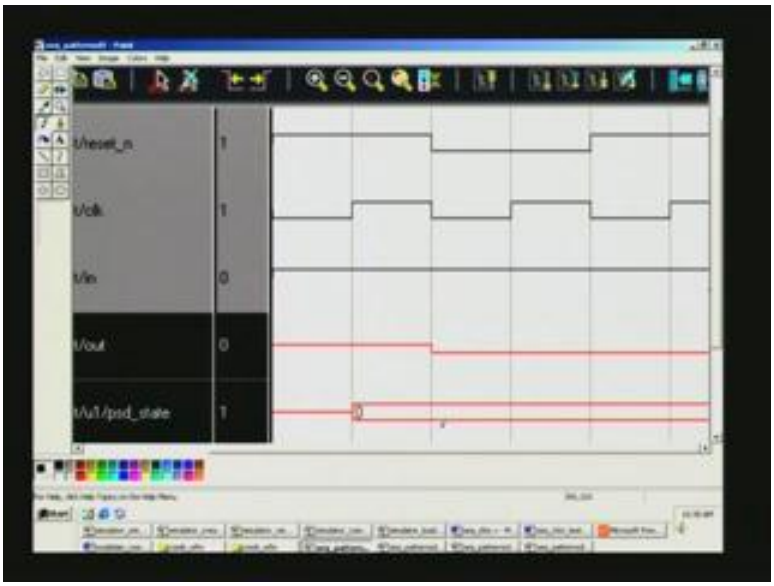

Just to see that, the very first 0 is not encountered to start with. There is not much activity in this first pattern as such. That is what is here as long as its input is 1; it continues to be in this state. Now next we have the second set coming over here and you can see this from state 0 we are moving onto state 1. Let us see what happens in the mean time. First, what we have is 0. Earlier it was 1, now the very first pattern that comes is 0 here and at every clock, transition is being reckoned.

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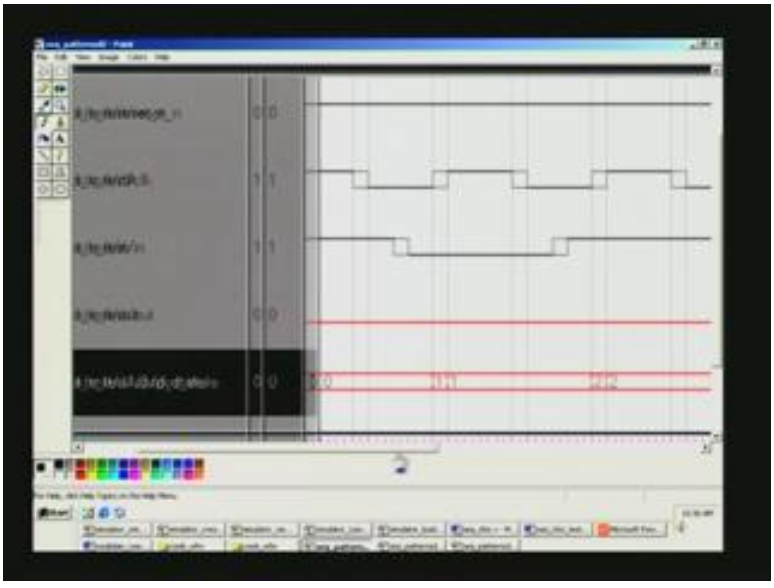

Here, the actual input is applied little offset, as you can see. This is because when we come to positive edge of the clock it must see stable value at the input.

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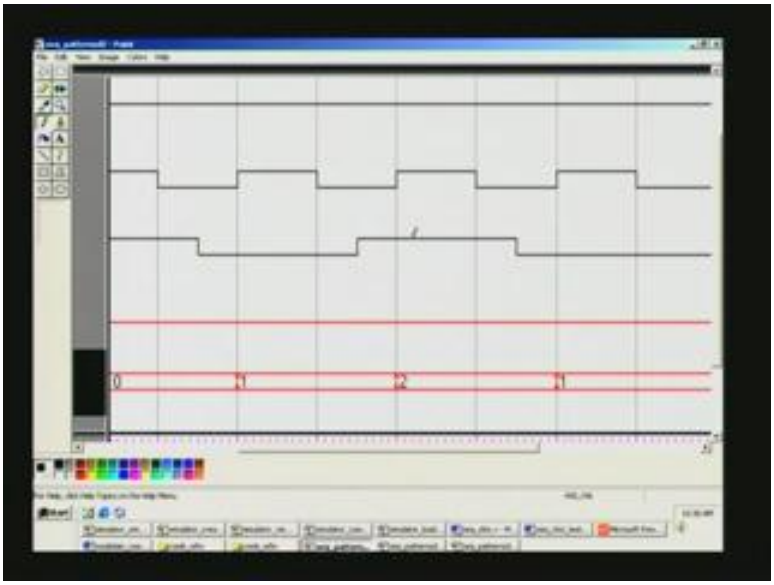

That is the reason why we have taken care in the test bench we had seen earlier. Now you can see this bit pattern that is being applied from the test bench. To start with, it was 1 now comes 0 here then 1 here, once again 0. Naturally, we will continue to remain in the same state and that is as per this, as long as it is 0, it will continue to be it. It was 0 there and it went to state S_1 and then continued to be in S_1 as long as 0 is the input and corresponding outputs are all this here, so what is indicated as out in the waveform is precisely this and in is this. We continue to be here in S_1 state. That is here. It is already in the S_1 state. Now we have skipped this.

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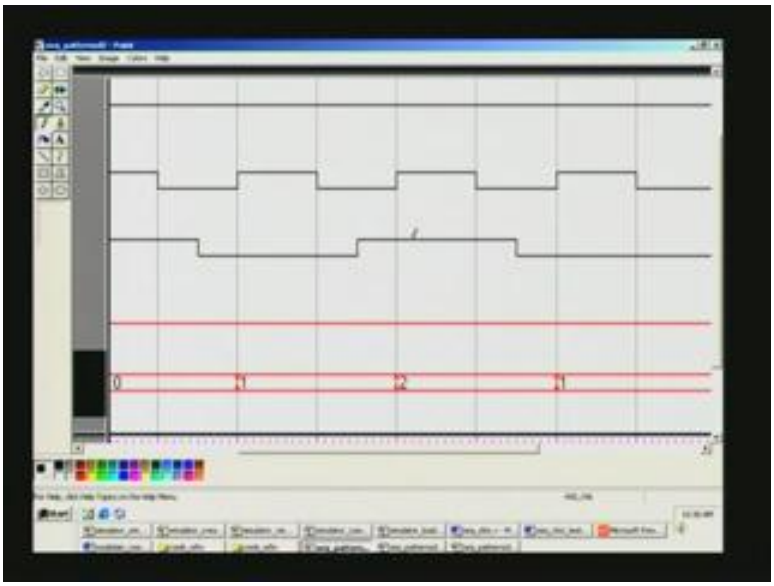

What happens here if 0, this is 1 to start with and 0 1 has been encountered. If it is 1, the input is 1, this is input. If it is 1, this is the output. In state 1 if the input is 1 what happens? It goes to state S2 and now once again we change the input here from 0 1 to 1. This is what we applied from the test bench.

Let us see what happens to this if it is one in state S_2, it goes to S_3.What is the problem? It is not going. It is 0 here, what is sensed here will be applicable only here. Let us analyze here, in S_1 when input is 1, it is changing state here. Subsequent transition is going to the input here so what does it sense here? Is it 0 that is to be sensed or 1 that is to be sensed?

In S_1 the question is, should we take 0 for this state or 1 for that state. Let us examine that. If S_1 state is 1 it should go to S_2, otherwise it should remain right there in S_1 state. Let us see what it is if it is 1. It should go to S_2 state. In the S_1 state if it is 1, which is here, then you should go to S_2 state. This means that only at this positive edge this is being sensed right and this is the result of the previous one, so whenever a positive edge of the clock is encountered, only at that point of time it is going to check the input here.

Now at 2 let us put the same condition so at 2 naturally it is not this 1 but this Yes, if it is 0, it should go to the S_1 one state. If it is 1 only, it will remain there so it is here. At this state what counts is not this 1 but this 0 prior to the positive edge clock transition. At this

point of time only this input is taken and processed and this corresponds to this state and as a result of which, you get a new state here. Let us see that in state 2, when input is 0, it should go to S_1. In state 2 if input is 1, is it 0.

If it is 0 then it should go to S_1 state, the input is 0. No, the output remains constant 0 we have not encountered 0 1 1 0 at all. I mean at this state, the first thing that will happen. Unless you go into that state, there is no question of that particular output being effective. It will take place only at the following clock pulse. That is what happens here, is this transition from 2 to 1? That is what we have seen and then we will see in 1, this input is continuing to be 0. Again this is the edge that is sensing the input here. In state 1, if it is 0 it should continue to be in same state. In state 1 if it is 0, it should be continuing it. We went to and fro here. Once again we will go back here. Let us see what happens to input when it is 1 now.

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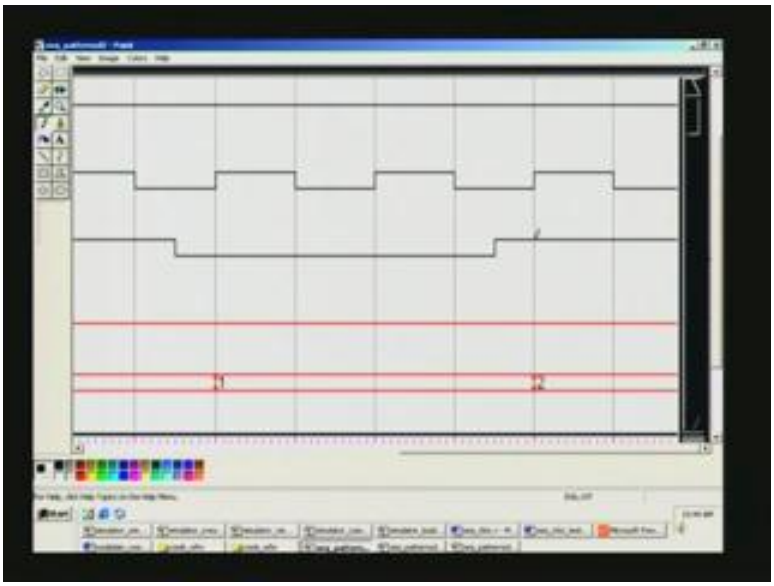

If it is 1, from 1 to 2 it is making a transition in S_1. If it is 1 it is making to 2 and in 2, I think this is the end of this current waveform. We will now invoke that next 1. In this case we started earlier; we ended up with 2 is it not so from 2.

What is happening? It is 1, so this is the edge. The input is 1 at 2 and at 2 the input is 1. It goes to S_3 and does it go to S_3? In this condition input is 0. Now this is the edge, and

from 3 it should go to 1, provided input is 0. Is that correct? Here this is the output. You can see now. We are in state 3, so you can see once again it is taking place. All outputs take place only at the following clock edge. Being a synchronous machine if it is a Boolean expression, then it would have taken immediate effect. Being a sequential thing it will always take place only at the positive edge of the clock. The state itself is changing at this positive edge.

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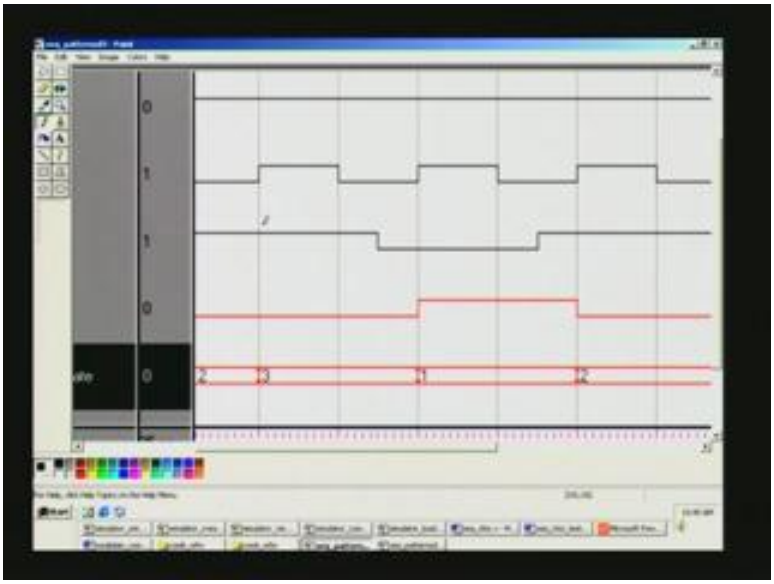

The corresponding output will get reflected only here because it has to wait for entering the state only at the next positive edge. It has just entered the state and that state will be processed only at the next clock edge. Only after you process for that particular state, you can get the output and that is why it is happening. I explained earlier that state changes at this point of time but this output is dependent upon this state. It has just changed here but it has not yet stabilized. It gets stabilized only at this point of time because this is basically a state machine. It functions from clock to clock and not in between. What you have changed here, you had to wait for the next clock to arrive, and only then will this corresponding state be actually processed.

If you look into the source code, verilog code, you will see that. We would have to always put a positive edge clock. Only at the positive edge clock does all this happen.

This was earlier in second state. At that point of time, only at this stage, it takes it from 2 to 3 and right at that point whatever is the actual input here only, that is being taken and then processed accordingly. In order to enter this here you had to satisfy this previous condition here. In order to enter the next state you had to create a favourable condition for the input. Only then will it go into the next one, and only after touching this, although it is changing here, the processing takes place only at this point of time, as far as the input is concerned, because the output is also dependent upon the positive edge of the clock.

In state S_3 you set that particular output it says here. That means it can take place only after one clock delay. The input is changed here and we are changing it because we have a prior knowledge that it will change from this state to this state only at the positive edge. Before this, you are free to make the transition either here or even here. You can even do it here, soon after this. You can make the change anywhere. I put it here that is all. Whatever you make when the clock slides, it plainly looks at the input and whatever the input is, it will go as per that.

As for this state only, at this following clock edge, processing will take place. That is what I want to impress upon you. Moving along, we have already gone from third state to first state and now let us see 1 2 and 1 here.

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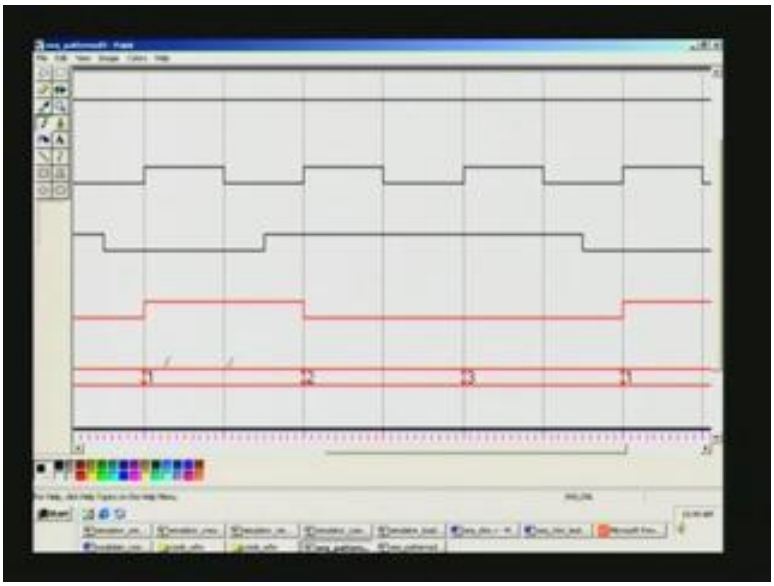

For 1, what is that we are looking into, so it is 1 here, this is the input here. Earlier, we had sensed this as 0, now here at next positive edge only you had to see. Now you will be sensing 1 for the input in state 1. Let us have a look, in state 1, if it is 1 so it should take you to S_2 here.

We went to and fro earlier and now we are coming back. If it is 1, what happens is that it has gone from 1 to 2. Now 0 1 1 0 has bit pattern that has been encountered, which was why at the last 0 it goes to 1 here. This is the corresponding output and whenever there is 0 1 1 0, even in recurring fashion; you should have 1 here, corresponding to that. In state 2 we are analyzing. What we sense here is 1 in state 2 and it goes to S_3. It is going to S_3 and just keep track of the pattern that we have already encountered 0 1 1 0.

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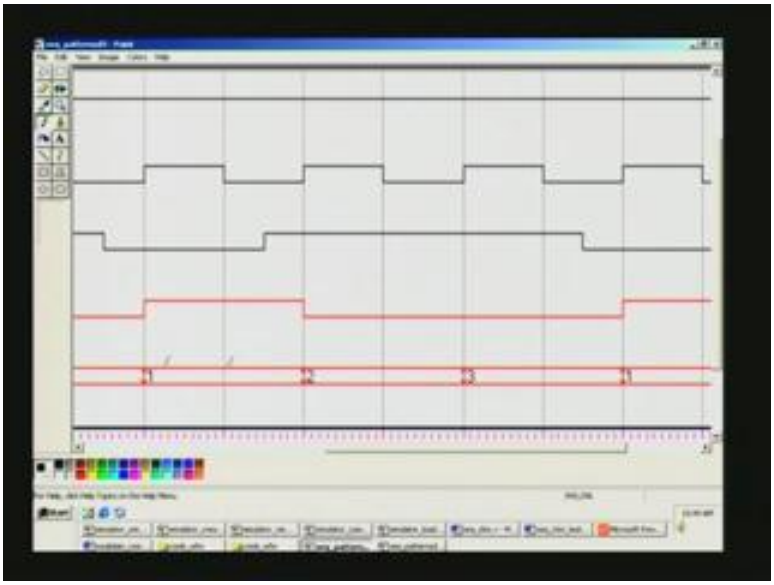

Now, one has come, so again you see two 1s are there, even when the last pattern is taken into account. 0 1 1, once again you see a 0 here, so promptly goes to the output high here and from third state you should finally have seen here. It should go to one state, provided this input is 0 in third state it is here. If input is 0 it should go to one state output is 1. That is what we have here.

We have one more waveform before we wind up. We were in state 1 and now what is happening, the input is 1 here. Then one input is 1 so we had taken this path we have

gone already here so we are taking the path once again here. It should go from S_1 to S_2, provided input is 1. Here again the 1 1, you notice this pattern, 0 here, then once again 1, then one more 1 and then again 0. The output is also correspondingly 1, so you can see 2 2 3 transition here. Then in S_2, if it is 1 you go to 2. If this is 1, is it correct? 2 to 1 to 3 and next, from 3 you have to go to 1, provided it is 0 3 and 0. In state 3, input is 0, so it should go to S_1.

In state S_1 this only produces that 1 again. In state 1 we had input 1, so it takes you to S_2 here. In S_2 input is 1. It should go to 3 and in 3, input is 1, it should take you to S_0. This completes both combinational and sequential circuit waveform analysis and we are actually winding up Modelsim simulation here. In the next class we will summarize all the commands so that it will be a ready reckoner for you.

Summary of Lecture 27

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