Solid State Devices
Dr. S. Karmalkar
Department of Electronics and Communication Engineering
Indian Institute of Technology, Madras
Lecture - 9
Equilibrium Carrier Concentration (Contd….)

Today is the 9th lecture of this course and 7th lecture on Equilibrium Carrier Concentration.

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Let us see what we have achieved in our discussion on the intrinsic carrier concentration which we completed in the last class. We have shown that this is the allowed levels and density of states picture. The density of states function is closed to parabolic near the band edge. Then the fraction of the occupied states function that is the Fermi-Dirac function as shown in this diagram.

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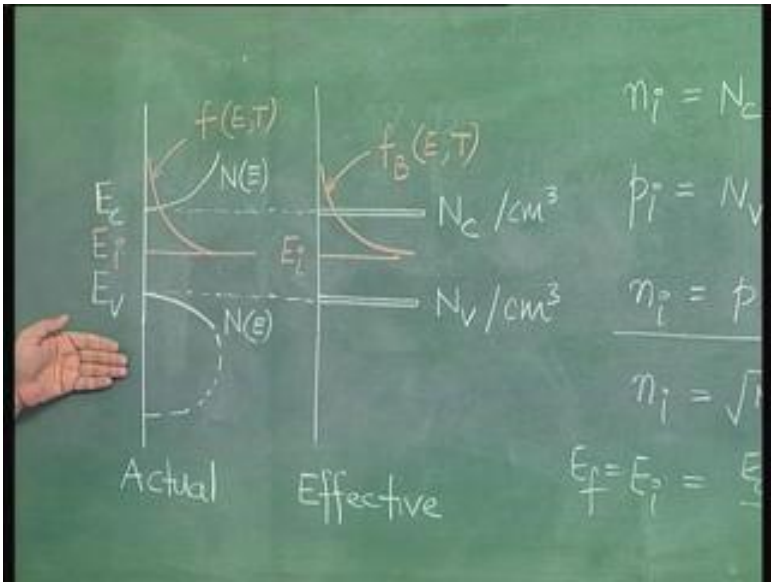

From fraction of occupied states and the density of states function you get the excess carrier concentration which is the area under the product of N(E) and f(E) functions. This is the n_i intrinsic concentration. Similarly, one can calculate the intrinsic hole concentration which is equal to n_i. This is the actual picture. Now the formula we have derived shows that you can replace the actual picture by a simpler effective picture which is given here. So, in the effective picture you have N_c by cm cube density of states at the conduction band edge; N_v by cm cube states allowed for electrons at the valence band edge and then you can multiply these allowed states by the fraction of occupied states function which is the Boltzmann approximation of the Fermi-Dirac function. And then you get the simple formula n_i is equal to N_c (the allowed states multiplied by the fraction of these allowed states which are occupied under the Boltzmann approximation) exponential minus E_c minus E_f by KT); n_i is the number of occupied states in the conduction band.

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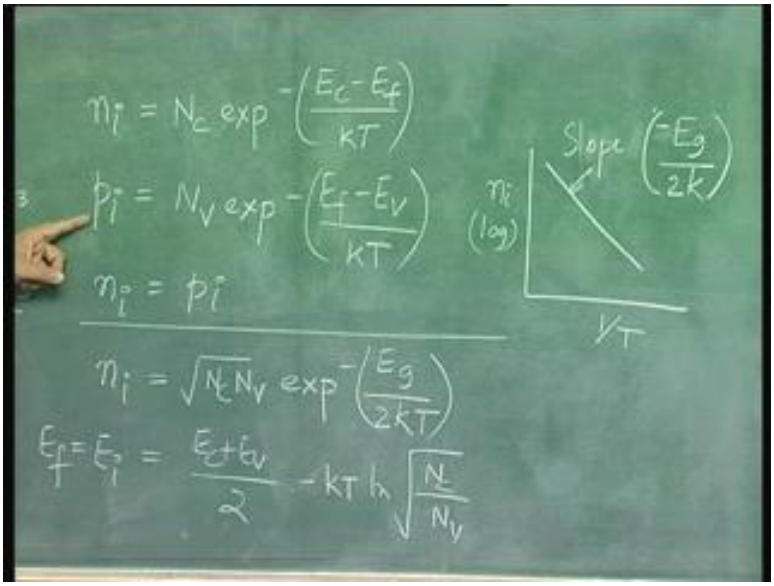

Similarly, one can write an expression for p_i for the unoccupied states in the valence band. And finally you know that n_I is equal to p_i. Now, from these three relations you can eliminate the Fermi-level and you can get the intrinsic concentration as square root of N_cN_v into exponential minus (Eg by 2KT). You also get the Fermi-level which for intrinsic semiconductors is called the intrinsic level E_i is equal to E_c plus E_v by 2 minus KT ln square root of N_cN_v. This term is generally very small, so one approximates E_i by E_c plus E_v by 2 and this is what is shown here. The E_i is almost in the middle of the energy gap. The n_i if you plot on the log scale as a function of reciprocal of temperature the slope of this line will almost be a straight line, and its slope will be minus Eg by 2K. That is how you can find out the energy gap of semiconductors from measured concentration versus temperature behavior.

It is important to note that this N_c the effective density of states is not exactly the same as the total number of states in the conduction band. Or for that matter N_v is not the same as total number of states in the valence band. For example, these total number of allowed states in the valence band we have seen is 4(5)(10) power 22, whereas N_v is of the order of 10 to the power 19. So one must not confuse N_v as simply the area under this curve; this is an effective picture. In today's lecture we will be discussing a model for the extrinsic semiconductor under equilibrium. We will be discussing a model for the carrier concentration.

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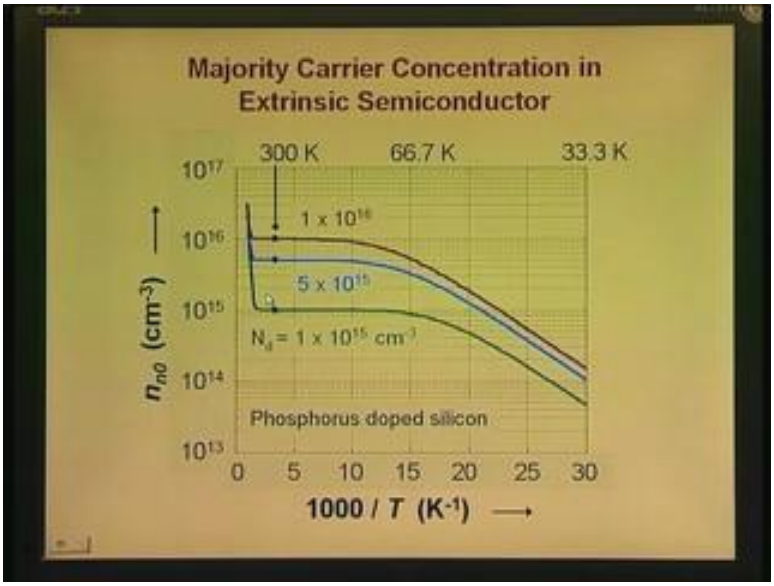

So if you recall what we want to explain here is the behavior shown in this slide. We would like to explain how you get a flat portion of constant majority carrier concentration over a certain temperature range. And adjacent to this you have for low temperatures an exponential behavior of the concentration with temperature, and also for very high temperatures an exponential behavior of the concentration. Another thing that we want to explain is, the fact that minority carrier concentration is given by (Intrinsic Concentration) whole square by Majority Carrier Concentration.

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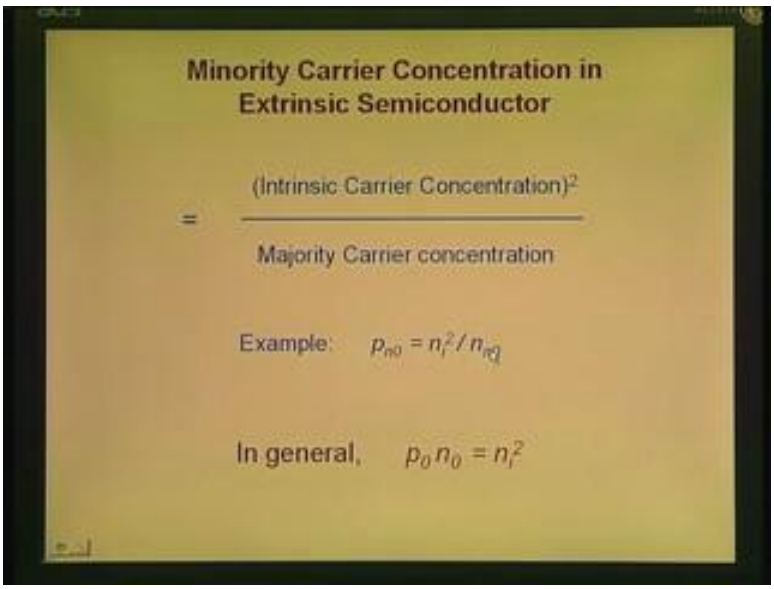

In a n-type semiconductor for example hole concentration is equal to $(n_i)_2$ by n_{n0}; that is the electron concentration or in general in any doped semiconductor p_0 into n_0 is equal to (n_i) whole square. This fact also we would like to explain. The way we will proceed for deriving this information will be the same as that we have used for deriving the intrinsic carrier concentration. That is, we will first consider a bond model a simple qualitative model of the semiconductor, and then we will consider the energy bond model of the doped semiconductor.

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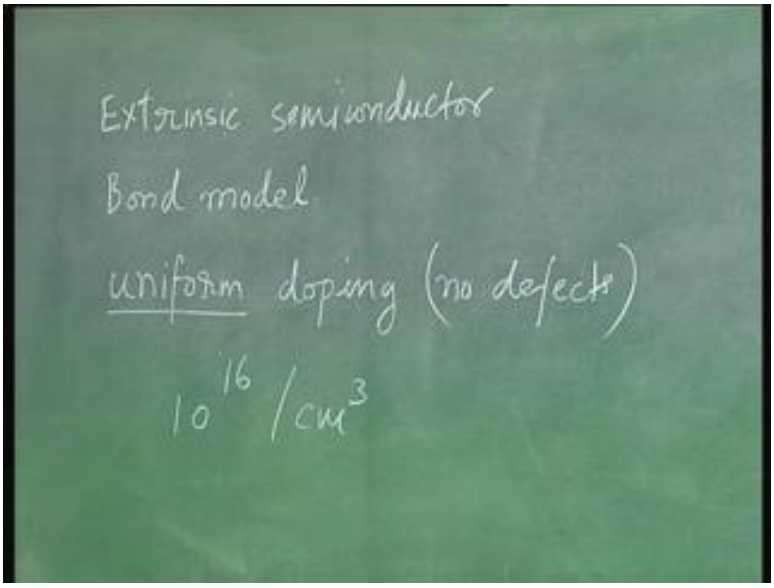

Extrinsic semiconductor bond model: At the outset let me state that we are considering a uniformly doped semiconductor and we will assume there are no defects but only impurities. It is very important to understand the meaning of the term "uniform" in uniform doping. It is very difficult to place the impurity atoms in semiconductor at regular intervals. Just as you have the silicon atoms in a silicon crystal at regular intervals it is not possible to have impurity atoms placed at regular intervals that easily. This is because the processes that are used to introduce impurities normally result in random location of the impurity atoms. That being the case, what is the meaning of uniform doping? So the impurity atoms are not regularly placed they are randomly located. The minimum uniform doping is as follows: Supposing I have 10 to the power 16 per cm cube of impurity atoms then I will find that if I take the semiconductor and I look at the different 1 cm blocks of this semiconductor at different places so each of this is a volume of 1 cm cube.

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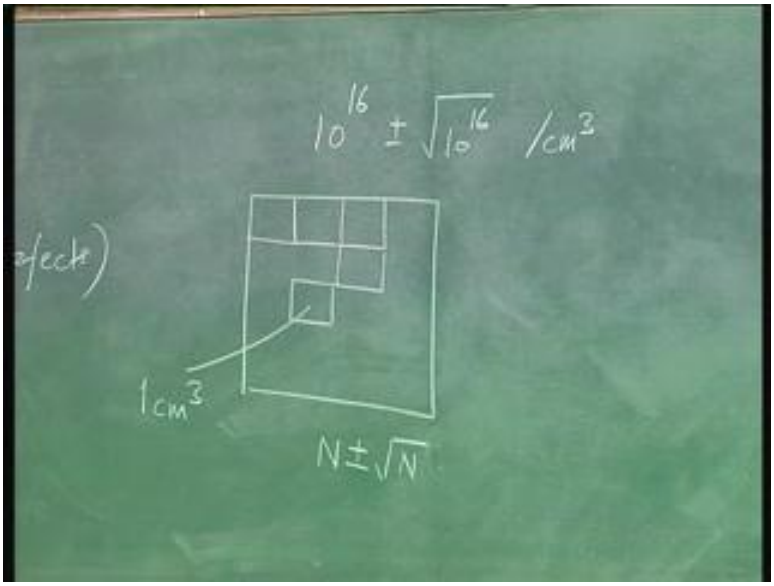

I am showing the picture in two dimensions. Then I will find that the concentration in any of these 1 cm cube blocks will lie between 10 to the power 16 and plus or minus square root of 10 to the power 16 per cm cube. The atoms are randomly located, definitely the concentration of impurity atoms cannot be exactly 10 to the power 16 everywhere. So there is a deviation but the deviation lies within plus or minus square root of 10 to the power 16 of that.

Now, why it should be square root, that we will not discuss but take it as a fact; but it is important to note the result is that square root of 10 to the power 16 is equal to 10 to the power 8 so 10 to the power 8 is much less than 10 to the power 16. This is the meaning of uniform doping that the average value is very large compared to the deviation and that is why we can assume doping to be uniform though the impurity atoms are located in a random fashion.

So, in general if N is the doping then the atomic concentration will lie within plus or minus square root of N of N. The next assumption that we will make in deriving our models is that the concentration of impurity atoms, 10 to the power 16 by cm cube is an example here, the concentration of impurity atoms will be much lesser than the concentration of silicon atoms. Therefore this is called a Dilution Approximation.

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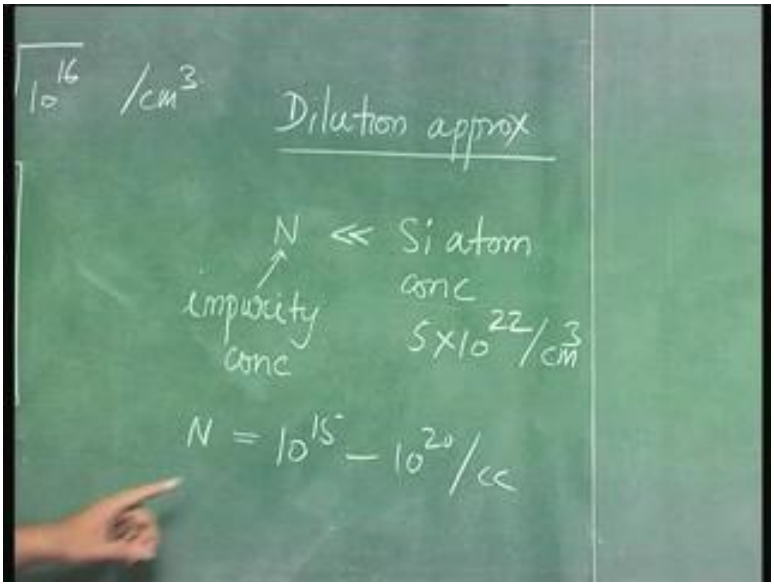

What it means is that, the concentration of impurity atoms N is much less than the concentration of silicon atom concentration. Silicon atom concentration for example is 5(10 to the power 22 per cm cube) and N is the concentration of impurity atoms; so this impurity concentration is much less than 5(10 to the power 22 per cm cube). So you have impurity doping in the range of 10 to the power 13 to 10 to the power 20 that is the kind of range we are talking about for N. N lies in the range 10 to the power 13 to 10 to the power 20. In fact this 10 to the power 20 is at higher range. We will be considering models for moderately doped semiconductors around 10 to the power 16 and so on. And we will assume that the models can be used over a wider range.

We will see that there will be some deviation as you go towards the higher doping levels. So what is the consequence of this dilution approximation? The word dilution means that the silicon is like a dilute solution. It is not a liquid but a solid solution which is dilute. That means the impurity is regarded as a solute and the silicon atoms are regarded as the solvent. The solute concentration is very small.

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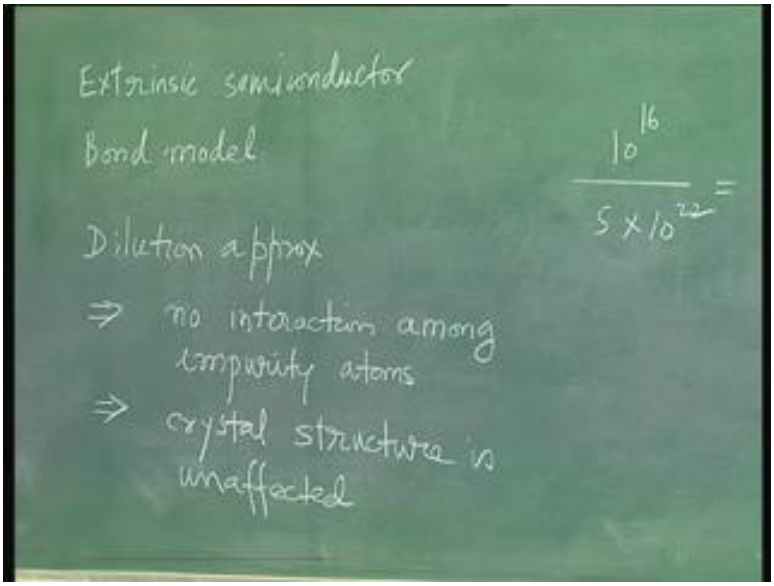

What are the consequences of this particular assumption?
First, dilution approximation implies, there is no interaction among the impurity atoms. For example, if you take 10 to the power 16 as a doping 10 to the power 16 impurity atoms into (5) (10 to the power 22) silicon atoms which means one impurity atom for every 5(10 to the power 6) atoms of silicon. One impurity atom is surrounded by 5(10 to the power 6) atoms of silicon. This evidently means that the next impurity atom will be so far away from this particular impurity atom that there cannot be any interaction between them. This simplifies the picture because we can take every impurity atom to be isolated and then discuss what is happening when you place such an impurity atom in silicon.

So the second consequence of dilution approximation is that the silicon crystal structure is unaffected. This means the atomic distance between silicon atoms is the same as that in a pure semiconductor. So whenever I talk of silicon it must be understood that you can extend it to any semiconductor unless I make statement otherwise. Now under such conditions we will try to derive the model. Let us see the bond model for the case of silicon doped with phosphorus impurity.

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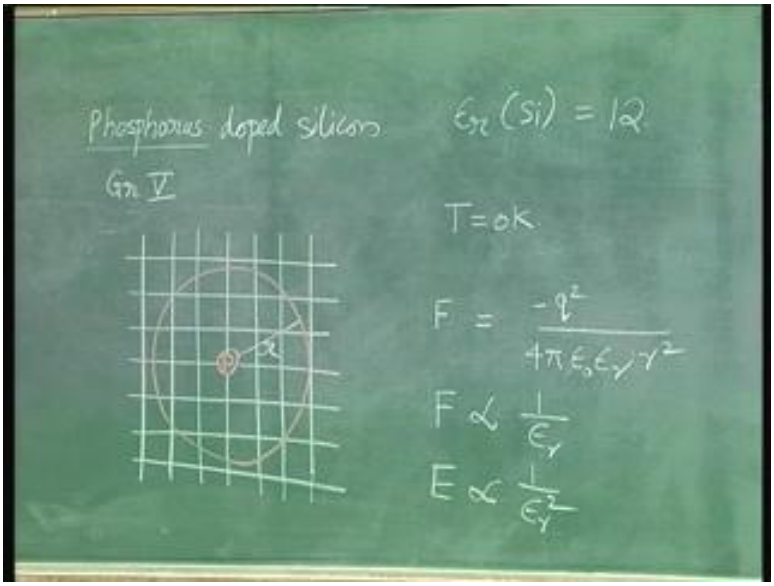

Phosphorus doped silicon: The phosphorus is a group 5 element. So whatever we discuss now is applicable to group 5 impurities in general. If you introduce phosphorus impurities in silicon what is the picture? Let us draw the bond model of pure silicon first; that is a two dimensional matrix and we assume that in this matrix somewhere instead of silicon you have introduced a phosphorus atom.

One can ask why should the phosphorus atom be located exactly in the place of silicon? Well, it is not necessary, the phosphorous atom can also be between two silicon atoms but we will not consider such complications instead we will take a simple situation. Further we are taking only one phosphorus atom because as we have said under dilution approximation the other phosphorus atom does not have any interaction with this. Now let us see what is the consequence of this? Let us talk about the T is equal to 0K first. The phosphorus has 4 electrons in the outermost orbit they will participate in bonding with 4 neighboring silicon atoms.

Now there is a 5th electron. What happens to the 5th electron? A simple model says that the 5th electron will simply revolve around the phosphorus atom, just as you have the picture of the hydrogen atom where there is positively charged nucleus and electron orbiting around it. Notice that since phosphorus is a group five impurity it has 5 electrons in the outermost orbit so without this particular electron the phosphorus atom is positively charged. It is important to note that the orbit radius is rather large and it is not as small as you have in a hydrogen atom and this is because the medium here is silicon and not vacuum.

One must consider the effect of the dielectric constant of the medium in which this particular electron is orbiting. So we are saying that this radius r is much more than that you have in a hydrogen atom. Let us see why? The force between this positively charged phosphorus and the negatively charged electron F is proportional to 1 by epsilon$_r$ because

if you write an equality sign here then the force is given by(minus q) whole square by 4pi epsilon_0 epsilon_r r square. What is of interest to us is this epsilon_r. So we find that the force is proportional to 1 by epsilon_r. In other words, if you have a dielectric medium whose epsilon_r is greater than 1 then the force between the two charges will be less than that in vacuum. So epsilon_r for silicon is about 12 which means the force between two charges assuming some distance r between them will be twelve times smaller in silicon than in vacuum. It is the reduced force that is responsible for a larger orbit.

If you calculate the energy of the electron in the orbit using the bore model of the hydrogen atom similar to that you will find the energy is proportional to 1 by epsilon_r square. This means that the energy of this electron orbiting around the phosphorus atom in silicon would be 144 times less (because the 1 by epsilon_r square for silicon would be (12) whole square) than that of a hydrogen atom. Now this energy of the electron that we are talking about is actually energy required to free the electrons from this particular orbit and take it to infinity. So this is the ionization energy of the electron or phosphorus so we can call this as E_{ion}.

The energy required to free this electron which is E_{ion} is proportional to 1 by epsilon_r square. So what this means is because of the presence of silicon atom surrounding phosphorus this phosphorus atom can be ionized rather easily when it is placed in a silicon medium. The same phosphorus atom if you move out of silicon its ionization energy will be much larger. It turns out that ionization energy of phosphorus is about 0.045 electron volt. Compare this with the ionization energy of the silicon atom.

A silicon-silicon bond, to break this, the energy required is 1.1 electron volt, so this is very small compared to that. Now as a result what will happen is that this electron which is orbiting round the phosphorus atom at T is equal to 0K can be freed very easily when you raise the temperature beyond 0K. For T greater than 0K this electron becomes free of this phosphorus atom because of thermal vibrations of silicon atoms.

Large number of electrons associated with phosphorus impurities which have been introduced will become free at much lower temperatures than the temperature at which the large number of silicon atoms will break their bonds. That is why even for small temperatures most of the phosphorus atoms would get ionized and each phosphorus atom would contribute to an electron.

Please note that, when an electron become free of a phosphorus atom it becomes available for conduction; but no hole is created. This is because a phosphorus atom without an electron is not a vacancy via which the bounded electrons of the other silicon atom can participate in conduction. So ionization of the impurity results in only one type of carrier namely the electrons. But as sure as a temperature it is also likely that some silicon to silicon bond will break and it will give rise to a free electron.

This process is the electron hole pair generation because the broken silicon bond we have said already is a vacancy or hole via which the bonded electrons participate in conduction. So this process of electron hole pair creation is an independent process which

also goes on. Hence like impurity ionization which gives rise to an electron there is also silicon ionization which gives rise to an electron hole pair. This will be an additional source of carriers. Now, if you want to summarize the processes which give rise to free carriers in doped semiconductor that would be something like this.

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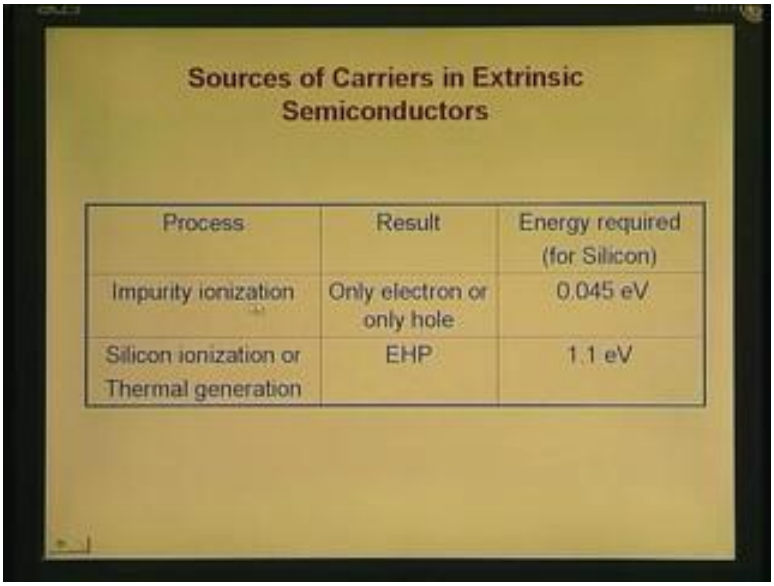

Sources of carriers in extrinsic semiconductors: The process of impurity ionization gives rise to an electron. We will see how it can give raise to hole also if you dope the semiconductor with boron. So impurity ionization in this particular case where phosphorus has been introduced into silicon gives rise to only electron. And the energy required for this is 0.045 electron volts.

There are other parallel processes namely silicon ionization which is also called thermal generation. The word generation in the context of semiconductors is used for creation of an electron hole pair because of thermal vibrations. This results in an electron hole pair, both types of carriers electrons and holes, and the energy required is 1.1 electron volts. Since this energy required is much higher than 0.045 therefore at any temperature, generally unless the temperature is high the impurity ionization process will dominate over the silicon ionization process or thermal generation process.

Supposing N_d is a concentration of phosphorus atoms where N stands for the concentration and suffix d stands for the word donor, a phosphorus atom is called donor because it donates an electron. So N_d is the concentration of phosphorus atoms introduced, then we can use the superscript plus (N_d to the power plus) to show the concentration ionized impurities. As we said at T is equal to 0 no impurity will be ionized, the electron will be orbiting around the phosphorus atom it is not free for conduction. So there are no electrons or holes even in a doped semiconductor at T is equal to 0.

As you raise the temperature, the electrons start becoming free of the phosphorus atom so the impurities start getting ionized. So N_d to the power plus represents the impurities that are ionized. So N_d to the power plus by N_d will generally be ≤ 1. What we are saying is that at any temperature which is not very high, for example supposing you take room temperature, at room temperature we will find that most of the impurities are ionized because the energy required for this is only 0.045 electron volts. And average energy of a particle under equilibrium conditions whether you take electrons, holes, photons, or phonons, we have said it is K into T is equal to 0.026 electron volts. If that energy is 0.026 electron volts to free an electron from a phosphorus atom an energy of 0.045 electron volts can be given by even 2 particles whereas to break a silicon-silicon bond and create electron hole pair you need to give 1.1 electron volts or 42 particles have to converge.

Therefore at room temperature you will find all the impurities will be almost ionized so N_d to the power plus by N_d is almost is equal to 1, whereas the number of silicon atoms which are ionized will be comparatively small. Based on this particular model we can easily explain a portion of the concentration versus temperature diagram.

Supposing I am talking of n_0, that is electron concentration in an n-type semiconductor, I will write it as n_{n0}. It is clear that in a phosphorus doped crystal the electrons will be in majority. You have electrons to be created by impurity ionization as well as by silicon ionization of thermal generation whereas holes are created only by thermal generation. So, electrons are in a majority. So it is majority carrier concentration n_{n0} versus 1 by T. If the same thing you plot as a function of temperature on a linear axis then what this same curve means is that you are going to start from 0 and the curve is going to saturate that is this portion, so this portion is coming here and this portion will go here in this right extreme on a linear temperature scale.

Now we can explain the behavior up to this point from 0. So at T is equal to 0 there are no electrons or no holes so concentration is 0. As the temperature raises the concentration increases. Why? It is because the process of impurity ionization is there and thermal generation is there. But as we said the impurity ionization process will always dominate over thermal generation because of the small energy. So while a temperature may be around 50K to100K the exact temperature depends on the value here. So, for different impurities you have different ionization energies. By this time all the impurities are ionized or N_d to the power plus by N_d becomes almost is equal to 1.

So once that happens the concentration has become almost constant because although this particular process of silicon ionization of thermal generation is going on increasing with temperature, the concentration because of this, the concentration is very small compared to that concentration. It can be shown like this, a dotted line shows the contribution because of thermal generation or silicon ionization. This shows the contribution because of impurity ionization; I will show it with a different color. I will remove this curve to avoid any confusion.

Already all impurities are getting ionized by this temperature which is less than room temperature so you are reaching saturation. Though this component is going on increasing this thermal generation component is very small compared to impurity ionization because of the different energies associated with these two. And then it is only beyond this temperature here that the thermal generation is becoming comparable to the impurity ionization. So here beyond this though the impurity ionization has saturated thermal generation is increasing and it is going beyond this so the carrier concentration now starts exceeding. That is how you can explain how you get an increasing portion in the beginning then a flat portion of the concentration and then again an increasing portion. This kind of a behavior arises from the two particular sources of carriers namely impurity ionization and thermal generation and their individual behaviors. This is the kind of bond model we have for phosphorus doped silicon.

We can have a similar model for boron doped silicon. Let us take boron doped silicon, boron is group 3 impurity. The ionization energy of boron is also about 0.04 electron volts. Let us see how this picture would be different in the case of boron. Here the phosphorus is being replaced by boron. Let us redraw this part of picture to understand how I can say that at T is equal to 0K you can have a hole revolving around a negatively charged boron atom. Let us see how this is true.

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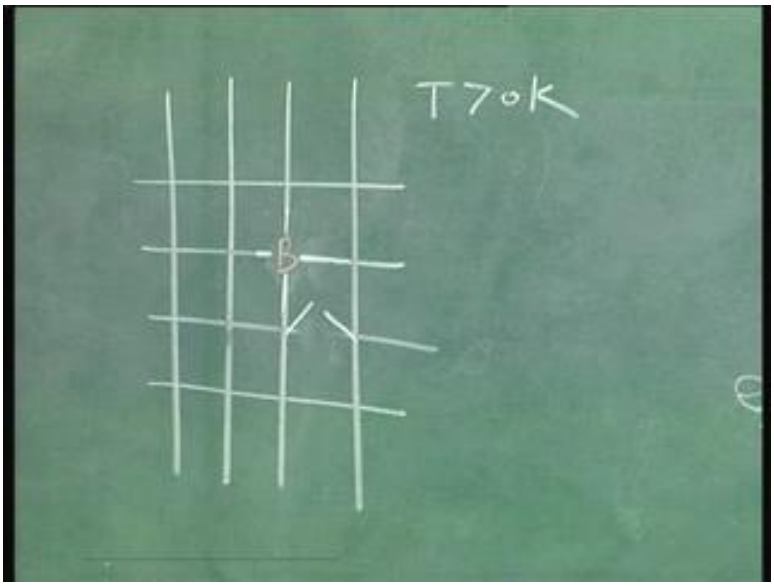

Let us say this is the boron atom here. Boron has three electrons in the outermost orbit; therefore, you will have 3 bonds; however one bond will be broken, because boron does not have a 4th electron whereas silicon has a 4th electron here. Now this particular picture of a boron atom without a electron or a broken bond can be regarded as equivalent to this picture of a boron atom negatively charged with the hole revolving around it. How can that happen? If you take for T greater than 0K, it is possible for an electron from any one of this bonding processes, electrons located in any of this silicon-to-silicon bonds

jump into this site and fill in this place and establish this bond. If that happen the electron which is coming to this boron atom will make this boron negatively charged.

But since the electron has come from somewhere nearby, let us say it comes from here, it will leave behind a vacancy here. Note that such a thing will happen only at T greater than 0K. So for T greater than 0K the absence of an electron near the boron side results in a broken silicon bond somewhere else because the boron atom likes to accept an electron at this side to fill in this bond I need results in a hole. So T greater than 0K each boron atom which is ionized will contribute to a hole, to breaking of a bond that is why boron atom is called the acceptor atom.

Therefore we could regard the picture for T greater than 0K to be a broken bond of silicon which cannot take part in the conduction because at T is equal to 0K you have no electrons or holes and no conduction in a semiconductor. This fact can be represented as a hole which is bonded to the boron atom which is revolving around it. Once the hole is bonded that means it is not a hole at all in stick sense because hole is a mobile carrier; something that can move in response to the electric field. This is the kind of imagination that we do to get a simple model.

The only difference between phosphorus and boron if you adopt this model is that at T is equal to 0K the phosphorus atom is equivalent to a positively charged nucleus with an electron revolving around it, whereas a boron atom is equivalent to negatively charged nucleus because it has taken the 4^{th} electron from somewhere else and a hole or a positive charge revolving around it.

Now that being the case the energy associated with this revolving charge is very clear that it would be the same as electron energy associated which electron revolving around phosphorus because all that has happened as a sign of this has changed. That really does not change the numerical value of the energy.

Again you have by the similar arguments that we have used for the phosphorus atom and because of the presence of the silicon medium the ionization energy of boron reduces drastically, energy proportional to 1 by $epsilon_r$ square, and that energy turns out to be 0.045 electron volts. Note that this method of calculating energy, ionization energy of impurities is qualitatively correct but for different impurities it is not necessary that the values you calculate by this approach will match and this is because this picture is somewhat more complicated than the simple bore model that we are assuming but that does not matter, we can still continue use this model for a qualitative understanding. Now we can proceed as we have done for the phosphorus atom and for T greater than 0K this charge carrier becomes free so it results in a positive charge hole.

Similarly, you also have a parallel process of silicon ionization which results in a hole and an electron pair. In the case of boron you are getting holes by two mechanisms; one is impurity ionization and other is the thermal generation or silicon ionization. Therefore the holes are in a majority and that is why this semiconductor will be called p-type. So, again if you see, the sources of carriers in semiconductors you have two processes.

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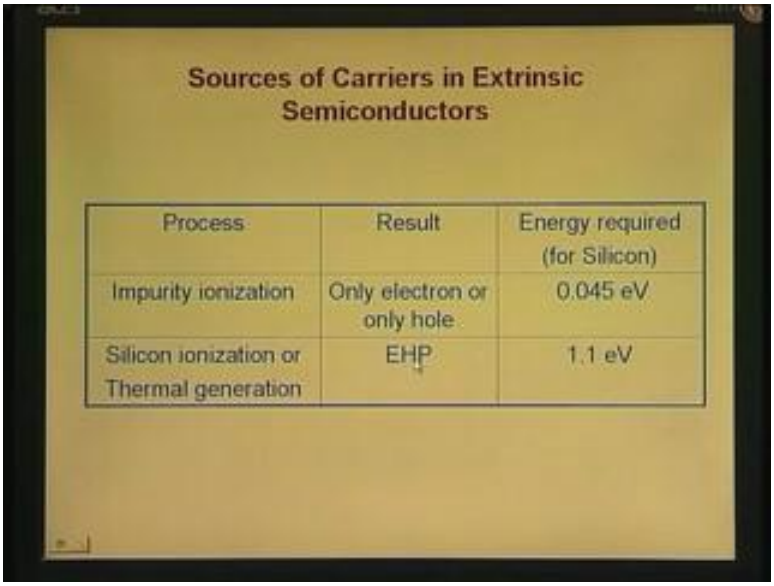

Impurity ionization in the case of boron resulting in only hole does not give rise to a free electron. Energy is 0.045 electron volts; you have silicon ionization which results in electron hole pair generation and energy 1.1 electron volts. The result will be similar to what we have drawn here for the phosphorus, the only difference being this n_{n0} will be replaced by p_{p0}.

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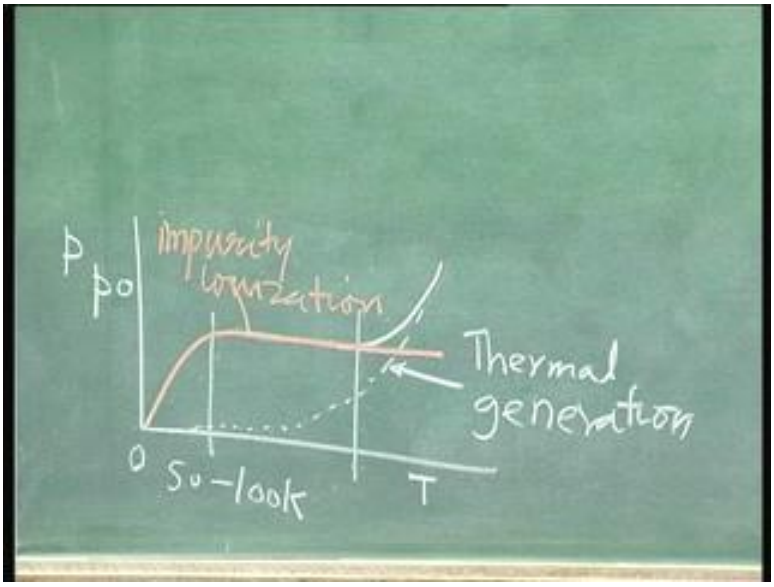

That is, the majority concentration of holes in a p-type semiconductor under equilibrium. Here you will have impurity ionization boron atoms getting ionized and ultimately almost fully ionized within the range of 50K to100K which is much lower than room

temperature and then saturation. So impurity ionization has saturated here N_a to the power minus by N_a; "N_a" is the impurity concentration; "a" stands for acceptor because boron accepts an electron or a group 3 impurity accepts an electron it is called an acceptor. And N_a to the power minus, "to the power minus" superscript indicates those fraction of N_a which are ionized. So, N_a to the power minus by N_a is lesser than or equal to 1 after 50K to100K N_a to the power minus by N_a is almost 1. So it has saturated. We have thermal generation similarly taking place which is much less for temperature less than this value. And then there after the thermal generation takes over impurity ionization and you have this curve. You have exactly a similar curve for boron impurity in silicon. We can write the relation between the majority carrier concentration and minority carrier concentration or electrons and holes in the following form.

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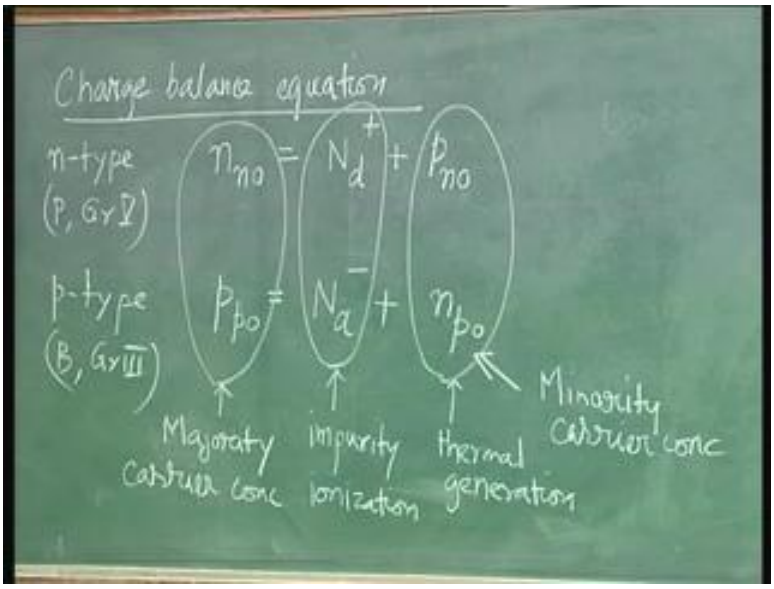

If you take an n-type semiconductor, example is phosphorus or a group 5 impurity, the equation is: the electron concentration in an n-type semiconductor is equal to the ionized impurity concentration that is the electrons contributed by ionized impurities, ionized phosphorus or donor atoms, plus the electrons contributed by thermal generation process. Since thermal generation process results in electron as well as holes the electron concentration which results from thermal generation is same as the hole concentration in an n-type semiconductor. Therefore we can write P which stands for holes in n-type semiconductor; suffix 0 under equilibrium. So n_{n0} is equal to N_d to the power plus plus P_{n0}. There is a advantage of writing the electron concentration contributed by thermal generation in terms of the hole concentration because this equation is also called the charge balance equation.

When you write it in this form electrons have negative charges, ionized phosphorus impurities or donor impurities are positive charges, and holes are also positive charges. It is like negative charges equal to positive charges; the statement of charge neutrality. That is why it is called charge balance. You can write a similar equation for p-type. So p-type

the impurity for example is boron or any other group 3 element. And here what happens, the holes are in a majority. I will write a hole concentration in a p-type semiconductor under equilibrium p_{p0} is equal to the ionized acceptor impurity concentration, that is, the carriers provided by impurity ionization plus the carriers provided by thermal generation. Again thermal generation in this case results in electron hole pair. So the hole concentration provided by thermal generation is same as electron concentration in a p-type semiconductor because the impurities do not result in a electrons.

Electrons can only be obtained from thermal generation in the case of p-type semiconductor. So I can write this as n_{p0} electrons in a p-type semiconductor under equilibrium. This is again a charge balance equation where the left hand side has positive charges and right hand side has negative charges.

There are several ways of interpreting this charge balance equation. One is in terms of balance between positive and negative charges, other way is in terms of the processes used or developed for generating these charges. So left hand side is majority carrier concentration; on the right hand side this represents impurity ionization and this represents the minority carrier concentration or the thermal generation process. This can be called thermal generation or silicon ionization, so it is impurity ionization and silicon ionization. And alternately or in addition to the fact that these carriers are created by thermal generation you know that these are the minority carriers. So, on the left hand side you have the majority carriers. This is another way of interpreting the charge balance equation.

The majority carrier concentration is provided by impurity ionization process and thermal generation process. On the other hand this equation also shows something very important, the minority carriers are provided only by thermal generation process because only this process results in electron hole pair generation.

Holes are majority in n-type semiconductor and electrons are minority carriers in p-type semiconductor. The fact that minority carriers are provided by thermal generation process is very important. We must remember this fact because later we will find that this particular fact is responsible for a slow response of minority carriers in switching conditions. With this we have come to the end of the bond model of extrinsic semiconductors. We cannot derive any further information out of this model.

As we have said we have been able to explain this particular behavior of this majority carrier concentration. So in general we could write here majority carrier concentration. And this is an impurity ionization process and this is thermal generation process so you can say this is the minority carrier concentration. We are able to qualitatively explain the shape of this majority carrier concentration versus temperature curve using the bond model. And we are able to explain why there is a significant flat range of this concentration. What we are not however able to derive from here is the concentration of minority carriers at any temperature.

We are not able to derive a value for this concentration nor are we able to derive the values of the majority carrier concentration. If you go to this graph the value of the majority carrier concentration under these conditions that is low temperatures, that is the range of partial ionization and at very high temperatures. In this range we can derive the expression for the majority carrier concentration and that is very simple because all impurities are ionized, here the majority carrier concentration is same as the impurity concentration. I will redraw this graph very clearly.

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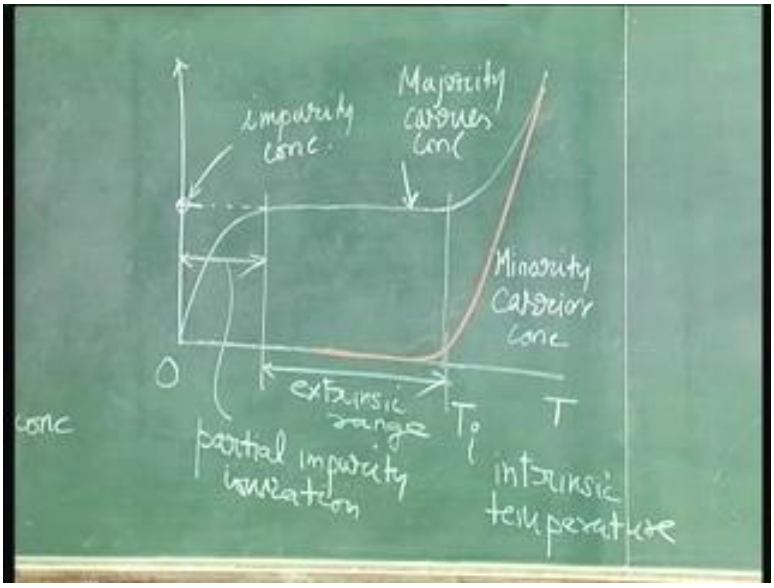

This is the flat portion. This is the temperature in a linear scale. Note that this is a linear scale and this is majority carrier concentration also on a linear scale in a semiconductor. This is 0. So I can show 0 of the majority carriers as well as the 0 of the temperature since the scales are linear. Here this flat portion we know this value is the impurity concentration. One can say why is it that this flat portion is only impurity concentration? What about though the impurities are fully ionized? There is a process of thermal generation also contributing to the majority carriers but that process is very small. That is why it is something like this, we are not able to show on the linear scale the minority carrier concentration. This is the region of partial impurity ionization. Beyond this all the impurities are ionized in this entire range this complete impurity ionization.

We can find out the majority carrier concentration, in the flat portion, in this temperature range, which is called the extrinsic range because in this region the semiconductor is extrinsic this means it is not intrinsic; that is one type of carriers are in a majority as compared to the other type. Strictly speaking even in this region the semiconductor has an extrinsic nature because minority carrier concentrations are small but the extrinsic nature is not fully developed. It is only here that the impurities which you have introduced to make the semiconductor extrinsic have fully ionized. So the extrinsic nature is fully developed only in the flat portion.

In this region the extrinsic nature is getting lost because as you can see minority carrier concentration has become equal to the majority carrier concentration. So we will shift this here. This is something like in a pure semiconductor electrons becoming equal to hole concentration; so extrinsic nature is getting lost. So this is not extrinsic range since the semiconductor becomes closer and closer to intrinsic semiconductor this is called the intrinsic range semiconductor and is entering intrinsic range. And this temperature beyond which semiconductor starts becoming intrinsic is called intrinsic temperature T_i. This is the amount of information that we have been able to derive from the bond model. Majority carrier concentration in the extrinsic range we can get very easily because it is equal to impurity concentration.

However, we need to get this region's behavior and that region's behavior also to get a complete picture. Also we need to know whether what we have shown for phosphorus and boron whether similar thing will be applicable for other impurities also? So to get a more complete picture we must go to the energy band model. The energy band model will be the next topic of discussion. Let us see if there are any questions.

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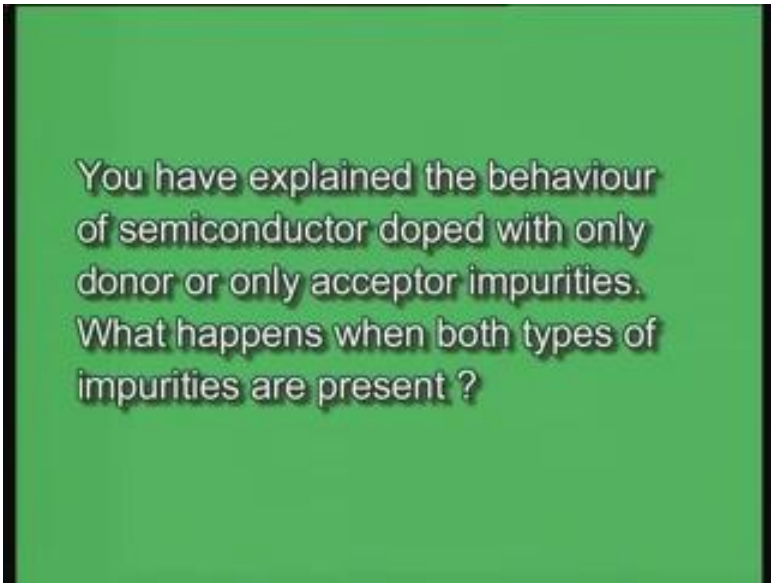

Sir, you have explained the behavior of a semiconductor doped with only donor or only acceptor impurities what happens when both type of impurities are present? When both types of impurities are present it is called a compensated semiconductor. Let us see what the picture in such semiconductors.

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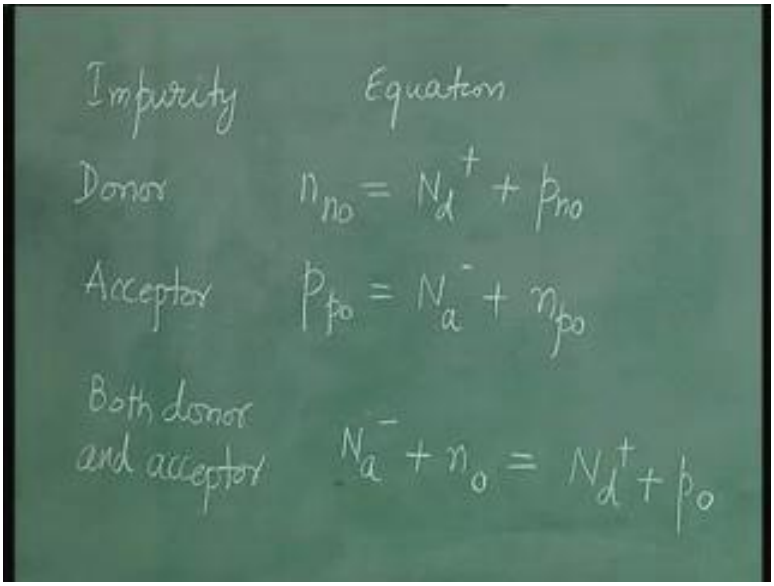

Now, here we have the table giving the impurity and the charge balance equation (refer slide). If you have only the donor type impurities, this is the charge balance equation. If you have only acceptor type impurities, then this is the charge balance equation. If you have both donor and acceptor type impurities then the charge balance equation can be constructed in a similar fashion from the knowledge of these two charge balance equations. We put all the negative charges on one side and the positive charges on other side, ionized acceptor concentration and electrons on one side, ionized donor concentration and holes on the other side.

Now notice carefully that we have not used a suffix "n" or "p" either for n_0 or for p_0. This is because we do not know if the semiconductor is n or p-type unless we know the relative magnitudes of N_a to the power minus and N_d to the power plus. So, if N_a to the power minus is greater than N_d to the power plus then it will be p-type as written here. So you have a p-type semiconductor if N_a to the power minus is greater than N_d to the power plus; this is because your hole concentration will then be more than electron concentration. The same equation has been rewritten to show this.

On the other hand, it will be n-type if N_d to the power plus is greater than N_a minus because electron concentration in that case would be more than hole concentration. So n_0 is equal to (N_d to the power plus N_a to the power minus) plus p_0. So in this manner we can determine the concentrations and polarity of the semiconductor when both donor and acceptor type impurities are present. We will have further discussion on these compensated semiconductors in the context of the energy band model. With this we have completed the discussion of the bond model of the extrinsic semiconductor. We will take up the band model in the next class.