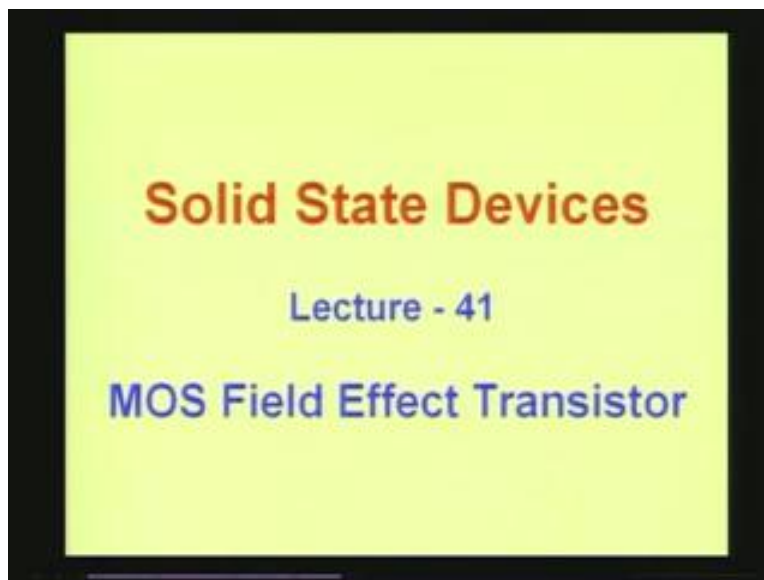


Solid State Devices
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Lecture - 41
MOS Field Effect Transistor (Contd...)

Now we come to the last lecture of this discussion on the MOSFET characteristics. This lecture will also be the penultimate lecture of the course. So we will have one more lecture which will summarize all that we have done in this course after we discuss a few advanced devices at the qualitative level.

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Coming back to the discussion on the MOSFET let us summarize what we achieved in the last class.

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$$I_D = \frac{\mu_n C_{ox} W}{L} \left[(V_{GS} - V_{BS}) V_{DS} - \frac{V_{DS}^2}{2} \right] \quad \text{for } V_{DS} < V_{GS} - V_{TS}$$

$$= \frac{\mu_n C_{ox} W}{2L} [V_{DS} - V_{BS}]^2 \quad \text{for } V_{DS} \geq V_{GS} - V_{TS}$$

$$V_{TS} = V_{FB} + V_T + \gamma \sqrt{\frac{2\epsilon_s N_A}{C_{ox}}} \quad \text{n-channel}$$

$$\gamma = \frac{\sqrt{2\epsilon_s N_A}}{C_{ox}}$$

In the last class we have written these equations which are in accordance with what is called the square law model. In these equations the current rises as a square law function of the drain source voltage for drain source voltage less than V_{GS} minus V_{TS} . This V_{GS} minus V_{TS} is the so called saturation drain source voltage. Once the transistor is in saturation according to the square law model the current is constant at this value obtained by substituting V_{Dsat} for these two V_{DS} terms. And these are the expressions for the threshold voltage and the body effect parameter which enters into the threshold voltage. Now this threshold voltage is with respect to the source.

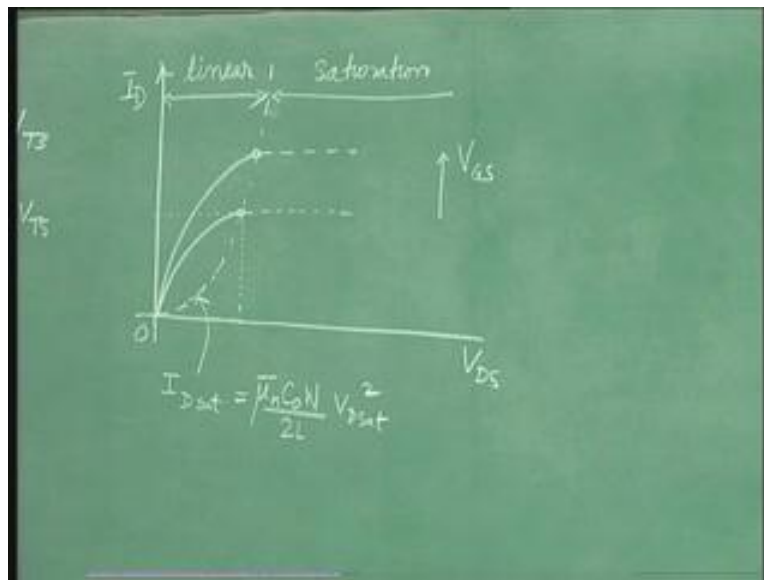
Please recall that in the MOS capacitor discussion and also in the early stages of derivation of the MOSFET characteristics we have always considered all voltages with respect to bulk. Therefore the threshold voltage expression was with respect to the bulk. Whereas in practice when you use a MOSFET the source is normally the common terminal and therefore here in these equations we are using all the terms with respect to the source. This equation also includes the body effect as you can see from the V_{BS} term coming here.

Now let us proceed further with the square law model and see what other effects we need to incorporate. The graph of this square law model is drawn here. This is I_D versus V_{DS} . This dotted line shows the separation between the linear and saturation regions. So this is the linear region, it is also called the ohmic region and this is the saturation region. Now please note that though we call this linear, strictly speaking only in a very small range near origin the characteristics are linear. This dotted line here shows the current in saturation. It is a flat line, constant and independent of V_{DS} , something that does not happen in practice.

Now what is the equation for this particular line that separates the linear and saturation regions?

This can be readily obtained from the saturation current voltage characteristics that are these particular characteristics. If you call this as a current I_{Dsat} and call this as the voltage V_{Dsat} then we have I_{Dsat} equal to this term multiplied by V_{Dsat} square. That is the shape of this particular dotted line here. So this dotted line is following the law I_{Dsat} equal to some constant which is $\mu_n C_0 W$ by $2L$ into V_{Dsat} square. So this is the saturation voltage and this is the saturation current for this curve. We similarly have saturation current and saturation voltage for the other curve. This equation represents the locus of the saturation points as a function of V_{GS} and V_{DS} . Now, how do we treat this region here where the current rises slowly because of channel length modulation.

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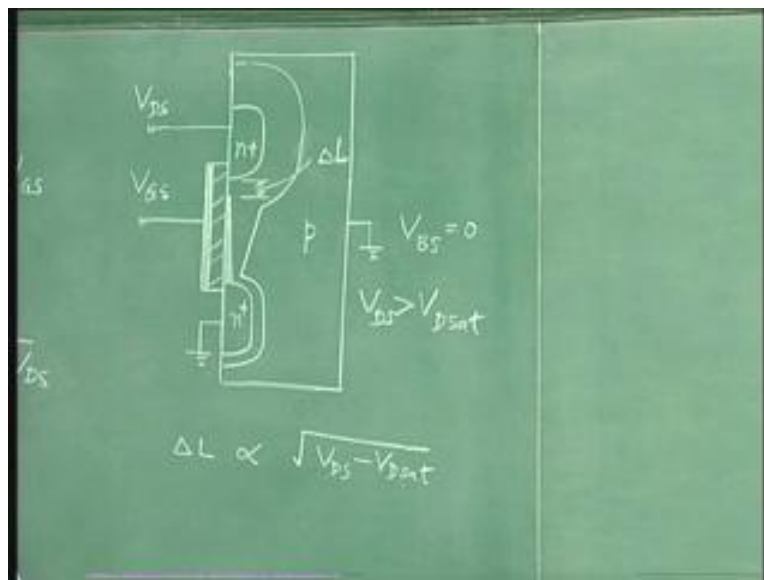


We have already explained the channel length modulation effect qualitatively using a diagram. We will redraw the diagram considering a real MOSFET. That is, this is your drain and this is your source and then you have a gate here, this is the oxide, this is the p-type substrate. Now, if you show the depletion region and the inversion charge it will look as follows: We are showing beyond saturation. So beyond saturation the picture is something like this. This is the inversion charge decreasing from source to drain and becoming 0 here and then you have a depletion layer coming like this.

The depletion layer is smaller at the source because drain to bulk voltage is more than source to bulk voltage. Of course in our characteristics we have assumed the source to be shorted to the bulk. Therefore both the source and bulk are the ground. And here you have the voltage V_{GS} and here you have the voltage V_{DS} . Now, the shift of this point from this end is the channel length modulation ΔL . Now this ΔL is responsible for the increase in current because this ΔL goes on increasing with this V_{DS} . This increase in ΔL with V_{DS} can be approximated by a square root formula of the following form: The ΔL is proportional to square root of the difference between V_{DS} and V_{Dsat} because you know that when V_{DS} is equal to V_{Dsat} ΔL is 0 so this point will coincide with this point here when V_{DS} is equal to V_{Dsat} at saturation.

Now beyond saturation the point is shifting. So we are showing these conditions for V_{DS} greater than V_{Dsat} . Now, how do you get this square root dependence of ΔL ? Well, you can do a detailed derivation which is beyond the scope of this particular course. All that we need to remember here is that when you take a PN junction and you try to express the depletion region of a PN junction in terms of the reverse bias you find that the depletion width varies as square root of the reverse bias. Now that is essentially what is being used here. So ΔL is this distance over which the electric field falls and this is a depletion layer so the width of this ΔL depletion width is a function of the reverse bias that is causing this depletion width. Now the reverse bias that is responsible for this width is V_{DS} minus V_{Dsat} . Now note that the reverse bias that is responsible for this depletion width here is V_{DS} . It is V_{DB} but since D and S are connected together because V_{BS} is 0 therefore V_{DS} is the voltage drop here so V_{DS} is responsible for this width but V_{DS} minus V_{Dsat} is responsible for this width. This is the kind of expression you have.

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Now how does this ΔL affect our equations. Let us incorporate ΔL and then we will have the equations as follows: In this particular equation which is valid for saturation we should replace L by L minus ΔL .

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$$\begin{aligned}
 I_D &= \frac{\mu_n C_{ox} W}{L} \left[(V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right] \quad \text{for } V_{DS} < V_{GS} - V_{th} \\
 &= \frac{\mu_n C_{ox} W}{2(L - \Delta L)} [V_{GS} - V_{th}]^2 \quad \text{for } V_{DS} \geq V_{GS} - V_{th} \\
 V_{th} &= V_{FB} + \phi_p + \gamma \sqrt{\phi_p - V_{BS}} \quad \text{n-channel} \\
 \gamma &= \frac{\sqrt{2q\epsilon_s N_a}}{C_{ox}}
 \end{aligned}$$

This delta L does not come into picture for this equation which is below saturation. Now we can take this L out of this particular bracket in which case the equation will get modified to L into 1 by 1 minus delta L by L. Since this delta L by L is generally small but less than 1 so 1 minus a small term much less than one can be approximated as simply 1 plus that term.

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$$\begin{aligned}
 I_D &= \frac{\mu_n C_{ox} W}{L} \left[(V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right] \quad \text{for } V_{DS} < V_{GS} - V_{th} \\
 &= \frac{\mu_n C_{ox} W}{2L} [V_{GS} - V_{th}]^2 \frac{1}{(1 - \frac{\Delta L}{L})} \quad \text{for } V_{DS} \geq V_{GS} - V_{th} \\
 V_{th} &= V_{FB} + \phi_p + \gamma \sqrt{\phi_p - V_{BS}} \quad \text{n-channel} \\
 \gamma &= \frac{\sqrt{2q\epsilon_s N_a}}{C_{ox}}
 \end{aligned}$$

So we use the approximation 1 minus delta L by L the reciprocal which is approximately equal to 1 plus delta L by L since delta L by L is much less than 1. If you do that then this will go in the numerator. That is your equation including the channel length modulation.

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$$I_D = \frac{\mu_n C_{ox} W}{L} \left[(V_{GS} - V_{TS}) V_{DS} - \frac{V_{DS}^2}{2} \right] \text{ for } V_{DS} < V_{GS} - V_{TS}$$

$$= \frac{\mu_n C_{ox} W}{2L} (V_{GS} - V_{TS})^2 \left(1 + \frac{\Delta L}{L} \right) \text{ for } V_{DS} \geq V_{GS} - V_{TS}$$

$$V_{TS} = V_{FB} + \frac{Q_f}{C_{ox}} + \gamma \sqrt{2q\epsilon_s N_A} \quad \text{n-channel}$$

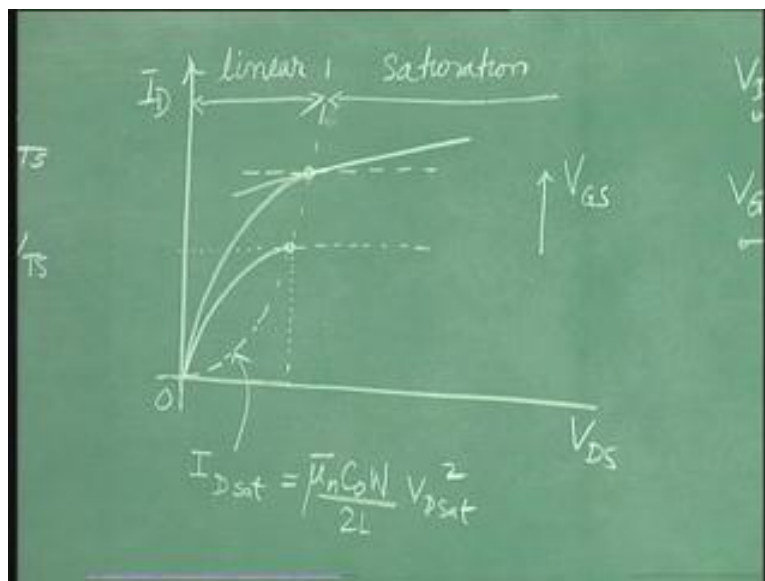
$$\gamma = \frac{\sqrt{2q\epsilon_s N_A}}{C_{ox}}$$

$$\frac{1}{1 - \frac{\Delta L}{L}} \approx 1 + \frac{\Delta L}{L}$$

$$\therefore \frac{\Delta L}{L} \ll 1$$

Now since ΔL increases with V_{DS} this particular equation shows a small increase with V_{DS} . Now let us plot this effect on the graph. So, if you draw it on the graph then what is happening is you have a curve that is slowly increasing like this. Now one problem here is that while the slope of this curve is non-zero and positive it goes like this. The slope of this particular segment according to the square law model at saturation point is 0 so you have a discontinuity in the slope here.

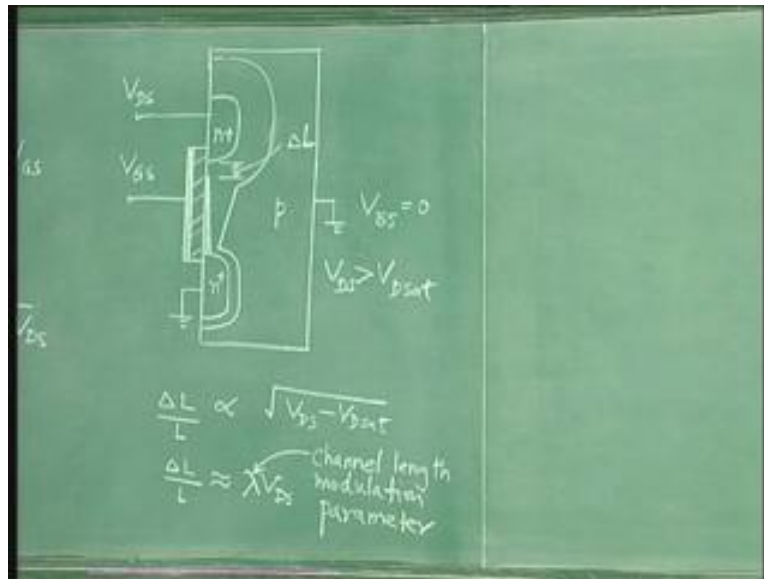
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Now, how do you take care of a discontinuity in the slope because this discontinuity is not good in modeling calculations?

A discontinuity in the slope creates problems when you use this model for computer calculations. So you can avoid the discontinuity by using the following trick. What we do is, when you want to represent this ΔL by L in terms of the drain to source voltage we use a simple empirical approximation to this square root formula. Look at this square root formula; ΔL is proportional to square root of V_{DS} minus V_{Dsat} so ΔL by L will also be proportional to the same quantity. But we write ΔL by L as proportional to V_{DS} and we include a proportionality constant that is normally represented as λ and this proportionality constant is called channel length modulation parameter.

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After doing this, what we do is we include that λV_{DS} term also in the expression below saturation. That is, here when you include the expression λV_{DS} for ΔL by L this will get changed to $1 + \lambda V_{DS}$. And then what we do is we use this multiplying term also here. So this also we multiply with $1 + \lambda V_{DS}$. Now please note, this is not physical because the channel length modulation does not take place for V_{DS} less than V_{GS} minus V_{TS} . But still for mathematical continuity of the derivative and the equation the value of these functions are such because these are two different segments.

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Handwritten equations on a chalkboard:

$$I_D = \frac{\mu_n C_{ox} W}{L} \left[(V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right] \quad \text{for } V_{DS} < V_{GS} - V_{th}$$

$$= \frac{\mu_n C_{ox} W}{2L} (V_{GS} - V_{th})^2 (1 + \lambda V_{DS}) \quad \text{for } V_{DS} \geq V_{GS} - V_{th}$$

$$V_{th} = V_{FB} + \frac{Q_f}{C_{ox}} + \sqrt{\frac{q N_a}{2 \epsilon_s C_{ox}}}$$

$$\lambda = \frac{\sqrt{2 q \epsilon_s N_a}}{C_{ox} L}$$

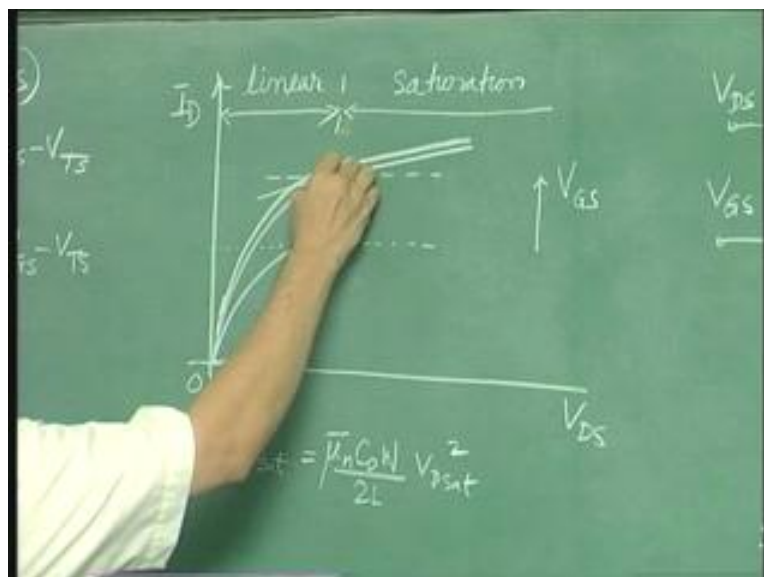
$$\frac{1}{1 - \frac{\Delta L}{L}} \approx 1 + \frac{\Delta L}{L}$$

$$\frac{\Delta L}{L} \ll 1$$

On the right, a small graph shows I_D vs V_{DS} with a curve starting at the origin and saturating.

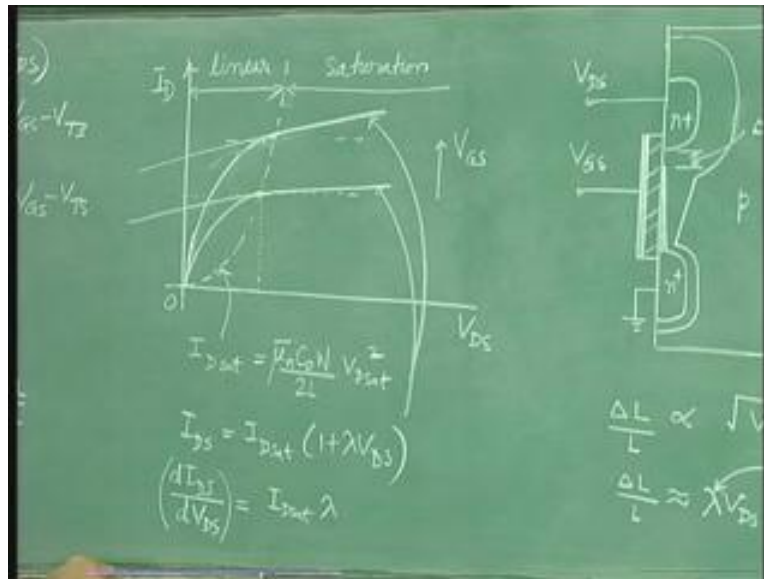
You must ensure that the segments are continuous at the point where they meet. So there should be continuity in the value of the two segments at that point and there should be continuity in the value of the derivative also. That is why this is done. Now please note since this λV_{DS} is really very small compared to 1 it does not affect this current significantly but it provides that small increase in current in saturation required here. So when you make these changes if you look at the graph the graph will now look continuous, it will be something like this. Instead of this current your current will be very slightly more but here the slope will not be 0 and it will have this slope that you require for the channel length modulation effect and that is the difference.

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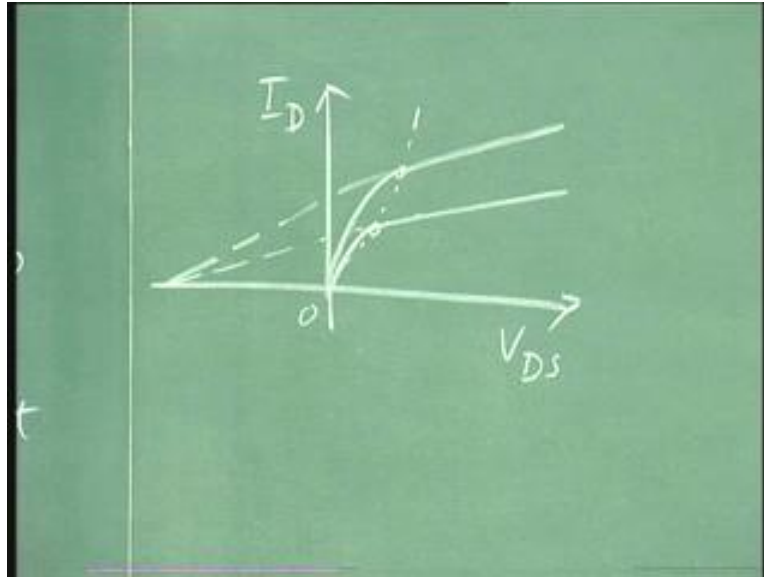
So we can remove this to avoid complication and that is a kind of curve you get, a smooth curve. Now here also you will get a similar curve except that the slope of this curve is less than the slope of this. Now that point is very clear from the mathematical equations. If you look at these equations here; I_{DS} is equal to I_{DSat} into $1 + \lambda V_{DS}$, this is the equation for this segment here. From here it is clear that dI_{DS} by dV_{DS} is equal to I_{DSat} into λ . Since λ is a constant but I_{DSat} increases with V_{GS} . Therefore the slope dI_{DS} by dV_{DS} which is the slope of this line increases with V_{GS} . In fact it increases proportional to this current I_{DSat} and as a result it extends all these lines back like this.

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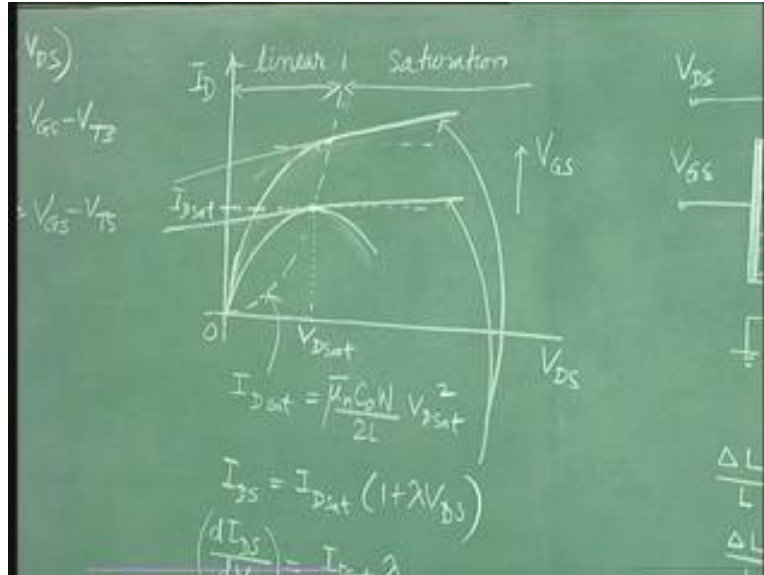
You will find that these lines will tend to meet this particular voltage axis at a common point. Now this can be shown clearly if you compress the graph. So, if you compress the graph it will look like this. And then you separate the linear and saturation regions and complete this curve. Now this is very much like what we have done for the bipolar junction transistor. Even there, if you recall we said that the way to draw the complete curve is to first separate the linear and saturation regions that is active and these regions using this line. Then you draw the curves in the active region starting from a single point and identify the saturation points. From there you connect the origin.

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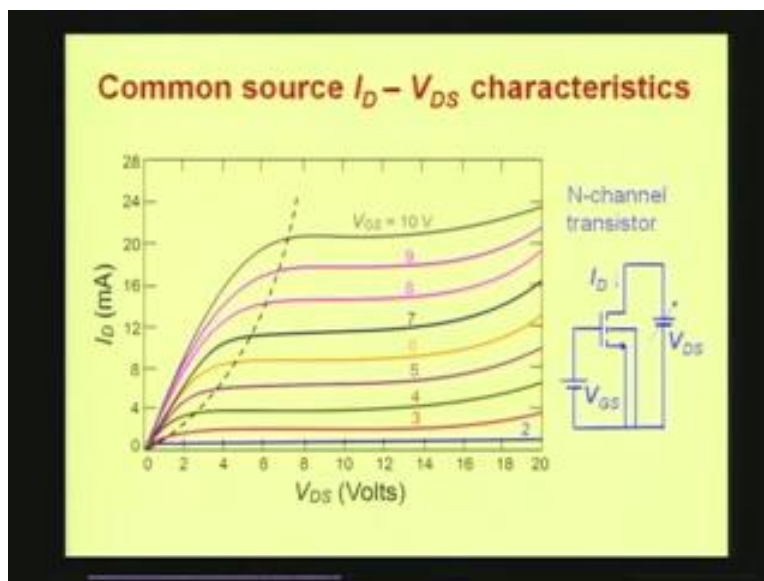
This is the way to draw the current voltage characteristics including all effects. Now let us look at the square law equation here ignoring this fine adjustment we have made for achieving model continuity. Let us just look at this equation: If you use the same equation beyond V_{DS} is equal to V_{GS} minus V_{TS} what is going to happen? If you draw the square law equation beyond this saturation point, that is, this is V_{DSat} and this is I_{DSat} . So beyond the saturation point if you draw this equation you will find that this equation will come down. It is like a parabola in shape, it will come down and here the current will decrease with voltage showing a negative differential resistance because current decreasing with voltage means the slope of the $I_D - V_D$ curve is negative which means the resistance is negative.

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Now obviously this is not physical. That is why we do not use the square law segment beyond this point. Now physically the reason why square law segment is not used is the square law characteristic is derived assuming that the inversion charge is present over the entire channel length from source to drain. But once saturation is reached the inversion charge becomes 0 at the drain and therefore beyond that point you cannot use that equation. Now let us look at the experimental characteristics which we had shown at the beginning of the discussion on the MOSFETs. Let us see the various features we explained of these characteristics. So these characteristics are shown on the slide.

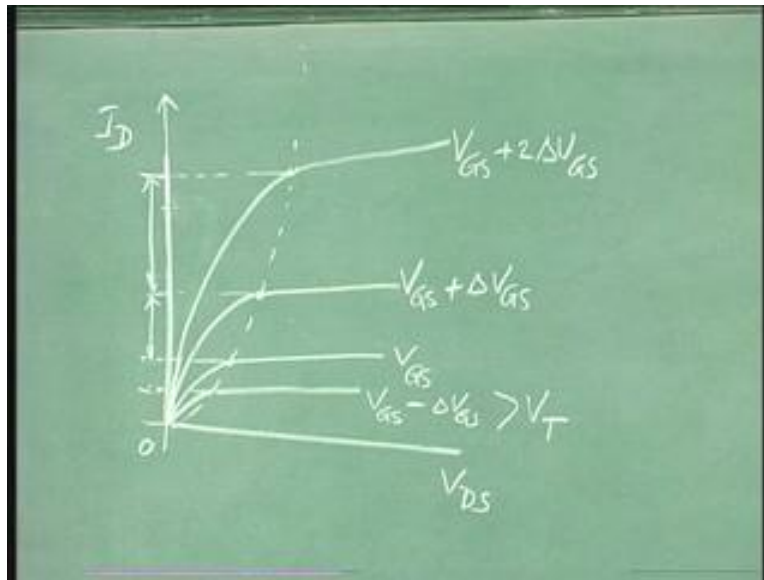
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We have explained the linear region here then the saturation region here and variation of the current as a function of V_{GS} . So this is that line, I_{Dsat} proportional to V_{Dsat} square. Now one thing you find here is that the spacing between the various current lines in the saturation region for different values of V_{GS} does not seem to follow a square law because if the segments in the saturation were following a square law and if the steps in the gate source voltage were constant, that is, if the gate source voltage was increasing in equal steps as shown in the slide then you find that the gate source voltage is increasing in steps of 1 V. So, if the gate source voltage was increasing in such equal steps then a square law means that the spacing between the currents should go on increasing because I_{Dsat} is proportional to square of the V_{Dsat} . In other words, it should be proportional to square of V_{GS} minus V_T . So, a square law means the following kind of spacing.

Suppose this is the I_{Dsat} for one gate source voltage and then you make an increment in the gate source voltage and you get another I_{Dsat} then if you make an equal increment in gate source voltage your current should be much above here. So this spacing between the saturation currents should be more than this spacing. **In fact let us exaggerate this little bit to show this clearly.** So this is the equal spacing in gate source voltage, that is, if this is V_{GS} this is V_{GS} plus some ΔV_{GS} , this is V_{GS} plus $2\Delta V_{GS}$. So this spacing should go on increasing. In fact the next spacing would be even higher and the spacing here would be lower as something like this. So this is V_{GS} minus ΔV_{GS} . Of course we are assuming that this quantity is more than V_T , all these are more than the threshold voltage.

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This is what we should have as per the square law behavior. But what we find on the slide is that the spacing between the currents does not seem to be increasing that much as you start from low values. And in fact in this region it appears to be almost kind of same. Now the reason for this is the mobility degradation. So what is happening is, here in this equation we are assuming the mobility to be constant.

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$$I_D = \frac{\mu_n C_{ox} W}{L} \left[(V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right] \quad \text{for } V_{DS} < V_{GS} - V_{th}$$

$$I_D = \frac{\mu_n C_{ox} W}{2L} (V_{GS} - V_{th})^2 (1 + \lambda V_{DS}) \quad \text{for } V_{DS} \geq V_{GS} - V_{th}$$

$$V_{th} = V_{FB} + \frac{Q_f}{C_{ox}} + \gamma \sqrt{A_0 - V_{GS}} \quad \text{n-channel}$$

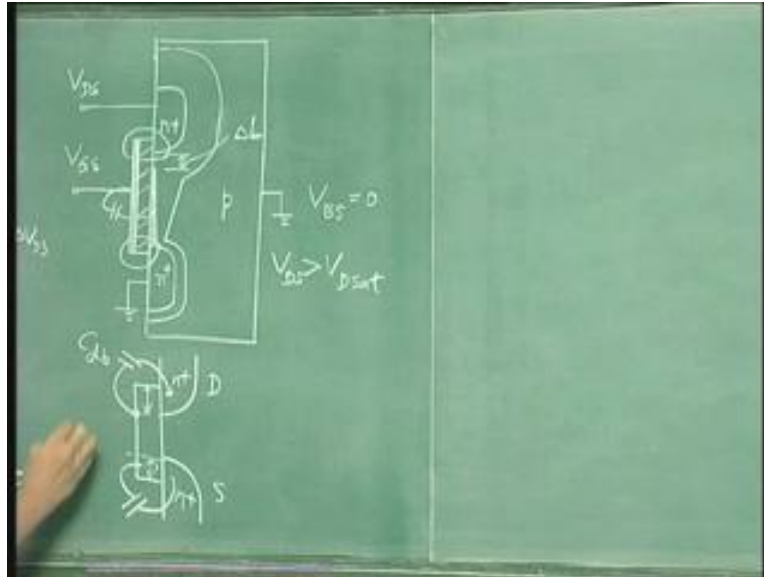
$$\gamma = \frac{\sqrt{2 q \epsilon_s N_A}}{C_{ox}}$$

So it is the same here or you can take this equation which is the equation in saturation. So we are assuming this mobility to be constant in this equation with gate to source voltage. But as gate to source voltage increases actually the mobility falls. That is why if you replace this mobility by the average mobility that we are putting here you replace this constant mobility by the real mobility with gate to source voltage. Then you will get a term dependent on gate to source voltage in the denominator and that will cancel to some effect which will be the effect of this square term and it will become almost linear in V_{GS} minus V_T . So it is the mobility degradation with gate source voltage and of course mobility also degrades with drain source voltage. So this mobility degradation is responsible for the deviation from the simple square law behavior of the saturation current versus the voltage characteristics.

Now these characteristics here are not showing the breakdown precisely but the current has started rising here in these regions so basically they are approaching breakdown. The breakdown in the case of MOSFETs is not as complicated as in the case of bipolar transistors. In bipolar transistors you had two types of breakdown voltages namely the BV_{CEO} that is the Breakdown Voltage between Collector and Emitter and Breakdown Voltage between Collector and Base BV_{CB} whereas here you do not have any such different breakdown voltages because very simply the breakdown occurs when this particular drain to bulk junction breaks down. So the breakdown phenomenon in MOSFETs is very simple. So when all the characteristics reach breakdown they will simply go up like this at the breakdown point. Now that completes the discussion of the DC characteristics.

So far all the discussions of our DC characteristics was developed assuming a surface channel MOSFET, the Physics, the equations and so on. So here this charge that is carrying the current because of inversion layer.

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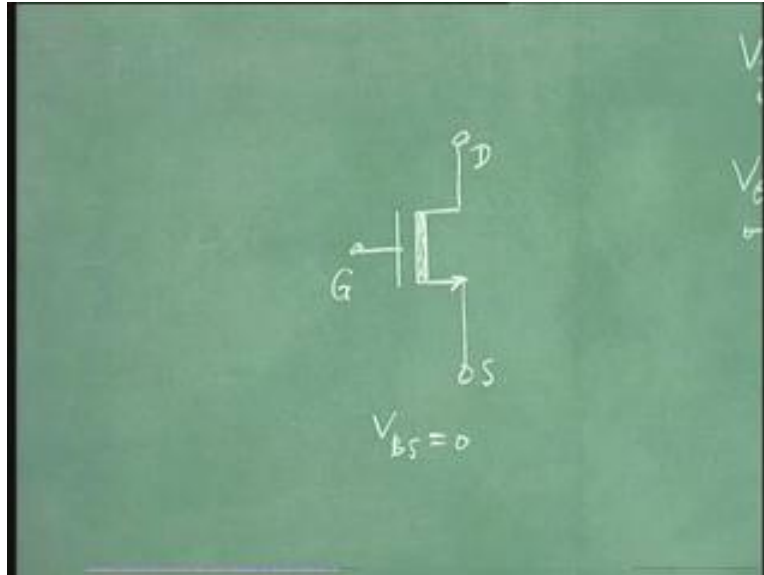


Now this kind of analysis also works for buried channel MOSFET in an approximate manner. But otherwise in a buried channel MOSFET as shown here in the slide where in the channel is because of a doped layer in such a case particularly when the doping depth is deep or the thickness of the channel from the interface is more than the theory is little more involved and the equations are little more complicated. However, whatever we have derived assuming a surface channel MOSFET is approximately valid for different types of MOSFETs we have discussed.

Symbol of this MOSFET:

So far we have been using a four terminal MOSFET symbol. For example, look at this slide. Here we have been using a four terminal MOSFET symbol because the MOSFET really has four terminals; the drain, the source, the gate and the bulk. But as shown in the slide in many applications the bulk and the source are connected together. So, in order to avoid complications in drawing a circuit consisting of a large number of MOSFETs, if for all the MOSFETs the bulk has been connected to the source it is useful to use a simpler symbol.

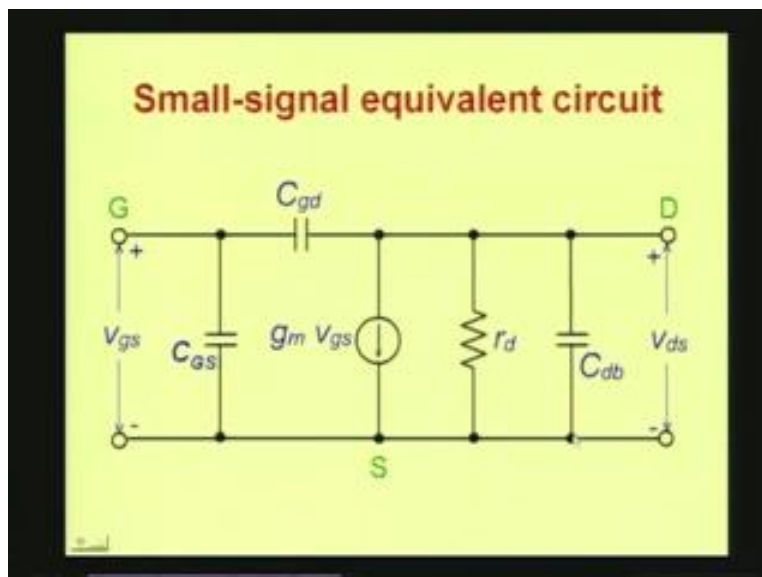
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That simpler symbol is a three terminal symbol as follows:

So this is the three terminal MOSFET symbols where the bulk has not been shown. It is assumed that bulk to source voltage is 0 wherever you use a three terminal symbol. Now how do you distinguish between a normally on and normal off device? This is a normally off device. If you want to show a normally on device all that is done is this line is made thick. So here you have gate, drain and source. Now let us discuss the small signal equivalent circuit of the MOSFET.

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Now another point to note is that the equivalent circuit is normally shown for the device working in the active region. So the bipolar junction transistor equivalent circuit was also applicable in the active region. Here in the MOSFET also this condition always holds. So the small signal equivalent circuit is shown or is used in the active region when the device works as an amplifier. Now, change in I_D because of the change in V_{GS} gives rise to a transconductance. That is why between drain and source you have a transconductance. So this is g_m and if you show the increment using a lower case letter small V_{GS} is the increment. Here you have the gate and source terminals. Therefore you are making an increment in the gate source voltage and the result is change in the drain current and that change in the drain current because of change in the V_{GS} is shown by a transconductance amplifier

Now the change in current I_D because of the change in V_{DS} is shown by a resistance. So this resistance is r_{ds} or very often this s is dropped and you simply call it r_d . In fact a part of this circuit is applicable at low frequencies. Without the capacitances this is the circuit. Now we must add the capacitances to this circuit so that it can be used at high frequencies.

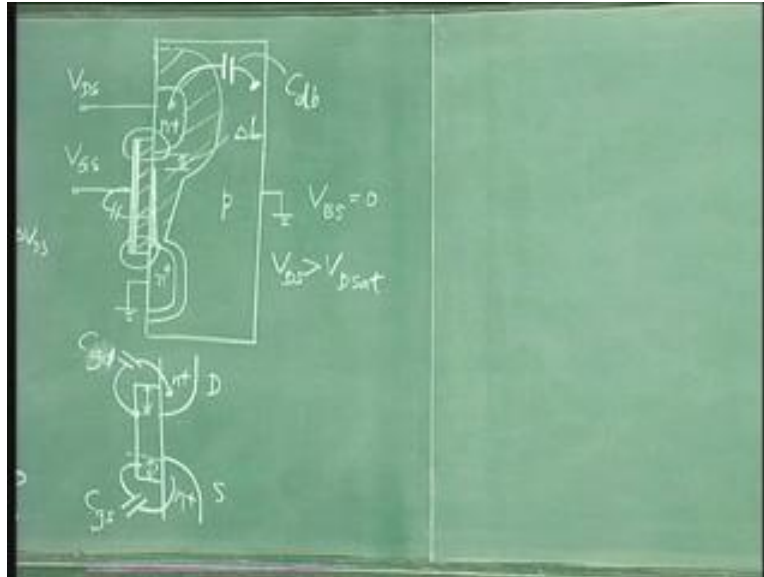
What are the capacitances?

To understand the capacitances let us look at this device structure with the various charges. If you look at this device structure you find that there is an overlap between the gate and the drain here. And similarly there is an overlap between the gate and the source here. So if I expand this then this is the source and this is the drain so this is the so called overlap region. So you have a capacitance between the gate and drain because of this which is this capacitance and similarly you also have a capacitance between the gate and source. This is source and this is drain because of overlap.

Now what about the capacitance between the gate and this channel charge?

This capacitance between the gate and the channel charge is normally separated into gate and drain and gate and source. This apportioning of this capacitance because of the channel charge between drain and source is a function of the gate source voltage. **Now this apportioning formula for this is beyond the scope of our first level course.** We will just remember that this capacitance between the gate and this charge which is this capacitance is separated between gate drain and gate source capacitance. Therefore you have only $C_{gate\ drain}$ and this is $C_{gate\ source}$.

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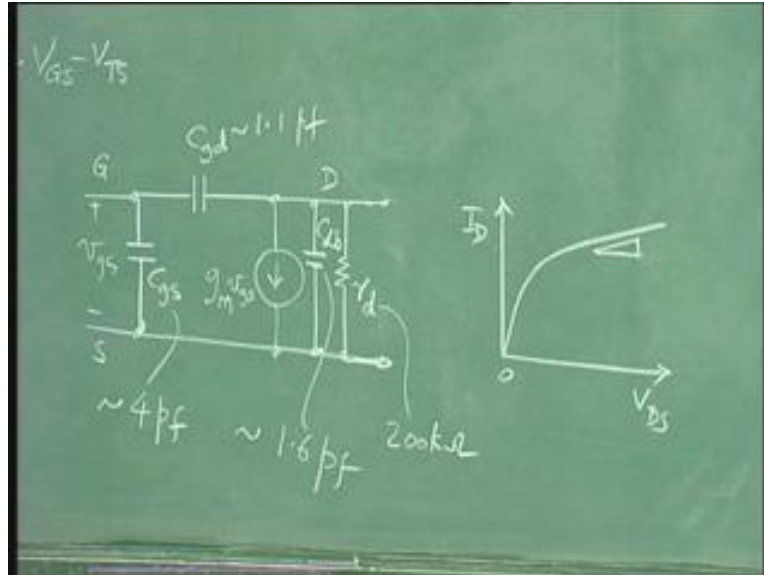
In addition to this you have a capacitance between drain and bulk because of the junction. This is the PN junction and here you have this depletion layer. So there is a capacitance associated with this. So this capacitance is actually known as C_{db} which is the C drain to bulk capacitance. Between this bulk and the source there is a common terminal here because these are shorted. Therefore this C_{db} is also appearing as C_{ds} . Now if you put these capacitances in our equivalent circuit they will appear as follows: So you have C_{gs} here you also have C_{gd} here and you have drain to bulk which appears as drain to source so you have a capacitance here C_{db} or C_{ds} . That completes the equivalent circuit.

Now you look at your slide. All the components and their origin have been identified. So this is the resistance r_d which represents channel length modulation. This current source represents the transconductance which contributes to the small signal amplification. And then for high frequency purposes you introduce these capacitances which are related to the device structure.

What are the typical values of the components?

These values depend on the bias conditions namely the drain source voltage, the drain current and so on as in the case of bipolar transistor. Now I will give you some values for some particular bias currents in a MOSFET. So, bias currents are of the order of milliamperes.

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The value of C_{gs} is 4pf, this is only an order. C_{gd} is 1.1 pf, C drain bulk is about 1.6 pf and r_d is about 200 kilo ohms. So this r_d is generally more than the corresponding resistance in the case of bipolar junction transistor. As far as the value of g_m is concerned we will do a solved example to see what this value is like.

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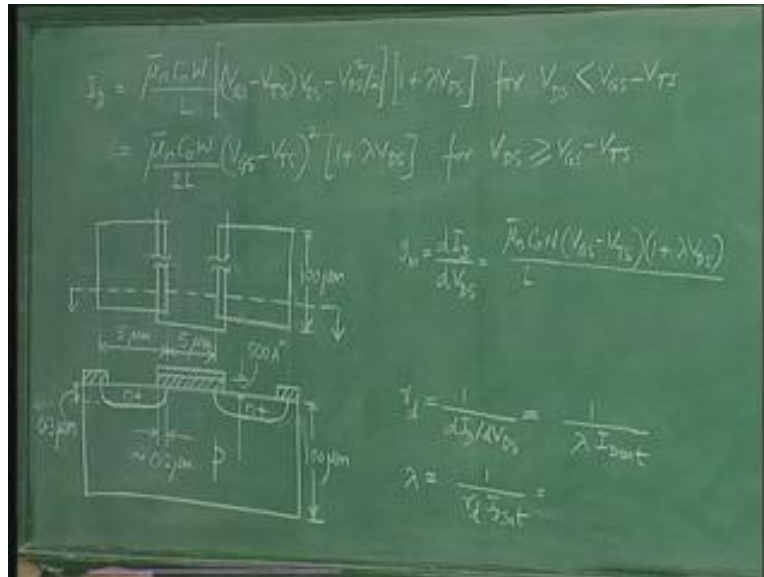
Solved example

Calculate the current and transconductance of an n-channel MOSFET having the following physical parameters: $L = 5 \mu\text{m}$, $W = 100 \mu\text{m}$, $t_o = 500 \text{ \AA}$, $\mu_n = 300 \text{ cm}^2/\text{V-s}$, $V_T = 1 \text{ V}$, and bias voltages: $V_{GS} = 4 \text{ V}$, $V_{DS} = 6 \text{ V}$, $V_{BS} = 0 \text{ V}$. What is the value of the channel length modulation parameter λ for this device, if $r_o = 200 \text{ k}\Omega$ at the given bias conditions?

This is the example: Calculate the current and transconductance of an n-channel MOSFET having the following physical parameters: Channel length 5 micron, channel width W 100 micron, oxide thickness t_o 500 Angstroms, the average channel mobility of electrons μ_n bar 300 cm square per volt second, threshold voltage V_T is 1 V and bias

voltages are V_{GS} is equal to 4 V, V_{DS} is equal to 6 V and V_{BS} is 0 V. The threshold voltage is given for V_{BS} is equal to 0. What is the value of the channel length modulation parameter lambda for this device if r_d is equal to 200 kilo ohm at the given bias conditions?

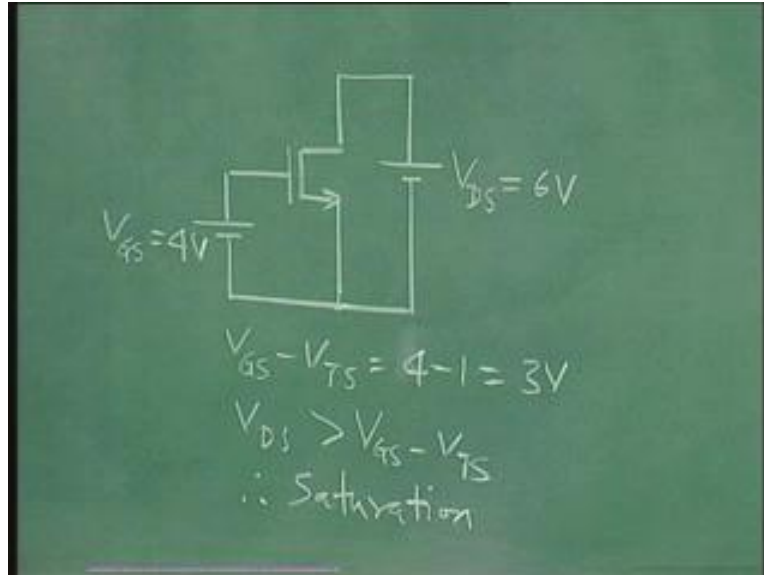
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Now let us look at the structure of the device. This is the top view and this is the cross section. The oxide thickness is 500 Angstroms, channel length is 5 micron so this is the distance between the source and drain junctions. Now, for the sake of completion some typical values of other geometrical parameters are also shown in the MOSFET. This will give an idea of the typical MOSFET geometry. So you find that the depth of this source and drain regions is about 0.3 micron, this is a rough order.

The overlap here is related to the junction depth, it is about 60 to 70% of this junction depth so this is about 0.2 microns overlap, so here also you have 0.2 microns. So the width of this gate here is more than the actual gate length which is 5 micron. Then on the top view you can see this is the width 100 microns and the width of this source and drain regions here is about 5 microns. So this diagram is not to scale because 100 microns is twenty times 5 micron so it is really long in this direction and that is why we have shown a cut. The thickness of the **wave** is 100 to 150 microns. Now let us see, what are the various equations we need to use. For this purpose let us look at the bias conditions.

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This is the circuit. Since V_{BS} is equal to 0 we are using a three terminal MOSFET. Now V_{GS} minus V_{TS} is 4 minus 1 that is 3 V. So this 3 V is less than V_{DS} which is 6 V. Therefore the device is in saturation. Since the device is in saturation you must use this equation here for the current. Now, what about the expression for transconductance? The transconductance expression is derived by differentiating this expression with respect to V_{GS} . Here g_m is dI_D by dV_{GS} .

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$$I_D = \frac{\mu_n C_{ox} W}{2L} (V_{GS} - V_{TS})^2 [1 + \lambda V_{DS}] \text{ for } V_{DS} < V_{GS} - V_{TS}$$

$$= \frac{\mu_n C_{ox} W}{2L} (V_{GS} - V_{TS})^2 [1 + \lambda V_{DS}] \text{ for } V_{DS} \geq V_{GS} - V_{TS}$$

$$g_m = \frac{dI_D}{dV_{GS}} = \left[\frac{\mu_n C_{ox} W (V_{GS} - V_{TS})}{2L} (1 + \lambda V_{DS}) \right] \cdot 1$$

$$= \frac{I_D}{(V_{GS} - V_{TS})/2}$$

$$g_{m0} = \frac{1}{dV_{DS}/dV_{GS}} = \frac{1}{\lambda I_{Dsat}}$$

$$\lambda = \frac{1}{g_{m0} I_{Dsat}}$$

So when you differentiate this square law expression you will get 2 here and you will get a linear term in V_{GS} minus V_{TS} so that is what is shown here. Now we can write this in a

more compact form as follows: You multiply and divide by V_{GS} minus V_{TS} and then you divide by 2 here and you divide by 2 here. After this you can recognize that this whole term is nothing but I_D . So, in a simple way we can write this g_m as I_D by V_{GS} minus V_{TS} by 2 so it is current by voltage which is very easy to remember. Now let us see the expression for lambda.

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The image shows a green chalkboard with handwritten mathematical derivations. At the top, it says λV_{DS} for $V_{DS} \geq V_{GS} - V_{TS}$ with a note ≈ 1.9 . The main derivation for g_m is as follows:

$$g_m = \frac{dI_D}{dV_{GS}} = \left[\frac{\mu_n C_{ox} W (V_{GS} - V_{TS})^2 (1 + \lambda V_{DS})}{2L} \right] \frac{1}{(V_{GS} - V_{TS})/2}$$

$$= \frac{I_D}{(V_{GS} - V_{TS})/2} \approx \frac{1.9 \text{ mA}}{1.5 \text{ V}} \approx 1.27 \frac{\text{mA}}{\text{V}}$$

Below this, the expression for r_d is given as:

$$r_d = \frac{1}{dI_D/dV_{DS}} = \frac{1}{\lambda I_{Dsat}}$$

Finally, the expression for λ is derived as:

$$\lambda = \frac{1}{r_d I_{Dsat}} \approx \frac{1}{200 \times 10^{-6} \times 1.9 \times 10^{-3}} \approx 2.6 \times 10^{-3} \text{ V}^{-1}$$

Now the expression for lambda is obtained as follows: You know that r_d is 1 by dI_D by dV_{DS} . If you differentiate this expression in saturation with respect to V_{DS} you will get a lambda here and you will have this quantity which we represent as I_{Dsat} . It is just this quantity without the 1 plus lambda V_{DS} is I_{Dsat} . Therefore this quantity is 1 by lambda I_{Dsat} . Therefore you can transform this and you get lambda is equal to 1 by r_d into I_{Dsat} . Now we can calculate the numerical values.

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The image shows handwritten calculations and a circuit diagram on a green chalkboard. The calculations are as follows:

$$I_{Dsat} = \frac{300 \times 71 \times 10^{-9} \times 20 \times 10^{-4}}{2} \left(\frac{1 \text{ V}^2}{1 \text{ V}^2} \right) \left(\frac{1 \text{ V}^2}{1 \text{ V}^2} \right) \text{ V}^2 \text{ A}$$

$$\approx 1.9 \text{ mA}$$

Below the calculations, there is a circuit diagram of a MOSFET. The gate is connected to a 9V source ($V_{GS} = 9\text{V}$), the source is connected to ground, and the drain is connected to a 6V source ($V_{DS} = 6\text{V}$). The threshold voltage is indicated as $V_{TS} = 1\text{V}$. The gate-source voltage is calculated as $V_{GS} - V_{TS} = 9 - 1 = 8\text{V}$. The drain-source voltage is $V_{DS} = 6\text{V}$. The condition $V_{DS} > V_{GS} - V_{TS}$ is noted, leading to the conclusion that the MOSFET is in saturation.

First we calculate I_{Dsat} . This is μ_n bar 300 cm square per volt second, this is C_0 71 Nano Farads so this is f by cm square 10 to the power minus 9 here for Nano Farad. Then this is W by L, this is V_{GS} minus V_T square that is 3 square so 3 V square by 2. Now you can see the units. So 1 V cancels here, f into V is equal to coulomb by second is ampere so the unit here is ampere. So if you complete the calculation you will get this as about 1.9 milliamp. Now we can substitute this 1.9 mA here to find out lambda so here lambda is 200 kilo ohms into I_{Dsat} is 1.9 mA. Obviously the unit is: kilo ohm into milliamperes is 1 by V. This result is 1 by 380 which will be about 2.6 into 10 to the power minus 3 V so this is your lambda.

Finally we can evaluate the g_m . To evaluate the g_m we have to find out I_D . This I_D is I_{Dsat} into 1 plus lambda V_{DS} as you can see from here. This is I_{Dsat} into 1 plus lambda V_{DS} . Now actually this lambda V_{DS} term is going to be rather small. We can neglect it, we can in fact assume that it is approximately I_{Dsat} itself and so your result will be 1.9 milliamperes by 1.5 V and this is 3 by 2. So this is approximately 1.27 mA by V. So that is the kind of g_m you have. These are the typical values of the various parameters. With that we complete the solved example. Now as a final topic we will compare the MOSFET along with the BJT.

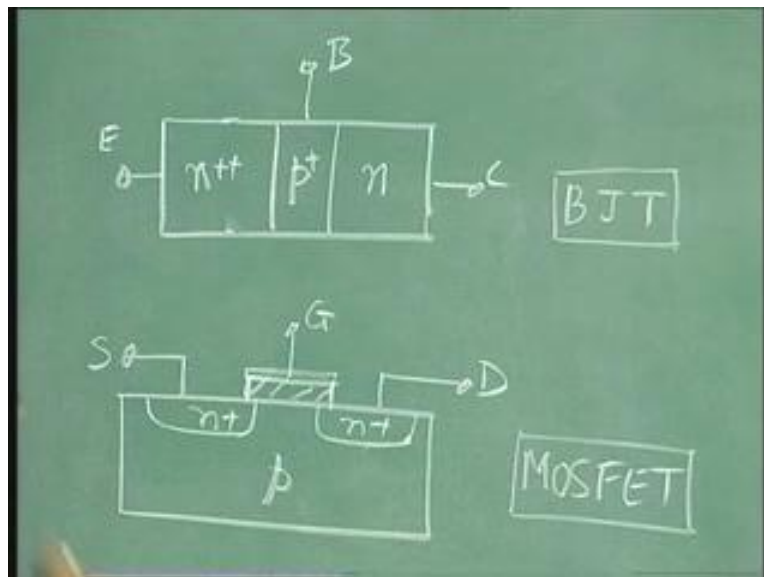
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	BJT	MOSFET
Structure	Unilateral	Bilateral
Current flow	Minority carrier Diffusion	Majority Carriers drift
Small-signal f_m $\frac{f_m}{f_T}$	f_T , high Geometry independent low to moderate	f_m , low Geometry dependent high
Current gain	$\beta \sim 50-150$	Very high
Breakdown	$BV_{CEO} < BV_{CBO}$ Second breakdown	— No such problem

What are the differences in the operation of these two devices?

Here is a table which shows the differences. In this column we have listed the various aspects of the two devices we are comparing. Let us take the first the structure of the device. The BJT is a unilateral device whereas the MOSFET is bilateral. Let us see what we mean by this.

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This is an n-p-n BJT and this is an n-channel MOSFET. Both these carry current due to electrons. You can see that the emitter is very heavily doped compared to collector so you cannot interchange collector and emitter whereas in the MOSFET you can interchange

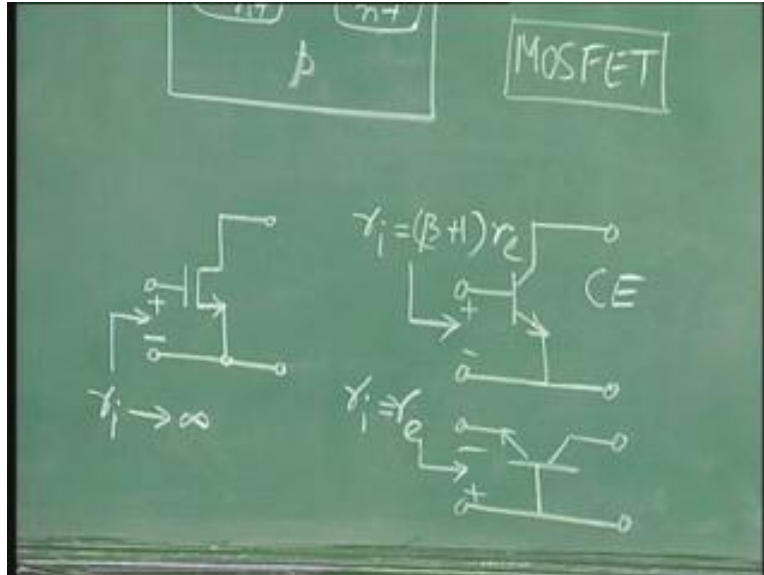
the source and drain because these are identical. So current can flow either this way or the other way. This has great advantages. The MOSFET can be used as a bilateral switch in many applications. The next thing is to see is the current flow.

In BJT the current flows because of excess minority carriers whereas in the MOSFET the current flows because of majority carriers. Now students sometimes have a doubt that the inversion layer of electrons is actually made of minority carriers as far as the substrate is concerned. Now please note that, in inversion layer the concentration of the carriers, let us take a p-type substrate, concentration of electrons in the inversion layer is more than that of holes. So in the inversion layer the electrons are only the majority carriers though they may be minority carriers as far as the bulk substrate is concerned. Now the current flows by diffusion in BJT whereas it flows by drift.

We will see some advantages of this in the case of MOSFET. Let us see the small signal parameters. And next the most important parameter is the g_m which tells you how much gain you can get. In the BJT the g_m is I_c by V_t whereas in the MOSFET it is I_D by V_{GS} minus V_{TS} by 2 that is half of this difference between V_{GS} and V_{TS} . So if you compare the g_m s of the same collector and drain currents the g_m of the BJT will be very high because this V_t is 0.026 V whereas this term half of V_{GS} minus V_{TS} is of the order of volts. Another property related to this g_m is that this term here of the MOSFET depends on the geometry of the device.

The threshold voltage depends on the geometry. Therefore the value V_{GS} minus V_{TS} for any I_D depends on the geometry. So g_m is geometry dependent in the MOSFET whereas in the BJT this V_t is independent of any geometry which is a great advantage and therefore it is geometry independent in the case of BJT. So, high g_m geometry independent which is independent of the structure is a great advantage for the BJT. Let us look at the input impedance of the BJT. Now there are two possibilities; you have the common base or the common emitter mode. Let us compare these two.

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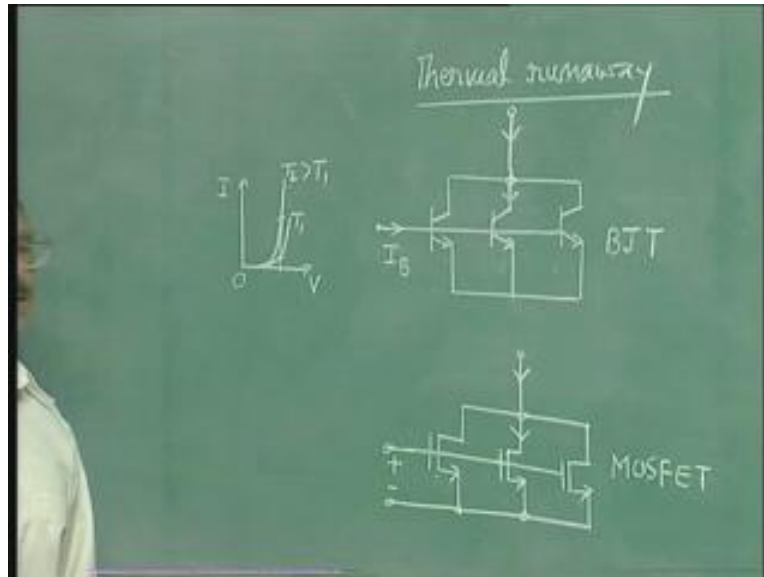


You also have common collector but even there the input impedance is same as common emitter. So, in the common emitter you find that the input impedance is beta plus one times r_e which is of the order of kilo ohms because r_e is of the order of tens of ohms. In the common base it is r_e of the order of tens of ohms. These resistances are not very high because you are seeing a forward bias diode in a BJT when it is used as an amplifier whereas in a MOSFET the input impedance is very high because there is an insulator between the gate and the channel.

Now look at the current gain. In the case of BJT the current gain from base to collector is 50 to 150 whereas it is very high in the case of MOSFET because there is really no input current into the gate. Finally the breakdown: In BJT you have at least two different breakdowns BV_{CEO} and BV_{CBO} so this breakdown is much less than the other breakdown. The breakdown between collector and emitter is much less than the breakdown between collector and base. Now in the case of MOSFET however there is no such problem. So breakdown voltage between drain and source is the same as breakdown voltage between drain and bulk.

A very important thing we should consider related to breakdown is the mechanism of second breakdown which afflicts the BJT. Let us understand this mechanism with reference to the diagram here which shows a parallel combination of devices.

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This kind of a parallel combination is used to increase the current carrying capability. So, instead of making one device with large current carrying capability you can parallel various devices so that you get an effective device which has high current carrying capability.

Now here because of the imbalance in the structures of the devices how much ever you try to make these devices identical there will be some imbalance because this one device will take more current than other devices. Since the voltages are the same for all the three devices because they are in parallel the device which takes more current dissipates more power, it gets heated up. And as it gets heated up it further increases the current because you know in a bipolar transistor the current voltage characteristics of the emitter junction is like a diode.

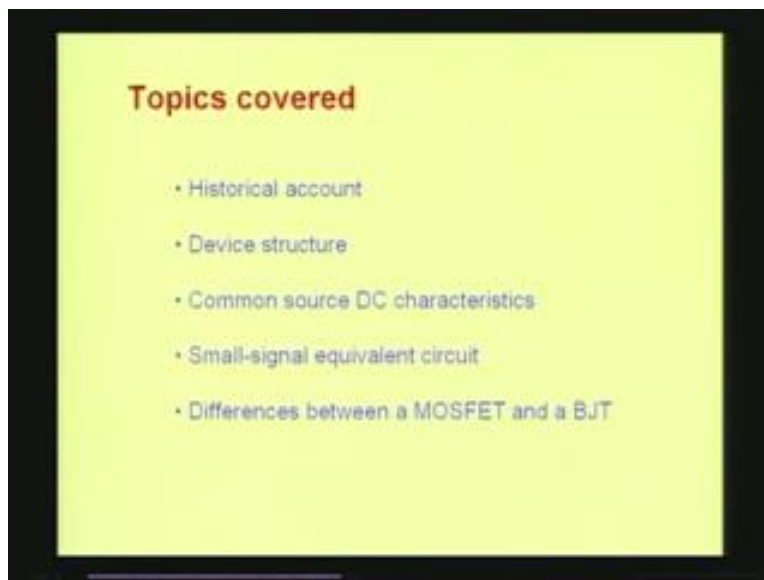
Clearly see that for a higher temperature for any give voltage the current is more. So here all the three have the same base to emitter voltage. So here the current will be more if it is at a higher temperature. This will further increase the power dissipation and further raise the temperature. This is like a thermal runaway. It is a situation going out of control and this device will end up **hogging** all the current and in the process heated up and it may also get destroyed. Whereas in the case of MOSFET no such thing happens, let us see why?

Here, if there is an imbalance between these three devices and because of that this device takes maximum current it gets heated up. But since in the MOSFET the current is because of drift and therefore the MOSFET behaves like a resistor and you know that the mobility falls with temperature around room temperature range where the devices are used therefore the resistance increases. This means that if any device gets heated up because of increase in resistance as compared to other devices its current will fall. So this is a negative feedback situation and because of this the current will get equalized among

all the devices. It is a great advantage in the case of MOSFET that you can parallel the devices without any second breakdown problem.

In summary those are the differences between the BJT and the MOSFET. What we find is that the BJT has a great advantage of very high geometry independent g_m but it has disadvantages that it is not a bilateral device unlike the MOSFET. Also, it has a second breakdown problem unlike the MOSFET which does not have any such problem. So you see that there are advantages and disadvantages that is why both devices exist today for different applications though the MOSFET is more suitable than BJT definitely from the integrated circuit point of view. Now with that we come to the end of the discussion on MOSFETs.

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Let us make a summary of all that we have done in the last few lectures on MOSFET. First we discussed the historical account of how these devices evolved. Then we discussed the device structure and fabrication. Then we considered the DC and small signal characteristics. Here we started with a qualitative analysis and then we wrote down the equations. And finally we discussed the differences between a MOSFET and a BJT. Now it is emphasized here that our discussion on MOSFETs was parallel to the discussion on BJT. So we considered a certain set of topics for both these devices in a certain order.

Now the next lecture will be the last lecture of this course wherein we will discuss some advanced devices in a simple manner and also summarize all that we have done in this course.